# Design of a Wideband Amplifier to test Instrument Current Transformers in the Supraharmonic Range

Andrea Mariscotti
*DITEN*
*University of Genova*
*Genova, Italy*
0000-0002-0096-7305

***Abstract*—Testing of current Instrument Transformers relies on low-distortion wideband generation, in particular for the modern exigency of extending testing in the supraharmonic range (up to $150\,\mathrm{kHz}$). Whereas single-tone amplitude accuracy and controllability has been mostly considered so far, low-distortion for non-linearity verification and transient behaviour in presence of commutating semiconductor devices are also relevant. The design of a stable, accurate and low-distortion amplifier is discussed, featuring $15\,\mathrm{A}$ output and sub-$\mu\mathrm{s}$ rise time in the present realization, but scalable to higher current. Design solutions were selected that can be easily replicated, including minor variants to adapt to different exigencies. Preliminary experimental results of the prototype are reported.**

***Index Terms*—amplifiers, current measurement, distortion, instrument transformers.**

## I. Introduction

It is commonly acknowledged that in modern grids power quality problems occur no longer only for the well-known harmonics, but distortion at higher frequency must be considered, due to the extensive use of static conversion technology. This applies to both low-voltage (LV) and medium-voltage (MV) scenarios, as discussed in [1]. The number of power converters directly connected to the distribution grid has increased, due to the significant presence of renewables (in particular photovoltaic parks, both at the LV and MV level, and wind parks, mostly at the MV level due to their considerable power rating) and of charging stations and supply points (for various forms of electromobility [2]). Recent studies have shown that significant distortion takes place well up to $500\,\mathrm{kHz}$ [1], [3], as confirmed by the latest update of the IEC 61869-1 [4], slightly beyond the supraharmonic range ($2\,\mathrm{kHz}$ to $150\,\mathrm{kHz}$).

Instrument Transformers (ITs) are collectively the devices for measurement of voltage and current at LV and MV levels with increasing requisites of bandwidth and accuracy through the years, following the development and update of IEC 61869 standards [5]. Focusing on current measurements, a wide range of sensors may be considered under the general "IT" classification, both active and passive [6]–[8].

The verification and calibration of current sensors comprises applying of complex waveforms, at fundamental and high-frequency components superposition [9]. The response with a transient DC offset has been long studied, especially for conventional current transformers, as it affects reliability of operation of the connected protection relay [7]. On the other hand fast transients may originate from lightning phenomena, switching manoeuvres and semiconductor commutation within power converters. The latter are becoming more and more common, with the widespread deployment of renewables and the use of SiC technology. In [10] it is demonstrated that when using a LEM Hall-effect sensor in the DC link of a SiC converter two noise contributions with different time scales take place: a rapid directly coupled through parasitic capacitance term with duration of some hundreds $\mathrm{ns}$ and a secondary slower noise term coupled onto the internal Hall-effect sensor, with dynamics of some $\mu\mathrm{s}$.

On this topic the 22NRM06 ADMIT Project [4], [11] was recently funded in the European Partnership in Metrology framework. The project aims at identifying suitable indexes and parameters to define the accuracy of voltage and current ITs and studying test and measurement instrumentation and setups with an extended frequency capability up to $150\,\mathrm{kHz}$.

A significant example of such characterization for current sensors [9] shows superposition of low- and high-frequency test current waveforms by using a suitably arranged summing circuit driven by two transconductance amplifiers (TAs) limited however to $100\,\mathrm{A}$. TA distortion is not addressed, from which the present work that proposes a robust architecture for a general purpose amplifier with similar capability, but with lower distortion and reliable transient behaviour. The architecture is scalable, so that even more demanding exigencies may be fulfilled.

The rest of the paper presents the requirements and design of the amplifier in Section II and the first experimental results of characterization of the prototype in terms of stability, transient response and distortion in Section III.

## II. Amplifier requirements and design

### A. Requirements

Some requisites for bandwidth, transient response and distortion may be derived:

- frequency band extended up to $150\,\mathrm{kHz}$, an upper corner frequency define with more than one criterion, namely attenuation, signal distortion and transient response;
- maximum distortion of $< 1\,\%$ to allow IT tests with clean sine signals;

- transient response exempt from oscillations and overshoots, with rise time complying with the $150\,\mathrm{kHz}$ bandwidth with a margin, better than $1\,\mu\mathrm{s}$.

For the selection of the architecture and its design, besides the performance requirements above, the characteristics that must be privileged are:

- stability, verified by stressing extreme conditions, such as large dV/dt and capacitive load;
- thermal and electrical robustness, selecting devices with large power dissipation and large voltage tolerability, de facto ensuring a large SOA (safe operating area);
- scalability, not only achieved by the large voltage tolerability, but also by the possibility of adding elements to the output stage within its driving capability.

### *B. High-level design*

The schematic of the amplifier is shown in Fig. 1.

Stability and robustness call for an emitter-follower output stage that features a low output impedance and almost unitary voltage gain. Constant output current would be achieved by selecting a common-base architecture, reaching a large voltage gain and output impedance. However, stability would be a major issue, relying on a carefully designed feedback using various compensating circuits, and requiring extensive verification for challenging reactive loads and parasitics.

Thermal and electrical robustness are pursued by selecting large-power transistors for the output (FJA4213 [12] and FJA4313 [13]), with $250\,\mathrm{V}$ of maximum collector voltage, $130\,\mathrm{W}$ of dissipation and a transition frequency of $30\,\mathrm{MHz}$, ensuring a current gain $h_{fe}$ equal to the nominal DC gain of 100 up to $300\,\mathrm{kHz}$.

Each NPN-PNP output transistor pair can handle $3\,\mathrm{A}$, intended as steady DC signal, reaching $6\,\mathrm{Apk}$ for AC signals there alternating conduction between the NPN and PNP devices. Larger current is allowed in transient conditions. A trade-off for the emitter resistors ($R_{11}$, $R_{12}$, etc. and $R_{21}$, $R_{22}$, etc.) was achieved, selected as $0.22\,\Omega$ and $5\,\mathrm{W}$ dissipation.

They are biased and driven by the driving pair (2SC4793 [14] and 2SA1837 [15]), that are moderately fast transistors with a transition frequency of $50\,\mathrm{MHz}$ for the designed bias current of $15\,\mathrm{mA}$, ensuring large bandwidth even at low collector current. This is an important point with metrological relevance to avoid deterioration of waveform quality, while swinging from low to high current values if at the bandwidth limits of $150\,\mathrm{kHz}$.

Biasing of the output transistors may be kept low to avoid power consumption (it will be identified as "$1.4\,\mathrm{mA}$ diode bias current", leading to about $18\,\mathrm{mA}$ to $20\,\mathrm{mA}$ through each transistor pair and a final temperature of $28\,^\circ\mathrm{C}$) or increased to reduce distortion at high frequency ("$2.7\,\mathrm{mA}$ diode bias current" condition, leading to about $150\,\mathrm{mA}$ through each transistor pair and a no load temperature of $50\,^\circ\mathrm{C}$). The output transistor pairs do not feature significant variation of their transition frequency with current.

The biasing diodes are epoxy glued on the mechanical support of the 5 output transistor pairs, following their temperature conditions to improve stability with temperature.

The preceding stage 1 is designed around two OAs in inverting gain configuration for better stability: due to the unitary gain of stage 2, the driving Operational Amplifier (OA) must swing the entire desired output voltage, so a $\pm 40\,\mathrm{Vpk}$ OA was chosen. The other reason for selecting the OPA453 is that it has better distortion than its companion OPA452 (about $-70\,\mathrm{dB}$ at $50\,\mathrm{kHz}$ contrasted to only $-50\,\mathrm{dB}$).

Similarly, another competitor might have been the ADHV4702-1 [16], used in [17] to test a voltage IT, that reaches $\pm 100\,\mathrm{Vpk}$, but whose harmonic distortion goes above $-70\,\mathrm{dB}$ already at $10\,\mathrm{kHz}$ with a steep slope.

The OPA453 requires a minimum gain of 5 for stability, and it was assigned a gain $G_5 = 10$, setting the preceding OA to $\pm 2\,\mathrm{Vpk}$ output swing, when the maximum $\pm 20\,\mathrm{Vpk}$ output is required. This input OA is an OPA27 for a matter of bandwidth, negligible distortion and availability in PDIP package for the prototype. It's gain is $G_6 = 5$, guaranteeing stability and use of low-amplitude signal generators.

The two OAs with such gains guarantee a bandwidth of $1\,\mathrm{MHz}$, so with margin on the $150\,\mathrm{kHz}$ target. A limiting factor is the unavoidable phase rotation typical of OAs that at $100\,\mathrm{kHz}$ approaches $90\,\mathrm{deg}$: care was taken for stability margin when crossing the $0\,\mathrm{dB}$ line, although, we will see, it may occur in case of fast transient excitation.

Considering the transient response, the two OAs were also selected to provide a slew rate of some $\mathrm{V/\mu s}$: $1.9\,\mathrm{V/\mu s}$ for the OPA27 and $7\,\mathrm{V/\mu s}$, ensuring a reliably fast response down to about $1\,\mu\mathrm{s}$, without seriously affecting stability.

### *C. Detailed design*

Some further details are provided indicating more accurately bias quantities, margins and electrical behaviour.

The target $3\,\mathrm{Apk}$ maximum emitter current for each pair (compatible with the SOA of the output transistors and providing $15\,\mathrm{A}$ in total) translates into a $30\,\mathrm{mA}$ peak base current, assuming $h_{fe} = 100$ is preserved. The driving pair feeds the 5 output stages in parallel with a target peak current of $150\,\mathrm{mA}$ plus some additional current through $R_{31}$ and $R_{32}$.

The base current required by the driving transistors is thus about $1.5\,\mathrm{mA}$ to $2\,\mathrm{mA}$ and this must be provided by the output of stage 1 ($I_{o1}$). An important point is that, while feeding this driving current, the instantaneous diode current varies, causing some additional distortion. This deserves attention to further improve distortion performance and may be addressed by designing a constant current source to replace $R_{41}$ and $R_{42}$. This current source must source a larger bias current, larger than $I_{o1}$, and able to withstand the full voltage swing. A circuit exploiting N and P JFETs (junction field-effect transistors) [18] is out of question, as they do not go above $30\,\mathrm{V}$ to $40\,\mathrm{V}$ of drain voltage. This will be part of the design optimization in the course of the project.

It is underlined that the output stage 2 distortion is reduced when it will operate in closed loop by the ratio of the open-

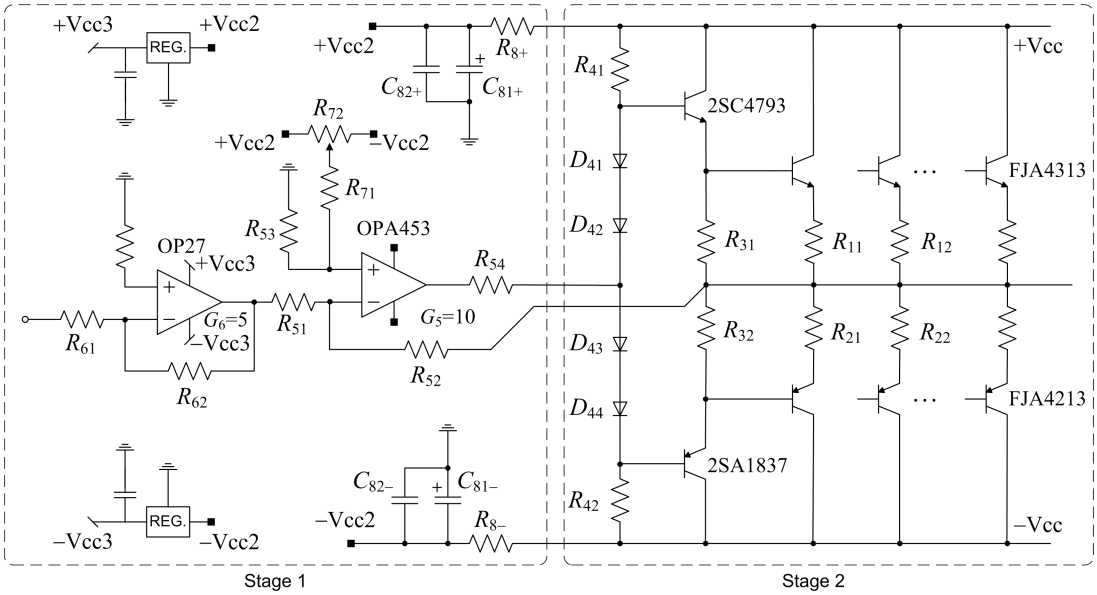



Fig. 1. Schematic of the amplifier showing stage 1 with an Operational Amplifier (OA) architecture and stage 2 with a cascaded emitter-follower architecture.

loop to closed-loop voltage gain of the driving OA stage. As a consequence of the feedback and OAs phase rotation, the absolute stability of the emitter-follower power stage is somewhat deteriorated, although the design margins are such to ensure a $150\,\mathrm{kHz}$ useful range and $0.2\,\mu\mathrm{s}$ rise time.

## III. Experimental characterization

The results reported and commented in this section provide experimental confirmation for the following points:

- nominal amplifier gain, namely ratio of output and input voltages ($V_o$ and $V_i$) at low frequency for various operating conditions;
- distortion of the output waveform at various input signal frequencies around the designed distortion corner frequency (with this term it is meant not the ability of the amplifier simply to deliver the output voltage waveform with a suitably large rms value, but to deliver without appreciably worsening waveform distortion);
- system poles and full bandwidth, observing the behaviour when excited with a step signal with adjustable rise time.

Results for each point are reported in the following in the respective subsections.

### A. Preliminary check

The final stage 2 of the amplifier, after being assembled, was preliminary checked for correct biasing and symmetry of the 5+5 output power transistors and of the driving transistor pair. A few attempts were taken of varying the current in the bias diodes, as well as the stability vs temperature was checked over about 30 minutes of operation with a temperature sensor fixed to the main heatsink in proximity of the 3rd transistor.

The DC bias measurement was taken after a warm up of 5 minutes and then after another 30 minutes of operation

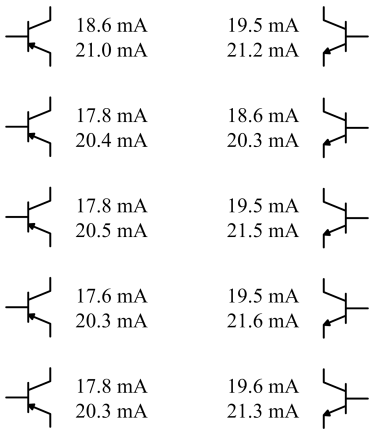



Fig. 2. Verification of the DC bias at 5 and 35 minutes from switch on, corresponding to $20\,^{\circ}\mathrm{C}$ to $22\,^{\circ}\mathrm{C}$ (initial temperature value with still gradient among the devices) and $28\,^{\circ}\mathrm{C}$ (regime temperature after 30 minutes, using the $1.4\,\mathrm{mA}$ diode bias), shown at top and bottom next to each transistor.

with the heatsink not completely fastened without the finned heatsink (that requires the box closed to work and impedes this type of measurements).

These measurements refer to the configuration with $1.4\,\mathrm{mA}$ diodes bias causing, as seen during the tests, slightly higher distortion. The remedy is doubling diode current to $2.7\,\mathrm{mA}$ that makes the current through the power transistors jump to about $150\,\mathrm{mA}$ and the no-load temperature to about $45\,^{\circ}\mathrm{C}$. Results are shown in Fig. 2.

### B. Low-frequency gain

By construction the emitter-follower stage 2 has a voltage gain approaching unity. Tests verified a gain of 0.98 with a load of $24\,\Omega$ and about $5\,\mathrm{Vrms}$ of output voltage. Increasing the

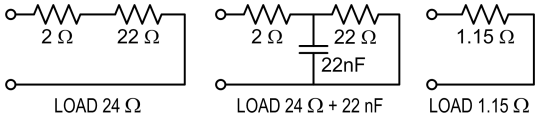



Fig. 3. Three loads used for verification of transient response and high-frequency response.

power absorption with a 21 times lower load resistance value and correspondingly a 21 larger output current, the voltage gain reduces to 0.91, due to various voltage drops along the structure (presently built with a wired through-hole PCB).

Closed-loop operation also compensates for such voltage drops. When closing the loop with stage 1 with an overall gain of 50, the combination of the OPA453 and the output stage 2 achieves a gain of 10 within the accuracy of the two gain resistors ($R_{51} = 2.62\,\mathrm{k\Omega}$ and $R_{52} = 26.2\,\mathrm{k\Omega}$, the latter sized to handle the large output swing with a flowing current of about $1\,\mathrm{mA}$). The OP27 stage was designed with a gain of 5 achieved with $R_{61} = 1\,\mathrm{k\Omega}$ and $R_{62} = 4.99\,\mathrm{k\Omega}$. A measurement using an oscilloscope leaves an uncertainty of about 0.3 % at unitary coverage factor due to the vertical accuracy even after correction. In the present case distortion measurements are relative and concentrated in a few octaves above the fundamental, reducing the error due to lack of flatness.

### C. Stability and transient response

The step response was verified with a test case with a strongly capacitive load (indicated as $24\,\Omega + 22\,\mathrm{nF}$) in Fig. 3.

Tests of the stage 2 alone were carried out by controlling the rise time (RT) of the applied step signal, taking measurements at $10\,\mu\mathrm{s}$, $1\,\mu\mathrm{s}$ and $100\,\mathrm{ns}$, the latter exciting a combination of the stray inductance of the setup and stray capacitance of the output transistors. Results are shown in Fig. 4 for the three different RT values. It is thus of some importance to control the applied RT when using the amplifier for transient signals with capacitive loads, in which case the behaviour is ideal with almost no peaking (visible only at the fastest RT values). As a note, the oscillation in the black curve is due to a wiring problem of the oscilloscope probe ground, but does not pass through the amplifier, as shown by the output response (blue curve). The final stage does not use a connector but soldered wires, that were brought outside for about $15\,\mathrm{cm}$; the oscilloscope probe ground was then connected to the ground terminal of the other probe at the amplifier output, adding another $20\,\mathrm{cm}$, that is the physical distance between input and output sides. As a matter of fact, the oscillation is not visible at the output although it falls well in the operating bandwidth of the amplifier, as it is not a real signal fed to the amplifier.

The tests have been repeated for the complete amplifier including stage 1, reaching an overall gain of 50. Using stage 1 has benefits for gain accuracy and distortion reduction, but introduces unavoidably some phase rotation and chances for instability (due to the deterioration of the open-loop gain curve of the OAs with increasing frequency and the influence of the introduced feedback). It is important thus to test stability and the tests were carried out again at $10\,\mu\mathrm{s}$ and $1\,\mu\mathrm{s}$, with the fast rise-time test limited to $500\,\mathrm{ns}$, to determine the limits of usability in transient conditions.

Test results are shown in Fig. 5, where the input is artificially multiplied by the gain (50), to have better overlapping input and output curves. A slight delay is visible, associated with the OA response.

The behaviour is almost ideal down to $1\,\mu\mathrm{s}$ RT, corresponding to $320\,\mathrm{kHz}$ of equivalent $-3\,\mathrm{dB}$ bandwidth. Tolerable overshoot characterizes the response with a halved RT (at $500\,\mathrm{ns}$) corresponding to $640\,\mathrm{kHz}$ of bandwidth (that was estimated assuming a $B = 1/(\pi t_r)$). A slight oscillation is visible indicating a $2\,\mathrm{MHz}$ dampened resonance.

### D. Distortion

Distortion was evaluated in two different ways, by subjecting the final stage 2 at various loading and bias current levels.

First, the sinusoidal test waveform was provided by a Siglent mod. 6022 waveform generator (WG) that has about $-60\,\mathrm{dBc}$ to $-70\,\mathrm{dBc}$ of spurious free dynamic range depending on the output level, with the second harmonic always showing as the highest one. Input and output signals were measured with a Tektronix mod. MSO2014B, whose additional distortion is not compensated, but is the same for all channels. The test frequencies are $50\,\mathrm{kHz}$, $150\,\mathrm{kHz}$, $250\,\mathrm{kHz}$ and $350\,\mathrm{kHz}$. The harmonics are collected up to order 6 and displayed with correction by subtraction of the WG distortion.

More accurate tests were then carried out cleaning the WG output with a custom designed Chebyshev passive low-pass filter of order 9. The small tolerances and approximations in the values of the passive components led to a frequency response that slightly deviates towards that of an elliptic filter, contributing slightly higher attenuation and steeper response, so about $64\,\mathrm{dB}$ at the 2nd harmonic. A photo and the measured frequency response (as scattering $S$ parameters measured with an Anritsu MS2036C VNA) of the $100\,\mathrm{kHz}$ realisations are shown in Fig. 6.

Results are reported in the following figures. Results for $24\,\Omega$ load and $1.4\,\mathrm{mA}$ diode bias, using subtractionare shown in Fig. 7. The applied voltage was $14\,\mathrm{Vpp}$, corresponding to about $4.7\,\mathrm{Vrms}$, a significant operating point for the amplifier.

Results show juxtaposed the spectral components of the input and output signals and the distance at each harmonic frequency indicates qualitatively the distortion introduced by the amplifier. Numeric results are shown in Table I.

TABLE I. Estimated distortion levels in % with preliminary tests.

| **Freq.** | **Harmonics** | | |
|---|---|---|---|
| **(kHz)** | $2^{\mathbf{nd}}$ | $3^{\mathbf{rd}}$ | $4^{\mathbf{th}}$ |
| 50 | 0.071 | 0.067 | 0.052 |
| 150 | 0.073 | 0.032 | 0.046 |
| 250 | 0.11 | 0.09 | 0.07 |
| 350 | 0.23 | 0.20 | 0.11 |

More accurate tests were repeated using the Chebyshev filter and replacing the oscilloscope with a Picoscope mod. 4424

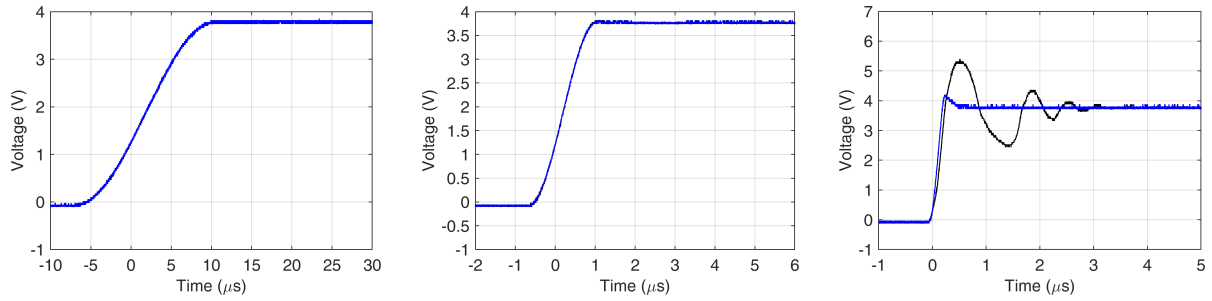



Fig. 4. Step function response for the stage 2 alone with different rise-time values: 10 µs (left), 1 µs (centre), 100 ns (right); input and output signals black and blue, respectively.

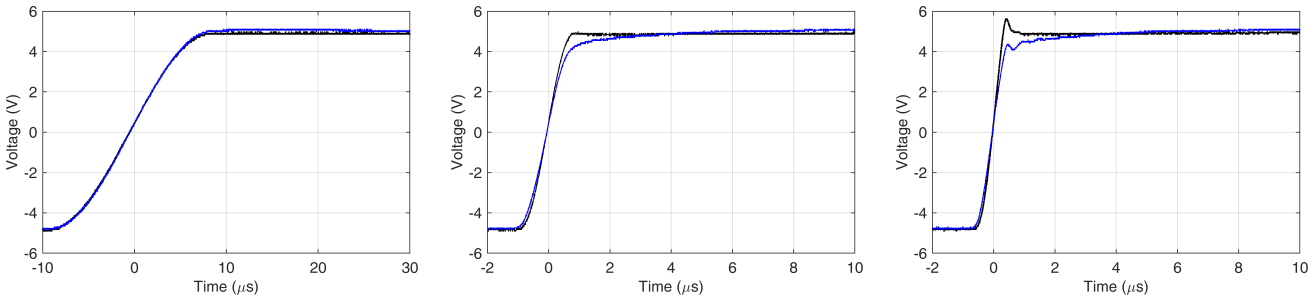
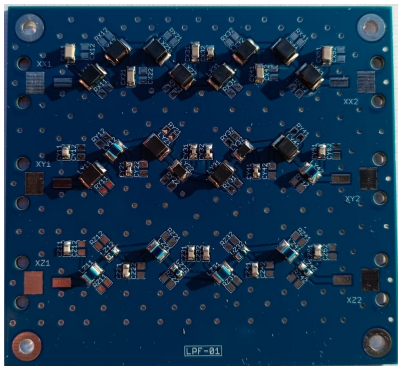
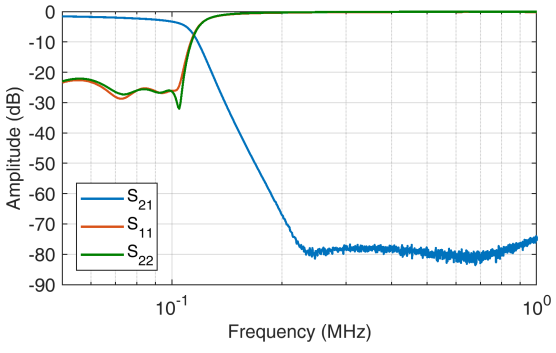



Fig. 5. Step function response for the complete amplifier (cascaded stage 1 and stage 2) with different rise-time values: 10 µs (left), 1 µs (centre), 500 ns (right); input and output signals black and blue, respectively.



(a)




(b)

Fig. 6. Chebyshev 9th order low-pass filter: (a) photo of the PCB, (b) measured S parameters for the 100 kHz version (top channel in photo) used in this work.

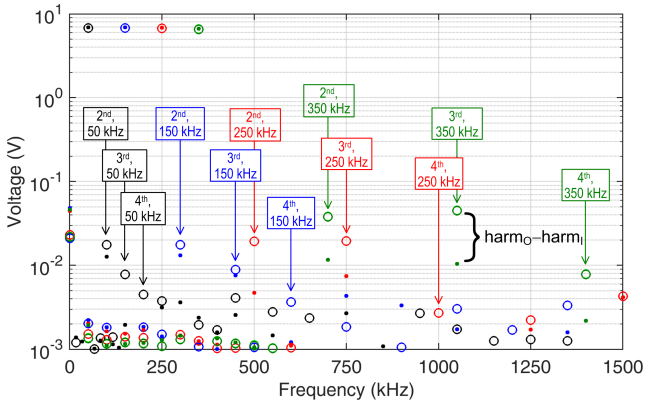



Fig. 7. Distortion tested at 24 Ω load, 1.4 mA diode bias current, and 4.7 Vrms output voltage) for the four test frequencies (black 50 kHz, blue 150 kHz, red 250 kHz and green 350 kHz), using a frequency resolution of 1/3 of the fundamental. Dot and circle indicate input and output spectrum.

[19]. The results for a test carried out at 100 kHz (available in the implemented filter) are shown in Fig. 8. The resulting largest harmonic is the 2nd at 0.079 %.

Considering that at this development phase the tests were carried out on the output power stage 2 alone, the observed low distortion is particularly remarkable. It is indeed a performance that is better than a top-of-range amplifier, like the Clarke Hess mod. 8210 and 8220 transconductance amplifiers [20], a commonly used equipment by research and metrological institutes [9]. The manufacturer [20] in fact reports −60 dB of THD up to 20 kHz and −40 dB of THD up to 100 kHz,

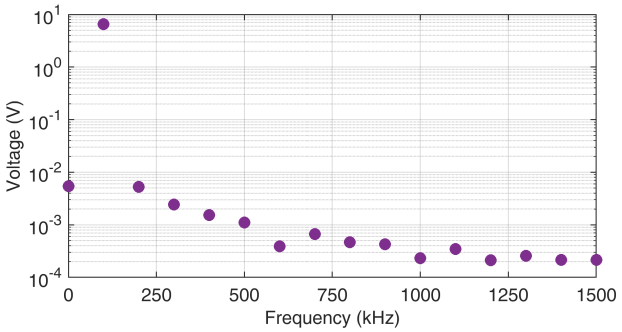



Fig. 8. Distortion for $24\,\Omega$ load, $1.4\,\mathrm{mA}$ diode bias current and $4.55\,\mathrm{Vrms}$ output voltage at $100\,\mathrm{kHz}$ measured using cleaned WG signal and 12-bit Picoscope oscilloscope.

whereas figures in Table I amount to better than $-60\,\mathrm{dB}$ up to $150\,\mathrm{kHz}$. In addition, the voltage compliance of the Clarke Hess of $7\,\mathrm{V}$ is more or less in line with the maximum output voltage swing of the presented prototype of $20\,\mathrm{Vpk}$.

Some tests were repeated for the complete amplifier, bringing the waveform generator to a lower distortion thanks to the required lower output voltage amplitude thanks to the introduced gain of 50. The introduced feedback is expected to provide reduction of distortion that cannot be presently estimated by subtraction: a low-pass filter with steep roll-off is currently designed for a clean undistorted sinusoidal signal.

## IV. Conclusions

The design principles have been discussed for a low-distortion amplifier able to cover the frequency range for the IT experimental verification up to $150\,\mathrm{kHz}$, and possibly up to $500\,\mathrm{kHz}$, after careful verification of the prototype and necessary adjustments.

The amplifier is composed of a very linear class-AB output stage able to source a maximum $\pm 20\,\mathrm{Vpk}$ with a $\pm 15\,\mathrm{Apk}$ current in the present implementation, that allows larger current is possible for limited amounts of time, limited only by internal dissipation. Larger output voltage is possible up to about $\pm 40\,\mathrm{Vpk}$.

Tests have been carried out at $\pm 6.7\,\mathrm{Vpk}$ and $\pm 5.8\,\mathrm{Apk}$ due to limitations of the available power supply.

Bandwidth verification was carried out not only by measuring the amplitude response (almost flat up to $1\,\mathrm{MHz}$), but evaluating distortion, that resulted in $< 0.1\,\%$ up to about $150\,\mathrm{kHz}$. The transient response to a step voltage signal also indicates good stability and very fast rise time, following the input signal without appreciable delay and limited overshoot down to $500\,\mathrm{ns}$ (a $-3\,\mathrm{dB}$ bandwidth of $640\,\mathrm{kHz}$).

Future development is the demonstration of the scalability to larger current by paralleling more output stages, including the driver stage with the 2SC4793 and 2SA1837 transistor pair. The increase of the output voltage is limited by two factors: the maximum output voltage of the power OA stage (presently implemented with an OPA 453) and the SOA of the output transistors. By simply scaling in current, the limited output voltage is compensated by means of an output transformer. In addition, the overall distortion can be slightly improved by optimizing the parameters and operating points, possibly keeping it below $0.1\,\%$ consistently.

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