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Full Length Article

An integrated housing with active cooling for Silicon Photomultipliers arrays in next generation of Ring Imaging Cherenkov detectors☆

M. Arvelos, R. Cardinale *, S. Ghizzo, M. Negri, A. Petrolini, S. Minutoli, S. Pezzulo, R. Puppo, C. Rossi, A. Sergi, F. Silenzi, E. Spadaro Norella

University of Genova and INFN, Via Dodecaneso 33, Genova, I-16146, Italy

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ABSTRACT

Silicon Photomultipliers (SiPMs) are increasingly considered as a baseline photon-detection technology for next-generation Ring Imaging Cherenkov detectors (RICH); however, single-photon RICH applications require an effective reduction of the dark count rate, especially after irradiation. An integrated and compact housing module for SiPM arrays is presented, in which mechanical support, compatibility with front-end readout, and active local cooling are combined within a modular and scalable architecture. The concept is derived from the Elementary Cell approach developed for the LHCb RICH Upgrade and is extended by embedding thermal management at the photosensor level. Several cooling strategies are under evaluation, with emphasis on multilayer ceramic substrates incorporating internal fluidic channels. Thermal modeling and prototype measurements indicate stable operation and good temperature uniformity of the cooled structure at temperatures well below 0,° C reaching the −80 °C range in dedicated tests. The proposed approach provides a path toward low-noise, high-density SiPM-based photodetector modules suitable for next-generation, large-area, scalable RICH detectors.

1. Introduction

Future collider experiments (such as those at the EIC [1], HL-LHC [2], FCC-ee/hh [3], and other colliders) require RICH detectors providing excellent charged-hadron separation over a broad momentum range. At the same time, operation in high-rate and potentially high-radiation environments, together with the need to instrument large surfaces with high granularity, drive increasingly stringent requirements on the photon-detection system, in terms of both performance and system-level scalability. In particular, next-generation photodetectors are required to deliver high single-photon detection efficiency in the near-UV/visible range, fine spatial granularity (typical pixel sizes down to 0.5 mm to 2 mm), and single-photon timing at the 100 ps level or better. Radiation tolerance compatible with HL-LHC-like conditions, up to about 3×10^{13} n_{eq}/cm^2, and the control of random and correlated noise sources are additional key constraints.

Silicon Photomultipliers (SiPMs) [4] satisfy many of these requirements and are therefore widely considered as a baseline option for future RICH systems, thanks to their high photon-detection efficiency, compactness, magnetic-field insensitivity, and potential for excellent timing with mm-scale segmentation. The dominant limitations are associated with dark count and correlated noise (afterpulsing and optical crosstalk) rates at ambient temperature, which are relevant for single-photon RICH applications, and are exacerbated by irradiation. Mitigation strategies include device-level R&D on SiPM technology (e.g. microcell design, trenching, and fabrication parameters), timing-based rejection of random background, shielding where feasible, and annealing approaches using controlled thermal cycles to partially recover radiation-induced damage, either during dedicated shutdown periods or, where feasible, in situ. Among these, operation at reduced temperature provides a direct and effective means to suppress thermally driven noise and to maintain the required detector performance under harsh operating conditions.

In this context, the development is presented of a compact and modular SiPM housing that integrates active local cooling at the photosensor level, while preserving a large optical fill factor and a scalable mechanical/readout interface suitable for large-area tiling. The proposed approach aims at achieving stable operation at temperatures of several tens of degrees below zero centigrade without imposing stringent cryogenic-temperature constraints on the design, thereby enabling a practical and extensible path toward low-noise, high-density photodetector planes for next-generation RICH detectors.

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* Corresponding author at: University of Genova and INFN, Via Dodecaneso 33, Genova, I-16146, Italy.
E-mail address: roberta.cardinale@ge.infn.it (R. Cardinale).

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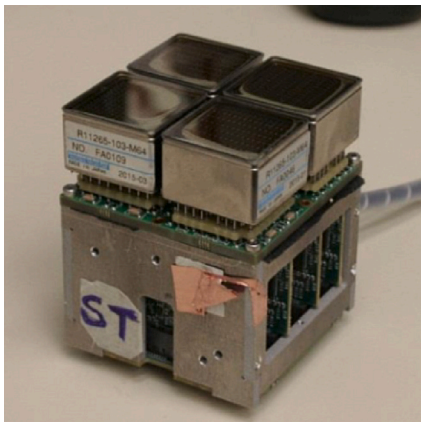

Fig. 1. The Elementary Cell (EC) developed for the LHCb RICH Upgrade I.

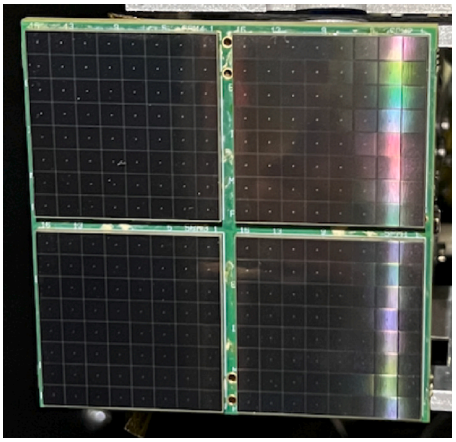

Fig. 2. BaseBoard v1 SiPM/MPPC housing PCB prototype.

2. Modular concept and SiPM housing development

A modular approach is adopted, inspired by the tiling philosophy of existing RICH photodetector units, such as the Elementary Cell developed for the LHCb RICH Upgrade I [5] to house multi-anode photomultipliers [6] shown in Fig. 1 and the dRICH developments for the ePIC detector at the EIC [7]. A first SiPM/MPPC housing PCB prototype, referred to as BaseBoard v1 (BBv1), was designed and tested. The board, as shown in Fig. 2, hosts four SiPM matrices, each consisting of an 8×8 pixel array with 3 mm pixel size in LGA packaging (Hamamatsu S13361-3050NE-08). The main challenge of this first generation is the achievement of a high geometric fill factor, both within the BaseBoard and between adjacent baseboards. BBv1 has been validated in laboratory, using an analog readout chain and has been also operated in testbeam at CERN [8].

2.1. Integrated housing with active cooling

The second prototype generation (BBv2) integrates active cooling into the sensor housing, targeting SiPM operating temperatures down to the −80 °C to −60 °C range. The adopted strategy is based on maintaining the photosensors at sub-zero temperature while thermally decoupling them from the front-end electronics, thereby reducing the need for electronics qualification at low temperature and limiting the overall cooling power. Several cooling technologies can in principle be considered, including fluid micro-channels and miniature cryo-coolers. Among the available technological options, the present development focuses on a simple coolant-fluid approach, integrated in the sensor support.

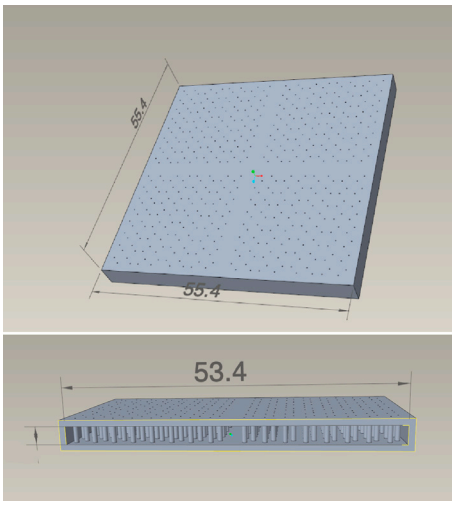

Fig. 3. BBv2 concept based on a hollow ceramic PCB with embedded cooling channels. Top: drawing of the ceramic substrate showing the top surface and the footprint for the placement of four SiPM matrices. Bottom: cross-section of the structure illustrating internal coolant routing and via/pillar signal connections for high-density readout integration.

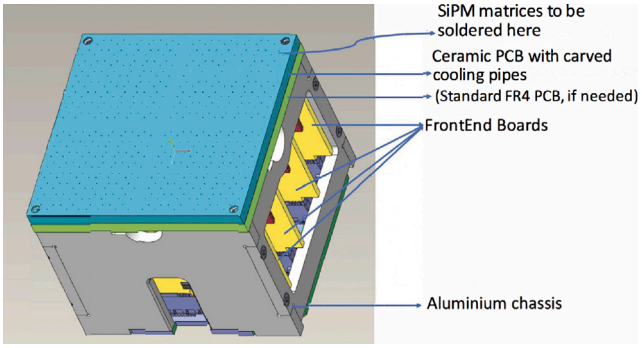

Fig. 4. SiPM-based Elementary Cell prototype: layout of the photodetector modular unit integrating SiPM matrices with the mechanical housing and the readout interface.

3. Ceramic substrate with embedded cooling channels

The second-generation concept (BBv2) is based on a hollow ceramic PCB that allows coolant circulation directly through the board (Fig. 3).

The design was developed to combine embedded thermal management with high-density electrical routing in a compact, tileable format. The current layout has a footprint of about 2×2 in^2 and a thickness of approximately 3 mm, and it can host four 8×8 SiPM matrices with 3 mm pixel size. Electrical routing is implemented with through-hole vias that bring anode and cathode signals across the ceramic layer within the supporting pillar structures. This architecture minimizes analog connection path lengths to the front-end electronics, thereby preserving signal integrity and supporting excellent timing.

In the current concept, the SiPM matrices are directly soldered onto metallized pads on the ceramic PCB. An additional PCB can be added to provide thermal insulation and mechanical stability, and to reroute signals to connector pins where the front-end boards with ASICs are attached (see Fig. 4).

In order to mitigate issues related to mismatched coefficients of thermal expansion between ceramic and standard PCB materials, the rerouting can alternatively be implemented within additional metallized ceramic layers.

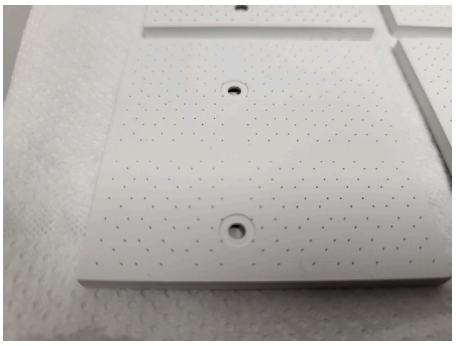

Fig. 5. 3D-printed AlN ceramic prototypes.

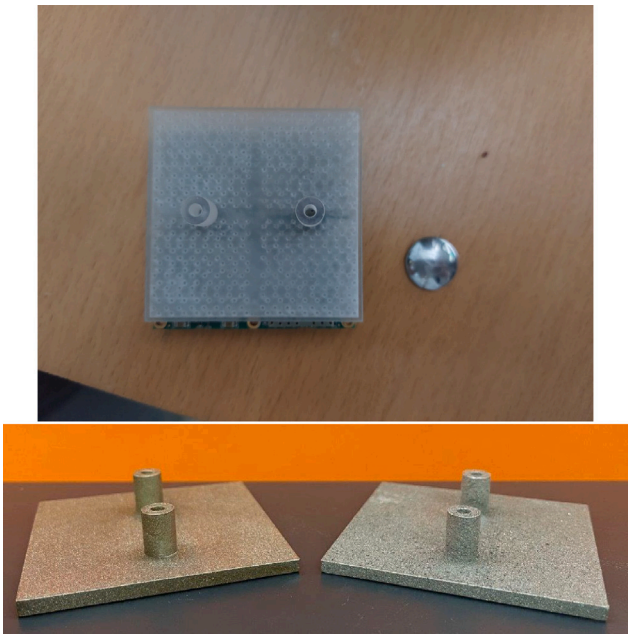

Fig. 6. 3D-printed plastic (top) and metallic (bottom) mock-ups used to validate and commission the internal cooling layout prior to ceramic production.

3.1. Ceramic prototypes and production status

Collaborations with multiple companies have been established to address the production of ceramic PCBs and the associated metallization processes. First 3D-printed aluminium nitride (AlN) ceramic prototypes, without metallized vias, have been ordered and produced (see Fig. 5).

In parallel, dedicated R&D is ongoing to define the constraints for through-hole via metallization, including the minimum viable diameter-to-length (aspect) ratio. Test coupons with increased via diameters of have been produced for metallization studies.

Once the ceramic samples are verified for conformity, metallization will be performed and followed by electrical validation, including signal-integrity measurements. In parallel, thermal and fluid-dynamics simulations are planned to validate and optimize the design, including the overall thickness as well as the number and positioning of coolant inlets and outlets under mechanical and space constraints. Ceramic-prototype validation in beam tests is foreseen this year within the DRD4 Collaboration, using a full module read-out by front-end boards developed for the ePIC dRICH [9] and equipped with the ALCOR ASIC [10].

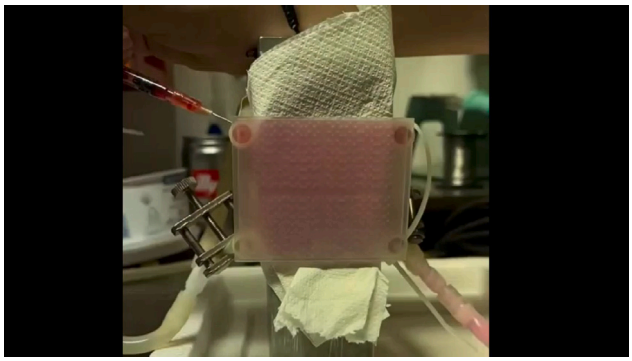

Fig. 7. Coolant circulation test in a 3D-printed plastic mock-up. The flow was visualized using colored water to identify potential regions with reduced or absent coolant flow.

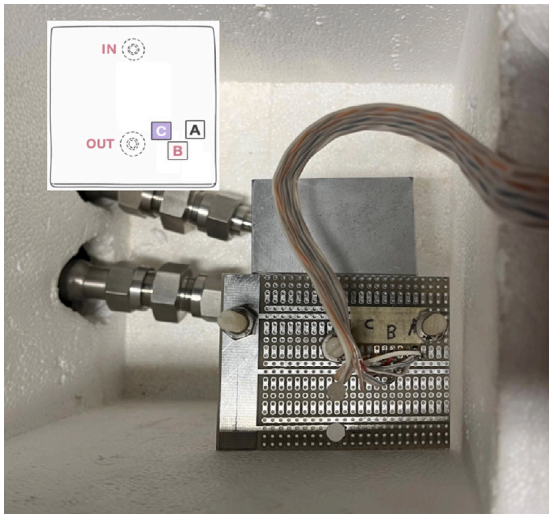

Fig. 8. Low-temperature test configuration operated inside a polystyrene enclosure and flushed with dry air to mitigate condensation during coolant circulation. The labels A, B, and C indicate the positions of the three PT1000 sensors used to monitor the mock-up surface temperature.

4. Mock-ups studies and thermal performance

Thermal tests on 3D-printed plastic and metallic mock-ups (see Fig. 6) were carried out to commission the cooling layout ahead of ceramic production, with emphasis on coolant circulation and thermal performance.

4.1. Plastic mock-ups: circulation and first thermal checks

Several 3D-printed plastic mock-ups reproducing the internal channel geometry were used to validate coolant circulation. Qualitative tests with colored water confirmed continuous flow throughout the full mock-up volume (see Fig. 7). First thermal checks were performed using water at approximately 12 °C and a thermal camera, indicating an overall uniform temperature distribution. As expected, corner regions were identified as the most critical areas and were therefore flagged for further layout optimization.

4.2. Metallic mock-ups and low-temperature setup

Two metallic mock-ups with the same size and internal design as the ceramic PCB were produced: one in aluminium and one in stainless steel 316L, with machined and polished surfaces. Most measurements

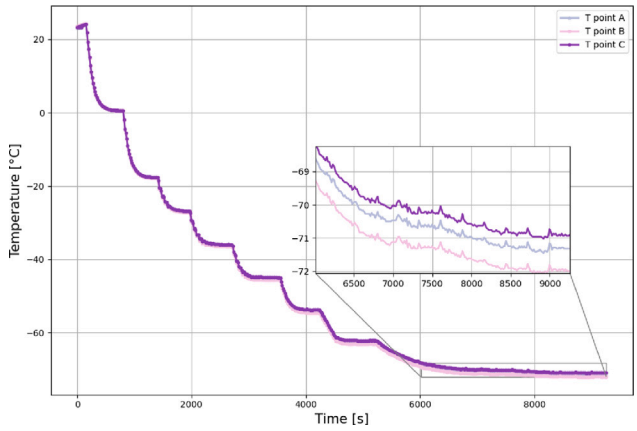

Fig. 9. Temperature evolution as a function of time measured at three different points of the aluminium mock-up (A, B, C) during the cooling cycle. The plot shows the decrease in temperature down to around −70 °C. The inset highlights the final part of the cooling process, where only small temperature differences among the three measurement points are visible.

were performed with the aluminium mock-up, selected because its thermal conductivity is closer to that of AlN. Low-temperature tests were carried out using a recirculating chiller and silicone oil, reaching coolant temperatures down to −80 °C. The setup was operated inside a polystyrene enclosure and flushed with dry air to mitigate condensation (Fig. 8). The temperature of the mock-up surface was monitored with three PT1000 sensors placed at different positions (Fig. 8).

A good temperature uniformity was observed across the monitored points. The maximum temperature difference between sensor locations was found to be $\lesssim 0.7$ °C in the lowest-temperature runs as shown in Fig. 9.

Complementary thermal-camera measurements performed at higher temperatures confirmed the uniformity, with maximum temperature differences $\lesssim 2$ °C.

These results validate the internal cooling-channel concept and motivate the next step, based on metallized ceramic prototypes and fully integrated readout.

5. Conclusions

An R&D program toward an SiPM photodetector housing module integrating active local cooling in the sensor housing for the next generation of RICH detectors has been presented. A new BaseBoard design based on a hollow ceramic PCB with internal coolant circulation and via-based signal routing has been developed. Plastic and metallic mock-ups were used to validate coolant circulation and thermal performance, demonstrating good temperature uniformity down to −80 °C. First AlN ceramic prototypes have been produced; metallization and signal-integrity tests constitute the next milestones. A testbeam validation of a full prototype module, read out by front-end boards equipped with the ALCOR ASIC, is foreseen in 2025 within the DRD4 framework [11]. Further developments are ongoing toward a new version with reduced pixel size down to 2 mm × 2 mm, enabling improved granularity for future RICH applications.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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