



**Università
di Genova**

Polytechnic School

DITEN - Electrical, Electronics and Telecommunication
Engineering and Naval Architecture Department

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and Complex Systems for Mobility

**Optimization-Based Power Control of CHB EV
Charging Station with integrated BES**

Supervisors:

Prof. Andrea Formentini

Prof. Mario Marchesoni

Author:

Muhammad Azhar Ghauri

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To my family, especially my parents, whose support made my achievements possible.

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Abstract

Environmental concerns and the increasing adoption of electric vehicles (EVs) are driving the need for extreme fast-charging (XFC) stations capable of delivering high power in short time intervals. However, such infrastructures impose significant stress on the power grid. Traditional low-voltage (LV) charging systems struggle to meet ultra-high-power requirements due to excessive current demands and limited scalability. To address these challenges, medium-voltage (MV) multiport architectures based on cascaded H-bridge (CHB) converters have emerged as a promising solution. Although such architectures offer high power capability and improved power quality, maintaining power balance among multiple charging ports while ensuring stable operation remains a critical challenge.

A cascaded H-bridge (CHB)-based multiport architecture integrated with distributed battery energy storage (BES) modules is considered a promising solution for extreme-fast charging stations for electric vehicles. It not only enables high-power EV charging but also mitigates power imbalance among charging ports. However, the BES modules in this architecture undergo frequent high-power charge–discharge cycles to compensate for dynamic load variations, thereby accelerating battery degradation and reducing system lifetime.

To address this issue, an optimized control framework is proposed for the integrated BES modules to reduce battery stress while ensuring fast convergence of state of charge (SoC) across all distributed units. The proposed optimization-based BES power management strategy is based on the intrinsic power-imbalance limits of the CHB rectifier submodules. These limits are analytically derived as a function of the total duty cycle and subsequently incorporated as constraints in a quadratic optimization problem. The objective is to minimize BES power utilization by using the BES module's battery power only when necessary, while maintaining the SoC of all modules close to their reference values.

The effectiveness of the proposed control strategy is validated through detailed MATLAB/Simulink simulations under highly dynamic EV charging scenarios, including random arrival and departure of vehicles with varying power demands. Furthermore, the

proposed approach is experimentally verified on a laboratory-scale prototype, demonstrating agreement with simulation results. Both simulation and experimental findings confirm that the proposed method successfully maintains CHB operation within the feasible region, ensures stable DC-link voltage balancing, and significantly reduces unnecessary BES power cycling while achieving reliable SoC regulation.

Abbreviations

AC	<i>Alternating Current</i>
DC	<i>Direct Current</i>
EV	<i>Electric vehicle</i>
ICEVs	<i>Internal-combustion engine vehicles</i>
EVs	<i>Electric vehicles</i>
MV	<i>Medium voltage</i>
AfE	<i>Active front-end</i>
BES	<i>Battery energy storage</i>
CHB	<i>Cascaded H-bridge</i>
DAB	<i>Dual active bridge</i>
XFC	<i>Extreme fast charging</i>
SoC	<i>State of charge</i>
GHG	<i>Greenhouse gas</i>
PFC	<i>Power factor correction</i>
ESSs	<i>Energy storage systems</i>
MV/LV	<i>Medium-voltage / low-voltage</i>
RESs	<i>Renewable energy sources</i>
XFCS	<i>Extreme fast charging station</i>
PWM	<i>Pulse-width modulation</i>
QP	<i>Quadratic programming</i>
RTI	<i>Real-time interface</i>
PLL	<i>Phase-locked loop</i>
LPF	<i>Low-pass filter</i>
PEV	<i>EV-load power notation</i>

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Chapter 1:

Introduction

1.1 Background and Motivation

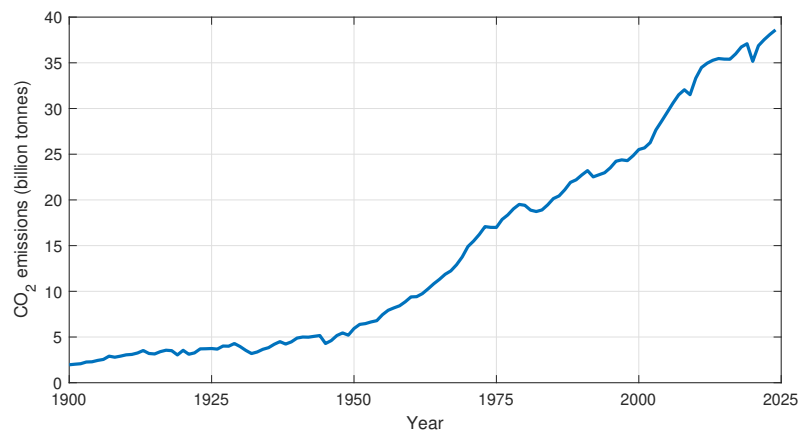
Increasing environmental awareness has strengthened the decarbonization and implementation of sustainable technologies. The negative effects of fossil fuel CO_2 emissions have triggered a shift in the world toward adopting renewable energy and extensive electrification of the industries. This change is an indicator of mounting pressure to reduce greenhouse gas levels and curb climatic change [1, 2, 3].

In 2025, it is estimated that the CO_2 emissions by fossil fuels will reach a record of 38.1 billion tonnes, and the long-term trend of increasing CO_2 emissions continues. Despite this expansion, the use of clean energy, particularly solar power, has already reduced major fossil fuel creation; even the solar energy prevented the emission of about 1.66 billion tonnes CO_2 in 2024 by itself [4, 5].

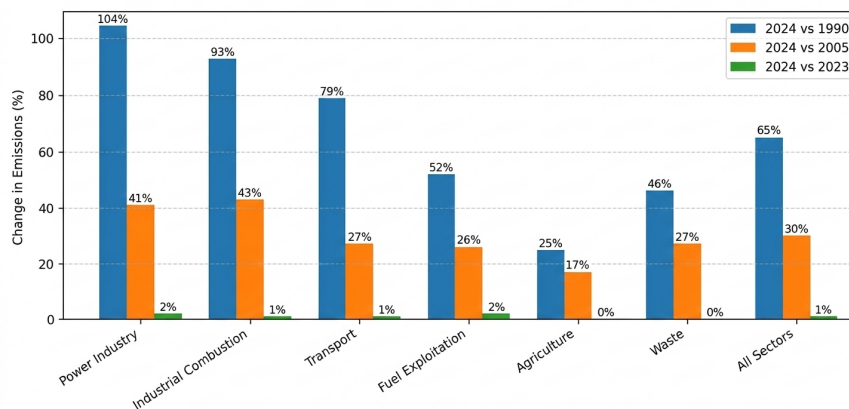
Figure 1.1b shows the sector-level contribution of CO_2 emissions. Notably, the transportation sector accounted for around 27% of total global energy-related CO_2 emissions, consequently making a substantial contribution to global greenhouse gas output and ranked as one of the most carbon-intensive end-use sectors [6]. As a result, decarbonizing transport has emerged as a key objective in national and supranational climate policies.

Consequently, internal-combustion engine cars (ICEVs) are gradually being phased out due to their inability to meet higher and higher standards of emissions. The emergence of electric vehicles (EVs) powered by renewable electricity has made them a viable alternative to conventional ICEVs. They have significant potential to reduce fossil-fuel reliance and greenhouse-gas emissions by exploiting various low-carbon energy sources. The rapid adoption of EVs is driven by several key benefits, including the absence of tailpipe emissions, reduced maintenance and ownership costs, the ability to

charge with locally produced renewable energy, and significantly lower noise levels.



(a) Global CO₂ emissions over time



(b) CO₂ Emission by sector

Figure 1.1: Global CO₂ emissions trends and sectoral breakdown

Over 20 million EVs were sold globally by 2025, accounting for over 25% of all new passenger cars sold. This indicates that despite a shifting market, electric transportation is being adopted strongly and consistently. This significant achievement comes after 2024, when electric vehicles accounted for almost 22% of all new car sales, demonstrating the rapid growth of battery-electric vehicles (BEVs) and plug-in hybrid electric vehicles (PHEVs) in recent years [7, 8]. Notwithstanding the influence of economic and policy factors on demand, these figures demonstrate a high level of market penetration and a rapidly increasing contribution of electrification to reducing emissions in the transportation sector.

In spite of the impressive progress, there are a number of enduring obstacles hindering the adoption of EV. The initial purchase prices, compared to ICEVs, sustained range anxiety (typically 250-500 kilometers), extended recharge times (typically more than 30



Figure 1.2: Extreme Fast Charging Station

minutes to fully charge), and a relatively sparse public charging network all discourage potential customers [9]. The reduction of these obstacles requires continued advances in battery technology, such as lower prices, improved energy densities, faster charging speeds, and longer cycle times, as well as the massive and coordinated development of fast-charging networks to keep up with demand cite 10, 11. In response to these challenges, medium voltage (MV) grid connected fast and extreme fast-charging infrastructures have emerged as a key enabler for large-scale EV adoption.

The emergence of DC fast-charging infrastructure has greatly enhanced the feasibility of electric cars by substantially decreasing charging duration. Recent DC fast chargers generally operate at 50-350 kW, enabling rapid recharging of electric vehicle batteries and enhancing the practicality of long-distance driving. A 350 kW ultra-fast charger can replenish a 60 kWh battery to over 90% state of charge in around 10 minutes, approaching the refueling experience of traditional gasoline cars. This capacity signifies significant technical progress in alleviating range anxiety and enhancing the overall user experience of electric vehicles [10].

High-power DC charging stations not only reduce charging time but also enable the deployment of extreme fast charging stations (XFCs), which aggregate multiple charging modules to accommodate several cars simultaneously. These stations are often constructed with modular power electronic designs that provide expandable power ratings and adaptable system operation. Integrating many chargers into a single station enables the infrastructure to accommodate high-power charging requirements while en-

hancing energy management and power distribution. Thus, DC fast-charging networks are essential to facilitating the extensive electrification of transportation by providing the rapid, convenient charging necessary for broad electric vehicle adoption.

However, even though MV grid-connected DC fast chargers substantially reduce car charging time, they inevitably impose heavy electrical and operational loads on the grid and local storage resources. In this context, this dissertation explores the control issues posed by the multi-port modular MV-DC extreme fast-charging station presented in [11].

1.2 Overview of Extreme Fast Charging Station

Figure 1.3 illustrates the architecture of the medium voltage extreme fast charging (XFC) station investigated in this thesis. The suggested architecture is split into three distinct stages: the first stage comprises an AC-DC conversion stage featuring a multi-level cascaded H-bridge (CHB) converter that functions as an active front-end rectifier (AFE). The multilevel converter facilitates operation at medium voltage while employing traditional low-voltage semiconductor devices at the module level. This modular construction improves fault tolerance, reduces filter requirements, and enhances the quality of grid-supplied power.

The 2nd stage is the distributed energy buffering stage, realized through split battery energy storage (BES) modules integrated directly within each converter module. Each BES module can absorb or deliver power individually. This distributed arrangement provides dynamic buffering capability, which reduces instantaneous demand on the MV grid—a key advantage in extreme fast-charging scenarios where multi-vehicle loads fluctuate rapidly.

The 3rd and final stage, also called the isolation stage, which consists of a dual active bridge (DAB), provides galvanic isolation, voltage conversion, and current control for EV charging ports while meeting safety and compatibility requirements across diverse battery pack voltages. The modular stacking of CHB cells, combined with the DC isolation and control flexibility of the DAB, enables scalability from single-port to multi-port charging, allowing charging station operators to adapt to different deployment scales and power ratings cite 13.

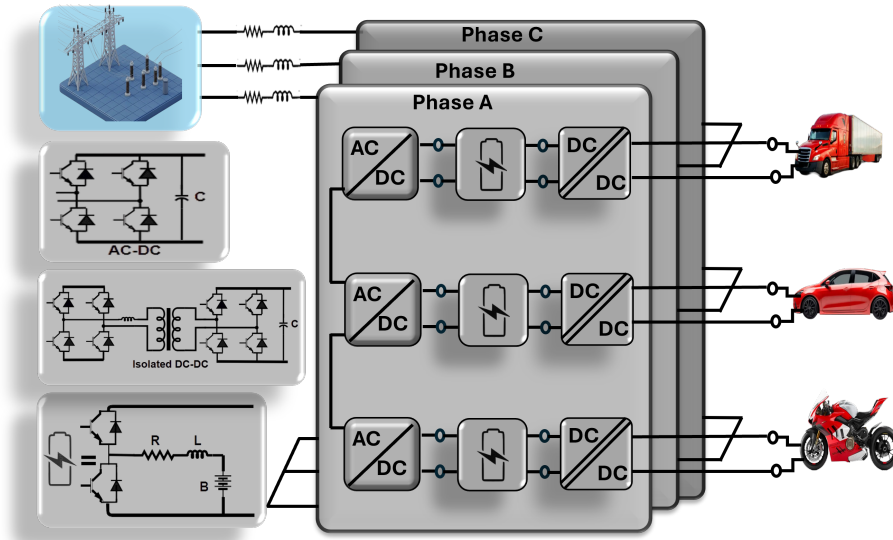


Figure 1.3: CHB With Integrated BES Extreme Fast Charging Station

While the presented architecture delivers transformerless MV interfacing, per-cell flexibility, and embedded energy buffering that mitigate grid stress, it also introduces new operational challenges: distributed BES modules can be subject to excessive cycling, which accelerates aging, and control operations can lead to DC-link voltage imbalance. To maximize the efficiency and adoptability of the presented architecture, it is essential to design a sophisticated control strategy that prevents the rapid degradation of BES module batteries without destabilizing the DC-link voltages.

1.3 Problem Statement

Although the XFC station architecture presented in Figure 1.3 minimizes instantaneous power consumption at the grid, it has an inherent operational limitation. Theoretically, individual cells in a CHB rectifier can handle various power levels within the converter's internal power bounds. However, the control strategy outlined in [11] enforces uniform active power allocation across all CHB modules. This forces every BES unit that serves as a power buffer to either supply or absorb a significant amount of active power. This homogeneous loading of the CHB converter cell consequently subjects all BES modules to excessive and unnecessary cycling, which accelerates degradation and shortens their lifespan.

Moreover, regulating only the average power of the CHB converter effectively restricts

all series-connected cells to function at a uniform operating point. The implicit equal-power limitation considerably restricts the intrinsic flexibility of the multilevel converter architecture. Therefore, an advanced control strategy is needed to alleviate this equal-power constraint and to utilize the BES module only when required. The control strategy should avoid unnecessary battery cycling while ensuring optimal converter functionality and uninterrupted power exchange.

1.4 Research Questions

This thesis examines the subsequent research questions arising from the challenges identified in the cascaded H-bridge (CHB) extreme fast-charging (XFC) station integrated with a distributed battery energy storage (BES) module:

- *What are the intrinsic operational limitations of the CHB converter that ensure steady DC-link voltages and feasible power transfer to the grid, especially during dynamic EV charging scenarios?*
- *How can we reduce BES module utilization while maintaining the DC_link voltage at its reference value and ensuring that CHB converter operation remains within its admissible operating region?*
- *How can the convergence of the BES module's state of Charge (SoC) to a fixed pre-determined reference be accomplished?*
- *To what extent can the developed control method be scaled to accommodate more CHB cells in modular XFC stations?*

1.5 Research Contributions

This thesis provides the following principal contributions to meet the research objectives outlined in the previous investigations:

- **Derivation of CHB operational limits:** *The inherent power limits of the CHB converter, which ensure DC-link voltage stability and feasible converter operation, are derived analytically.*

- **Formulation of power constraints:** *Power constraints are formulated by converting the obtained DC-link voltage balancing limits into power constraints for XFC stations.*
- **BES power optimization strategy:** *To minimize BES module stress and prevent rapid degradation, an optimal control strategy is designed to ensure that only the minimum necessary power references are generated for BES modules when required.*
- **Simulation-based validation under practical XFC scenarios:** *The proposed control strategy is validated through extensive MATLAB/Simulink simulations that illustrate a hypothetical XFC station profile, demonstrating stable operation of the CHB converter and reduced utilization of BES modules.*

1.6 Dissertation Outline

The dissertation consists of six chapters, followed by a concluding chapter, which are summarized as follows:

Chapter 2 examines the available literature on extreme fast charging (XFC) for EVs, focusing specifically on charging topologies and power conversion solutions. It analyzes the constraints of existing fast-charging methods and evaluates both AC- and DC-bus-based XFC station designs. An overview of various multilevel AC–DC converter architectures is presented, along with a critical examination of DC-link voltage balancing and modulation schemes for cascaded H-bridge converters. This chapter identifies the research gaps that drive the control and optimization strategies formulated in the following chapters.

Chapter 3 delineates the architecture of a multilevel cascaded H-bridge converter and provides the mathematical models employed for analysis and control. The model includes the CHB rectifier, transformation of the reference frame, and a control-oriented representation of AC-side dynamics and DC-link voltage characteristics. The battery energy storage (BES) module is modeled to reflect its interaction with the converter system, establishing the basis for future control design.

Chapter 4 emphasizes the optimal management of the CHB converter integrated with

a battery energy storage system (BES) module. It outlines the steady-state operating conditions and nonlinear properties of the averaged model, and then addresses linearization and operating-point analysis. The control design for the CHB-AFE system is developed, incorporating voltage-oriented control that includes inner current regulation, as well as average DC-link voltage regulation. Furthermore, constraints for balancing the DC-link voltage are established, and an effective optimal control strategy for the BES module is formulated to guarantee stable operation while minimizing battery usage.

Chapter 5 *presents the simulation and experimental findings employed to assess the effectiveness of the proposed control strategy. Hypothetical extreme fast-charging scenarios are implemented to evaluate DC-link voltage management, state-of-charge balancing behavior, and battery energy storage utilization compared with traditional methods.*

Chapter 6 *concludes the thesis by summarizing the most important results, outlining practical implications, and addressing future research directions.*

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Chapter 2:

Literature Review

2.1 Introduction

The state of the art relevant to this research is reviewed in this chapter. After providing an overview of electric car chargers and associated standards, it goes on to discuss power conversion topologies suitable for fast and extreme-fast charging.

The review begins with two-level voltage source converters and the challenges they encounter when connecting to a medium-voltage grid. After that, it moves to multilevel converter architectures, such as cascaded H-bridge (CHB), neutral-point-clamped, and flying-capacitor converters, emphasizing the benefits of the CHB structure and its applicability for transformer-less medium-voltage operation. Moreover, this chapter examines DC-link voltage-balancing methods and control strategies for CHB converters. The strengths and weaknesses of existing approaches are evaluated critically to assess how well they perform in real-world operational scenarios with fluctuating power demands.

The currently available MV-XFC station architectures are also thoroughly examined in this chapter, with an emphasis on both their advantages and disadvantages. A summary of the results and a clear identification of research gaps are included in the chapter's conclusion.

2.2 Electrical Vehicle Fast Charging

An electric vehicle (EV) charging station is a grid-connected piece of equipment located in home garages, commercial buildings, roadside locations, and public parking spaces. EV charging systems can be classified into AC and DC types, which are further subclassified into three levels based on charging power: Level 1 (L1), Level 2 (L2), and Level 3 (L3) [1]. Level 1 (L1) chargers are the slowest charging option, commonly used

in residential areas for overnight charging; they operate at 120V AC and have a maximum output of 1.9 kW. Level 2 (L2) chargers are frequently installed in businesses and public parking areas, operate at 208–240V AC, and deliver charging capacities of up to approximately 20 kW [2]. Although L1 and L2 chargers work well with long dwell times, they have low power ratings which extend the charging duration to a few hours, limiting their applicability in long-distance travel and high-load situations [3, 4].

In spite of, AC Level 3 chargers (≈ 480 V, ≥ 50 kW) have been proposed to address the issues presented by L1 and L2 chargers, their implementation is still restricted in comparison to DC fast charging because of efficiency issues and the additional infrastructure, needed for high-power AC delivery [5, 6].

L3 DC fast chargers mitigate these constraints by bypassing the on-board charger and delivering high power directly to the car battery, typically providing 50–300 kW at DC output voltages between approximately 300V and 600V. Due to their substantial power levels, L3 chargers are designed as off-board, stationary devices that can provide considerable state-of-charge improvements within 20 to 30 minutes [6, 7]. Table 2.1 delineates the comprehensive charging standards and classifications by power level.

Table 2.1: Charging types and levels

Charging type	Level	Charger location		Time to recharge 60 kWh (h)	Specifications		
		On-board	Off-board		Voltage (V)	Current (A)	Power (kW)
SAE AC charging standards							
AC	Level 1	✓	–	7–17	120	12–16	≤1.92
	Level 2	✓	–	0.4–1.2	240	80	1.92–19.2
	Level 3	–	✓	0.5–1	480	≥100	≥50
SAE DC charging standards							
DC	Level 1	–	✓	0.4–1.2	200–450	80	36
	Level 2	–	✓	0.2–0.4	200–600	200	90
	Level 3	–	✓	0.2	200–600	400	240

Despite Level 3 AC fast charging substantially reducing charging time compared with Level 1 and Level 2 solutions, the overall time required to charge an EV remains a considerable obstacle to EV proliferation. Even with the state-of-the-art DC fast chargers with a power range of 50 kW to 150 kW, it usually takes 20–40 minutes to get a significant increase in the state-of-charge of the EV battery, which is significantly longer than the amount of time needed to refuel a conventional ICEV [7, 8]. Consequently, additional

reductions in charge duration—aiming for approximately 10 minutes—are widely recognized as crucial for mitigating user inconvenience and alleviating ongoing concerns about charging time and range anxiety.

Simultaneously, a driving range of 350km was once considered adequate, but nowadays most EV models come with larger battery packs capable of traveling 500 km or more with ease, and 600km or more in certain cases under standardized test conditions. Although a longer range reduces range anxiety in everyday applications, it also increases the necessity of other charging infrastructure that is able to quickly recharge large battery packs on extended trips and on extreme-use applications [9, 10]. The combination of expanding battery capacities, consumer demand for rapid recharging, and the constraints of traditional DC fast charging has directly driven the development and deployment of extreme fast charging (XFC) stations.

XFC systems generally operate with DC output voltages between 800 and 1000 V and provide charging power of 400 kW or greater, aiming to recharge an EV battery from approximately 10% to 80% state of charge in a time similar to traditional refueling. Attaining this capability is essential for long-distance travel, business fleets, and high-capacity charging stations, since it enables the use of smaller, more economical battery packs while preserving user confidence and alleviating range anxiety [11, 12, 13].

To demonstrate the impact of charger power on charging duration, imagine a vehicle equipped with a 60 kWh battery and an average energy use of 15 kWh per 100 km. Using a typical 11 kW onboard charger, restoring sufficient energy for 300 km of travel takes over four hours; with a 50 kW DC fast charger, the equivalent energy transfer takes approximately one hour, while a 135 kW charger reduces the duration to around twenty minutes. This comparison can be measured through a fundamental energy–power relationship.

Let C_{veh} denote the vehicle energy consumption in kWh/100 km, R the desired driving range in km, and P_{chg} the charging power in kW. The electrical energy required to cover distance R is

$$E_{\text{req}} = \frac{C_{\text{veh}}}{100} R. \quad (2.1)$$

Assuming (for first-order comparison) a constant charging power, the corresponding

charging time is

$$t_{\text{chg}} = \frac{E_{\text{req}}}{P_{\text{chg}}} = \frac{C_{\text{veh}}}{100} \frac{R}{P_{\text{chg}}}. \quad (2.2)$$

For $C_{\text{veh}} = 15 \text{ kWh}/100\text{km}$ and $R = 300 \text{ km}$, $E_{\text{req}} \approx 45 \text{ kWh}$, yielding $t_{\text{chg}} \approx 4.1 \text{ h}$ at 11 kW , 0.9 h at 50 kW , and 0.33 h at 135 kW [13]. (Note: real charging profiles correspond to CC-CV behavior and battery/thermal limitations; the constant-power approximation is employed here for preliminary infrastructure comparison).

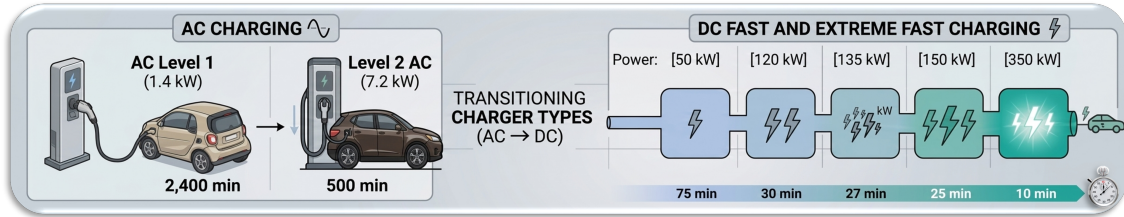


Figure 2.1: Charging required by AC and DC chargers for a 60 kWh battery

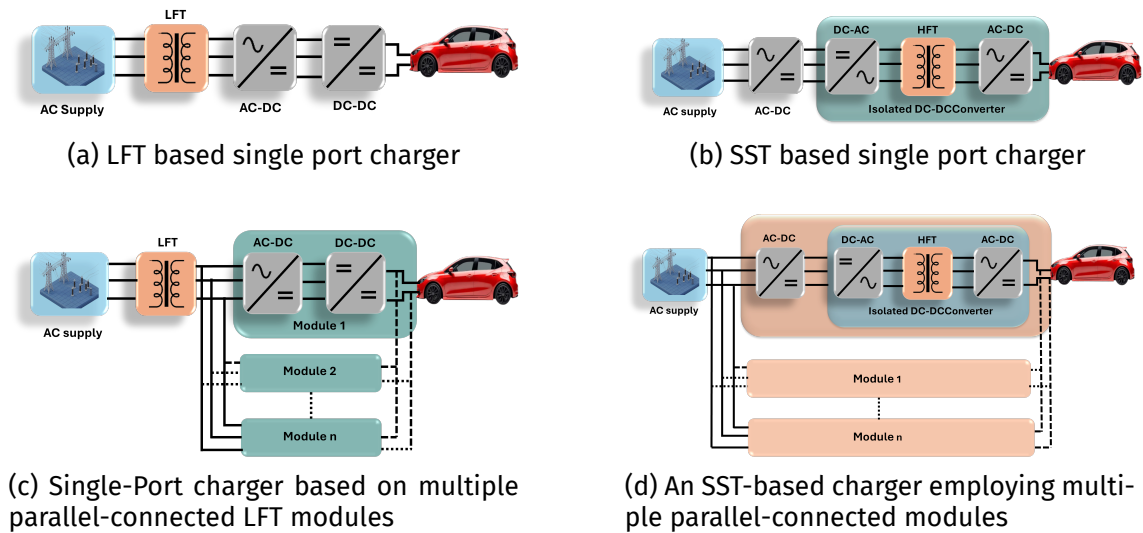


Figure 2.2: DC fast charger based on LFT and SST [10]

The multi-hundred-kilowatt power levels linked to XFC fundamentally transform the interface between charging stations and the electrical grid. When an off-board charger connects directly to the medium-voltage (MV) distribution network (approximately 13–15 kV AC), the station's power-conversion system must incorporate MV switchgear and a step-down/isolating transformer or substation to step down the MV supply for the subsequent AC–DC rectifier. The MV interface enforces particular technical and regulatory stipulations: the front-end must comply with grid-code specifications (harmonic emission thresholds, flicker, voltage-ride-through), restrict injected current harmonics

(standard THD targets <5%), ensure near-unity power factor via active PFC, and synchronize protection and inrush control to prevent detrimental effects on the MV network. MV-connected stations thus integrate harmonic filtering, reactive power compensation, or active power stabilization (e.g., ESS/STATCOM), along with protection mechanisms designed for MV fault currents.

The high power levels (hundreds of kW) required by the XFC introduce significant limitations on both the converter architecture and the overall system design. A major architectural decision relates to the location and installation of galvanic isolation. In certain configurations, as illustrated in Fig. (2.2b) and (2.2c), respectively, galvanic isolation at the grid interface is achieved via a low-frequency transformer (LFT), which ensures substantial protection and a relatively simplified system architecture; however, this results in greater size, weight, and a reduction in power density. Alternatively, isolation can be achieved by a high-frequency transformer (HFT) illustrated by fig. (2.2b) and (2.2d), respectively, integrated into an isolated DC–DC conversion stage, facilitating increased power density and a substantial decrease in the volume of magnetic components [10, 14]. However, increased converter complexity and control challenges.

Modern XFC installations typically utilize a modular power-conversion architecture, wherein identical converter modules are interconnected in parallel or configured in stacked arrangements, to attain station-level power ratings in the hundreds of kilowatts while preserving system maintainability and serviceability. This modular methodology improves system redundancy and facilitates incremental power scaling; however, it requires precise coordination, current distribution, and control measures to avoid circulating currents and reduce the chance of single-point failures.

A summary of several advanced DC fast chargers and extreme fast-charging systems now available in the market is provided in Table 2.2. These entries demonstrate the industry's shift towards elevated DC output voltages and increased per-station power ratings to meet the rigorous performance, safety, and grid compliance standards of fast EV charging.

Table 2.2: Commercially available DC Fast and XFC stations

Charger Model	Rated Power (kW)	Input Voltage (V _{AC})	Output Voltage (V _{DC})	Ref.
ABB Terra 360	360 (peak)	400	150–920	[15]
Tritium Veefil PK350	350	480	~950	[16]
Tesla Supercharger V3	~ 250\vehicle	~430	50–500	[17]
Siemens VersiCharge Ultra 175	~175–178	480	~950	[18]
Gilbarco / Blink RT175-S	175	480	~200–920	[19]
Delta UFC 200	200	400	~1000	[20]

2.3 Limitations

Despite considerable progress in charger and modular designs, the implementation of extreme fast-charging (XFC) infrastructure continues to face several rigorous technological limitations. Primarily, charging systems must function with high conversion efficiency to guarantee that electrical energy is delivered to the EV battery with minimized thermal losses [11]. High power density is equally important, as it allows for delivering high power with a small physical footprint.

Moreover, safety remains a paramount concern in XFC design. To ensure user safety and compliance with electrical safety standards, galvanic isolation is essential between the utility grid and the electric vehicle battery. Moreover, chargers must handle a broad range of output voltages to accommodate the diverse range of EV models currently on the market.

The ability to fulfill these demands, including high efficiency, high power density, galvanic isolation, and wide voltage flexibility on a single platform, is a significant engineering challenge and requires the implementation of new power electronic topologies and control mechanisms. In addition to the charger, system-level factors are also crucial. XFC stations must connect to the power grid while ensuring stability and power quality, necessitating the injection of low-distortion, low-harmonic currents from the grid side. In the absence of adequate management and filtering, high-power charging systems may impose significant stress on grid components, potentially overloading transformers, increasing system losses, and degrading overall power quality [13, 21].

Therefore, XFC infrastructure needs to be designed to provide grid-side currents with

minimal harmonic distortion. Without sufficient harmonic mitigation, grid components may experience excessive stress, leading to transformer overloading, increased system losses, and degraded power quality. The integration of charger-level and grid-level requirements necessitates the advancement of power electronic architectures and intricate control strategies that can simultaneously achieve high efficiency, lightweight design, electrical isolation, broad-range voltage adaptability, and grid compliance in extreme fast-charging applications.

2.4 Extreme Fast Charging Station Architectures

An advanced XFC station often requires a three-phase medium-voltage (MV) grid connection to meet the substantial power requirements of extreme fast charging. The incoming medium voltage supply is reduced to the operational voltage of the charging infrastructure using either a traditional medium-voltage/low-voltage (MV/LV) low-frequency transformer (LFT) or a solid-state transformer (SST). The selection of transformer technology directly influences system efficiency, power density, controllability, and integration flexibility with sophisticated power electronic interfaces.

Subsequently, after voltage conversion, the station bus bar, which connects various extreme fast chargers, localized renewable energy sources (RESs), and energy storage systems (ESSs), may be configured as either an AC or a DC distribution bus. Each design offers unique advantages and technological obstacles (conversion phases, control complexity, protection, and standards compliance); the following sections give further insights into both models.

2.4.1 XFC Station with AC BUS

Fig. 2.3a illustrates the XFC station designed on an AC bus architecture. The system involves stepping down the three-phase medium-voltage (MV) supply to the station distribution level using a single central transformer, which may be either a traditional line-frequency transformer (LFT) or a power electronics-based solid-state transformer (SST). The transformer output establishes a shared low-voltage AC bus that powers all on-site appliances. Each XFC interfaces with the AC bus via an individual AC/DC rectifier,

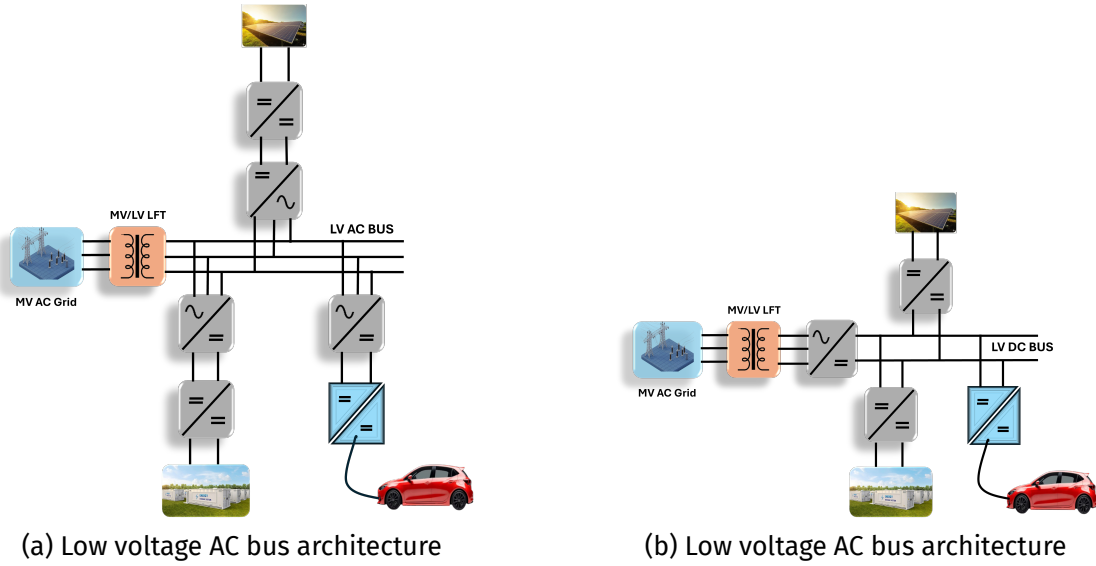


Figure 2.3: Extreme Fast Charging Station based on AC and DC bus

subsequently followed by a DC/DC stage that generates the regulated DC link necessary for the car charger. Local renewable energy sources, such as photovoltaic systems and battery energy storage systems, are interconnected to the same AC bus, which is used by converters for each source, such as DC/AC inverters for photovoltaic systems and bidirectional converters for batteries [22].

Although the AC-bus design advantages come from a robust AC distribution system, including established protection devices, switching equipment, metering equipment, and clearly defined installation procedures that facilitate the utilization of readily available charger modules for straightforward procurement and maintenance, the necessity for dedicated AC/DC and DC/DC converters for each XFC charger and each energy storage or renewable unit markedly escalates the number of power-conversion stages [23]. An increase results in higher capital costs, larger cumulative conversion losses, higher harmonic emissions, and greater complexity in control and thermal management. The use of solid-state transformers (SSTs) or station-level active filtering methods might mitigate these constraints by improving voltage control and power quality, yet these solutions also entail increased system costs and design complexity.

2.4.2 XFC Station with DC BUS

A DC-bus charging design, shown in Fig. 2.3b, employs a centralized power-conversion stage located after the line-frequency transformer (LFT) to create a unified DC distribu-

tion bus. Multiple extreme fast chargers may be linked to the bus using specialized DC/DC converters. Furthermore, renewable energy sources (RES) and energy storage systems (ESS) may be interconnected with the DC bus using specialized DC/DC converters to facilitate grid support [24, 25]. Unlike AC-bus configurations, the DC-bus method obviates the need for separate AC/DC conversion stages at every charger and interfaced source, thereby reducing the total number of power-conversion stages. This reduction enhances system efficiency, lowers the component count, and reduces capital and maintenance expenses.

The DC-bus voltage is often chosen to be below 1 kV to minimize insulation needs, alleviate safety concerns, and assure compatibility with recently developed battery voltage ranges. At this voltage level, a DC-bus-based XFC station may comply with the same safety and regulatory criteria as typical AC-bus-based XFCS [26, 27]. An further benefit of the DC-bus arrangement is the existence of one single point of common coupling (PCC) with the medium-voltage grid, which optimizes the execution of both grid-connected and islanded operating modes and improves station-level power-flow regulation.

The DC-bus design has advantages from a system-control standpoint, such as eliminating reactive power transfers with the upstream AC network and enabling more direct and decoupled management of active power flows [28]. Furthermore, the DC-bus configuration facilitates the implementation of partial-power converter (PPC) topologies, in which only a portion of the total electric-vehicle charging power is managed by the power-electronic interface [29]. PPC-based solutions mitigate semiconductor stress by restricting processing power, enhancing conversion efficiency, and minimizing converter dimensions, thereby facilitating the development of small, modular, and scalable extreme-fast charging station architecture.

2.4.3 Medium/HFT based DC Bus Architecture

In conventional MV-connected charging infrastructures, galvanic isolation between the medium-voltage grid and the low-voltage DC bus is typically achieved using a line-frequency transformer (LFT), as illustrated in Fig 2.3. However, such transformers are generally bulky, expensive, and occupy significant physical space. Moreover, their integration introduces additional design constraints related to installation, thermal man-

agement, and the interfacing of the medium-voltage grid with the power electronic conversion stages. To mitigate these restrictions, an isolated DC/DC conversion stage using a medium- or high-frequency transformer (Medium/HFT), positioned next to the front-end AC/DC converter, can supersede the traditional LFT while maintaining the necessary galvanic isolation in compliance with IEEE 1547.

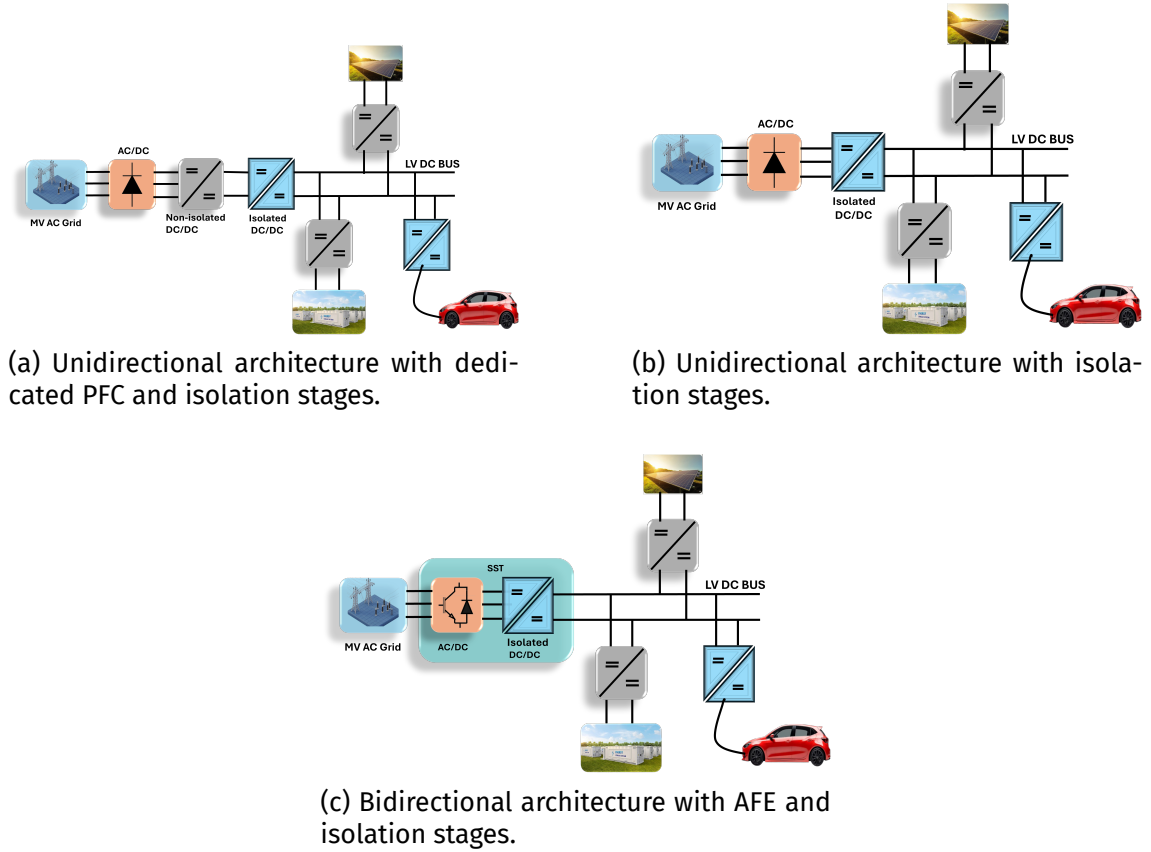


Figure 2.4: An Medium/High frequency transformer-based common DC bus configurations. [21]

A number of MV/HFT-based DC-bus configurations have been presented in the literature and are shown in Fig. 2.4. The three-stage unidirectional arrangement shown in fig. 2.4a comprises a front-end AC/DC rectifier, followed by a non-isolated DC/DC converter with power factor correction (PFC), and finally an isolated DC/DC stage to ensure galvanic isolation. A different structure, shown in Fig. 2.4b combines the PFC and isolation functions into a single conversion stage, thereby minimizing the total number of power-conversion stages and enhancing overall system efficiency [30].

Figure 2.4c illustrates a bidirectional design that incorporates an active front-end (AFE) for AC/DC conversion with power-factor adjustment, using pulse-width-modulated

(PWM) control of the active switches, preceded by an isolated DC/DC converter. This design facilitates bidirectional power flow and offers a significant advantage over unidirectional options: the second-stage isolated DC/DC converter can be rated at lower power, reducing converter size, improving efficiency, and lowering system cost [31, 32]. The comparison of DC and AC bus architectures with their advantages and disadvantages is summarized in the table. 2.3.

The architectures examined to far generally use a standard two-level active front-end (AFE) for the front-end AC/DC stage. In medium-voltage extreme fast-charging (XFC) stations, this stage can potentially be replaced with a multilevel converter without modifying the rest of the system architecture. The multi-level converter facilitates direct integration with the medium-voltage grid, and power factor regulation is achieved within the converter control [33]. As a result, multilevel converter-oriented front ends have received increased attention for extreme fast charging applications.

The aforementioned architectural alternatives demonstrate that, although the fundamental structure of the XFC station may remain consistent, the choice of the front-end converter is crucial for enabling medium-voltage operation, scalability, and compliance with power quality standards [34]. The increasing acceptance of multilevel converters as front-end stages in XFC structures necessitates a comprehensive examination of multilevel converter topologies and their operational principles for XFC applications.

Table 2.3: Comparison between DC and AC connected EV charging architecture.

Criteria	DC Bus Architecture	AC Bus Architecture
Integration of Energy Sources	Easier	Complex
Number of Conversion stages	Lower	Higher
Efficiency	Higher	Lower
Impacts from utility side	Less	High
Rating of AC-DC rectifier	High	Medium
Protection devices	Sophisticated	Unsophisticated
Control	Simple	Complex
Cost	Less expensive	More expensive

2.5 Multilevel Converter Topologies

Multilevel converters (MLCs) are extensively used in both research and industry to generate alternating voltages from many lower-level DC sources [85]. For fast and extreme-fast EV charging applications, MLCs are frequently used as the AC-DC active front-end owing to their capability for high power transfer, thereby enhancing efficiency and power density [35]. Charging systems may be classified into three categories based on the existing literature: (1) cascaded H-bridge (CHB), (2) flying-capacitor (FC), and (3) neutral-point-clamped (NPC) converters.

The operational principle of a Multi-Level Converter (MLC) is to generate a staircase voltage waveform at the output by dynamically switching combinations of capacitors, voltage sources, and power electronic devices. This methodology provides numerous practical benefits for high-voltage, high-power converters: diminished total harmonic distortion (THD) via multilevel pulse-width modulation, diminished dv/dt across the load, minimized electromagnetic interference (EMI), decreased voltage stress for individual semiconductor devices, and the potential for utilizing smaller magnetic components [36, 37]. These attributes enable MLCs particularly suitable for medium- and high-voltage charging structures, where operating stress on power devices, power quality metrics, and thermal management are essential design factors.

2.5.1 Neutral Point Clamped Multilevel AC-DC Converter

The neutral-point-clamped (NPC) 3-level converter is a commonly used multilevel AC-DC configuration that enables medium-voltage operation while generating low-distortion output waveforms and input currents, minimizing total harmonic distortion (THD). Figure 2.5 depicts a three-phase, three-level neutral-point clamped (NPC) converter. In this architecture, each semiconductor device is required to withstand approximately half of the total DC-link voltage; hence, lower-voltage devices (for instance, 500 V instead of 1000 V) can be used, which generally provide enhanced switching characteristics and lower switching losses.

In reference [37], the authors presented an electric vehicle charging station using a centrally positioned NPC AC-DC converter connected to the medium-voltage grid on

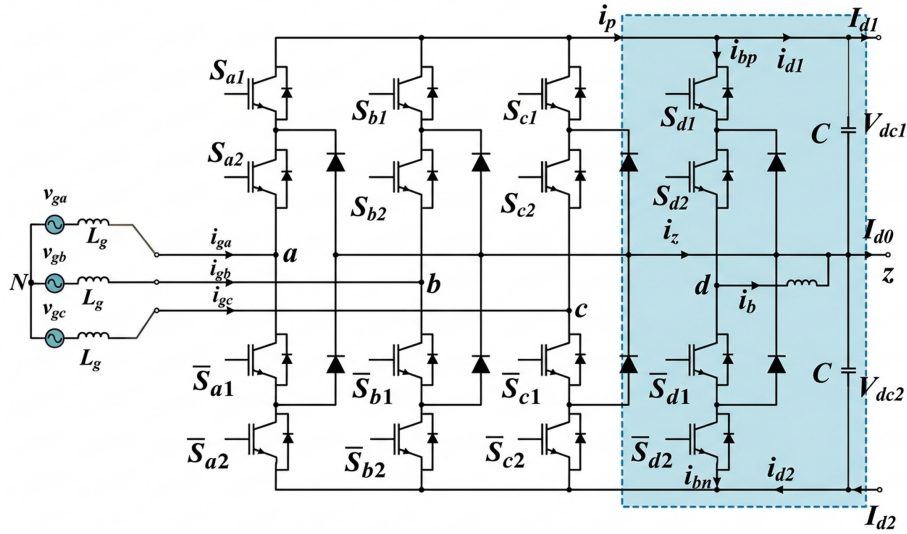


Figure 2.5: Neutral Point clamped multilevel AC-DC [38]

the AC and to a bipolar DC bus on the DC side. The integration of NPC topology with a bipolar DC bus presents multiple practical benefits: (1) it diminishes the step-down requirement for subsequent DC-DC fast chargers, (2) it enhances operational reliability by allowing one DC-DC unit to supply the load throughout the breakdown or maintenance of a separate unit, and (3) it significantly improves station power requirements due to the increased equivalent DC-link capacitance [38].

Notwithstanding these advantages, bipolar DC-bus configurations exacerbate DC-link voltage imbalances, which are less evident in unipolar systems. In contrast to the unipolar scenario, these imbalances cannot be entirely alleviated by modulation strategies alone; the stochastic characteristics of charging stations, such as unpredictable car arrivals and diverse battery chemistries, exacerbate the imbalance. A prevalent mitigation strategy involves incorporating an active voltage-balancing circuit, configured as an auxiliary leg in addition to the three conventional NPC legs, thereby restoring the symmetry of the bipolar DC linkages (Fig.2.5) [38, 39].

The research presented [40] indicates that a three-level stacked neutral-point-clamped (NPC) design surpasses the traditional three-level NPC in AC-DC applications, primarily due to its capacity for higher switching frequencies and enhanced loss distribution. The conventional NPC architecture has a notable practical constraint due to the unequal distribution of conduction and switching losses across semiconductor devices, complicating thermal design and potentially restricting both the attainable switching frequency

and maximum phase current [41]. The active NPC (ANPC) topology enhances the NPC by including supplementary active switches in antiparallel with the NPC diodes. The additional degrees of freedom provided by ANPC, along with appropriately designed modulation schemes that utilize redundant zero-voltage switching states and alternative commutation sequences, enable a more uniform distribution of conduction and switching losses among devices, consequently mitigating thermal areas and enhancing overall loss balancing [42, 43]. These advantages include elevated hardware and control complexity, as each additional switch needs a specific gate-drive interface, and the control system must oversee a much expanded switching state space.

2.5.2 Flying Capacitor Multilevel AC-DC Converter

Figure 2.6 illustrates the flying-capacitor multilevel converter (FC-MLC), a topology extensively studied for medium- and high-power applications. The intrinsic voltage modulation of multilevel converters generates fundamental-frequency ripple among the converter phases; alleviating this ripple requires additional submodule capacitor energy, consequently placing constraints on size, cost, and thermal management [44]. The flying-capacitor multilevel converter (FC-MLC) can diminish the necessary capacitor energy while functioning at elevated switching frequencies, since elevated switching activity alleviates low-frequency voltage fluctuations. Three-phase MLCs are typically favored for EV charging due to their enhanced power-delivery capacity; however, three-phase rectifiers cannot attain the minimal conduction losses achievable with single-phase rectifiers utilizing unfolding techniques, as current introduced into one phase gets returned through the other phases.

Seven-level flying-capacitor multilevel converters (FC-MLCs) demonstrate efficiency and performance on par with other multilevel converter configurations. FC-MLCs may serve as rectifier stages, perhaps when combined with an unfolding stage, and experimental implementations of seven-level FC-MLC rectifiers are documented in [46, 47]. Moreover, interleaved six-level FC-MLC topologies have been suggested to achieve enhanced efficiency and elevated power density. A further benefit of the FC-MLC topology is the diminished demand on the PWM modulator: due to the elevated switching-node frequency characteristic of FC-MLCs, substantial modulation resolution can be attained

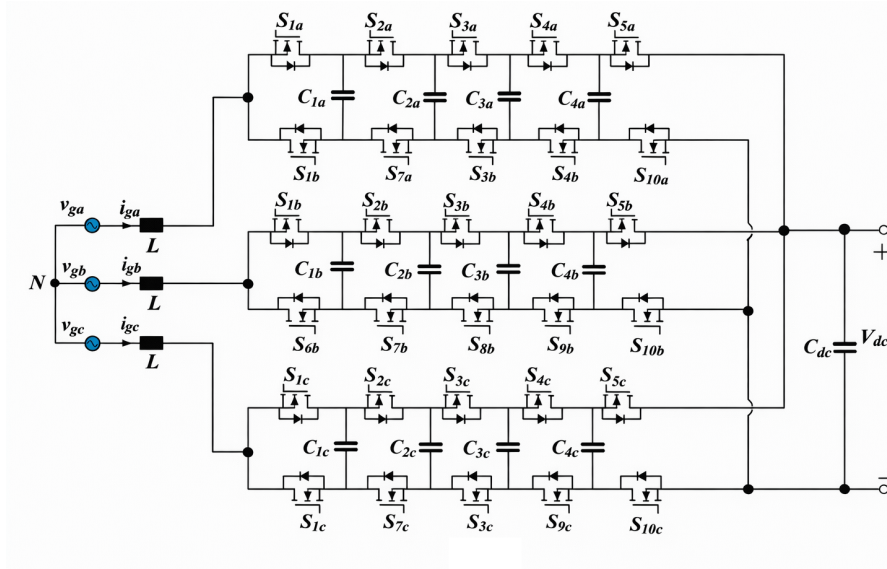


Figure 2.6: Flying Capacitor Multilevel Converter for EV charging. [45]

without significantly raising the PWM frequency, thus facilitating modulation and control execution [48].

Additionally, to alleviate the double line-frequency power pulsing characteristic of AC-DC conversion, active buffer stages are often used for power decoupling in FC-MLC-based rectifiers. Due to the high-frequency functioning of FC-MLCs, the necessary filter components may be significantly reduced; nevertheless, the use of smaller inductive elements may result in leading current behavior, complicating power-factor-correction (PFC) regulation. The research detailed in [49] tackles this problem by using feedforward control techniques. Furthermore, [49] suggests a specialized control methodology to mitigate voltage spikes and regulate carrier-signal deterioration while functioning at zero current ripple. A hybrid control technique that integrates valley current detection with constant effective duty-cycle management has been implemented for a four-level FC-MLC, therefore improving capacitor voltage regulation and ensuring stable capacitor balancing throughout a broad load range[50].

2.5.3 Cascaded H-Bridge Multilevel AC-DC Converter

One of the most flexible multilevel converter topologies is the three-phase cascaded H-bridge (CHB) converter, as shown in Figure 3.3. Its modular structure allows fault isolation at the submodule level and simplifies maintenance without shutting down the entire system. The CHB inverter can be installed in a delta or star connection for three-

phase installations [51]. Moreover, The total number of cascaded cells per phase may be freely changed while operating in a star configuration, enabling scalable operation from single-phase to multi-phase systems. In order to guarantee the correct voltage reference in single-phase operation, the neutral point of the converter has to be linked to the grid ground.

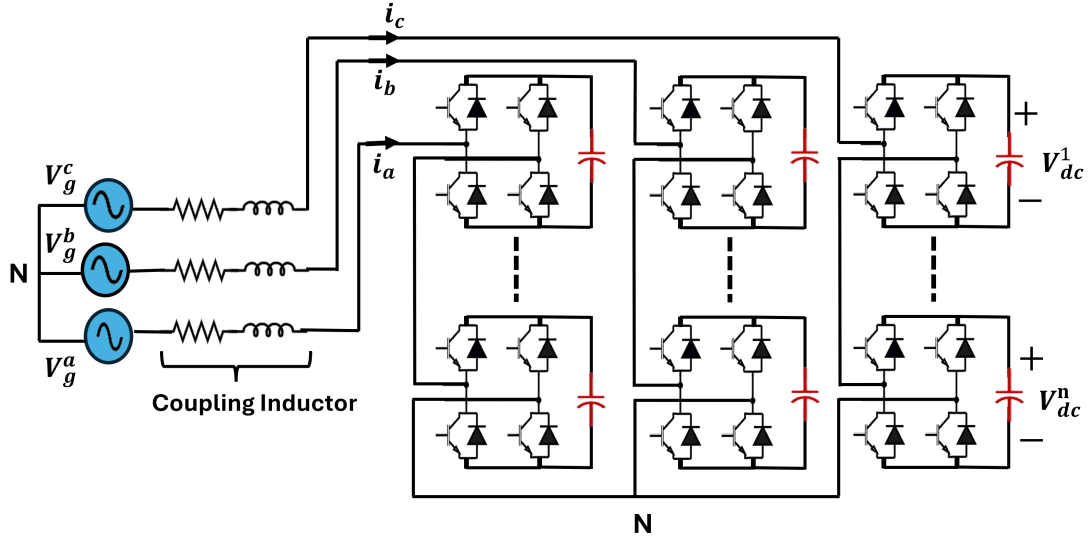


Figure 2.7: Cascaded HBridge AC-DC converter

The intrinsic modularity of the CHB topology enables the cascading of many low-voltage power cells for direct interfacing with medium-voltage grids. This attribute is especially beneficial for high-power electric vehicle fast charging stations, where scalable voltage levels, the possibility of modular expansion of the system, and independent control over converter modules are required.

References [51, 52] delineate three-phase electric vehicle charging station structures by employing modular cascaded H-bridge multilevel AC-DC converters. The series-parallel configuration of unit cells produces several redundant switching states, which can potentially be used to balance capacitor voltage and fault isolation without disrupting normal operation [51]. The research presented in [53, 54] investigates the single-phase and three-phase CHB converters being used as AC-DC rectifiers. In real applications, device-level nonlinearities—such as activation and deactivation delays and semiconductor saturation voltages—can induce distortion in individual cells, resulting in deviations in the generated output voltage. To mitigate these impacts, compensating approaches based on predictive current management have been developed to enhance the grid-current

harmonic performance over one fundamental PWM fundamental cycle [55].

Another modular multilevel electric vehicle charging station is explained in [56], whereby each submodule, as shown in Fig. 5(a), enhances the total voltage and power capacity of the system. The design may be easily modified to fulfill the high-voltage and high-power demands of fast and extreme fast EV charging by cascading the numerous submodules in series.

Advanced CHB-based XFC designs have also been documented in the literature. A extreme fast charging station using a solid-state transformer (SST) connected with a cascaded H-bridge (CHB) converter as the medium-voltage AC–DC active front end is discussed in [57]. In this structure each CHB cell followed by an isolated quad active bridge (QAB) stage, facilitating the establishment of several separate fast-charging ports and obviating the need for a low-frequency transformer. Nonetheless, the separate loading of these ports results in inter-cluster power imbalance, observable via unequal DC-link capacitor voltages and elevated zero-sequence currents, which exacerbate current stress in the CHB switches. To alleviate this impact, the authors include a balancing winding in the QAB transformers to partly redistribute power across clusters. Although the presented strategy is effective to some extent, it elevates transformer complexity, circulating currents, and magnetic losses. Moreover, its performance is largely dependent upon transformer specifications, consequently limiting its efficacy under extreme or abruptly fluctuating load circumstances.

A novel multi-port bidirectional three-phase AC–DC converter for electric vehicle charging microgrids is shown in [58], which integrates the utility grid, solar power generation, battery energy storage, and several charging ports inside a singular conversion stage. This architecture attains a high power factor, minimal current distortion, and simplified transformation for low-voltage charging applications; however, the absence of galvanic isolation and the centralized single-stage configuration limit its implementation as a fast charging stations. Furthermore, the difficulties of scalability, redundancy, and DC-link voltage balancing associated with multilevel active front-end converters are not adequately addressed.

Another CHB-based XFC station is reported in [59], whereby each CHB cell module followed by a DC/DC stage and serve as an autonomous charging port. Since, a single

multilevel CHB-AFE serve several vehicle at the same time, may introduce a considerable stress on the MV grid. To mitigate this impact, battery energy storage (BES) modules are connected to every converter cell in a distributed manner, which facilitate partial buffering against high-power fluctuations.

Despite the appealing attributes of CHB-based XFC designs with distributed battery energy storage module, their physical implementation presents significant obstacles. In particular, the existence of many independent DC links which serves to unequal port loads, results in DC-link voltage imbalance and elevated stress on both converter switching devices and BES module. As a result, even though this architecture is a highly motivated and promising solution for applications requiring extremely fast charging, its successful implementation greatly depends on sophisticated control strategies that can guarantee reliable DC-link voltage balancing while also reducing the stress on BES module under highly fluctuating operating environments.

A comprehensive comparison of the CHB converter architecture with other multilevel AC-DC converter configurations is highlighted in Table 2.4.

Table 2.4: Comparison of Multilevel AC-DC Converter Structures

Structure	Power (kW)	Output Voltage (V)	THD (%)
Cascaded H-bridge (two cell)	2	540	< 5
Three-phase Hybrid Cascaded H-bridge	0.55	–	< 5
Four-leg three-phase NPC with voltage balance circuit	3.6	~450	5.39
Three-level NPC	30	858	2
Three-level NPC	1.2	~210	2.95
Three-phase three-level stacked NPC	2	110	2.03
Single-phase seven-level active NPC	50	1000	–
Seven-level FCMLC	1.5	400	< 3.5
Interleaved six-level FCMLC	7	400	< 3

The cascaded H-bridge (CHB) architecture provides flexible scalability, medium-voltage capabilities, and intrinsic redundancy, making it ideal for electric vehicle fast-charging infrastructure. The existence of many separate DC links presents significant issues in power regulation and voltage control, especially under the dynamic operating circumstances of extremely fast charging stations. Consequently, ensuring balanced DC-link voltages among cascaded cells emerges as a primary control need, prompting a com-

prehensive examination of DC-link voltage balancing methodologies in the subsequent section.

2.6 DC-Link Voltage Balancing Strategies

Cascaded H-bridge (CHB) converters inherently employ multiple independent DC-link capacitors, one per power cell, enabling modularity and medium-voltage operation using low-voltage semiconductor devices. While this structural characteristic offers significant advantages, it also introduces a fundamental control challenge: maintaining balanced DC-link voltages across the cascaded cells [60]. In practical CHB-based systems, unequal power sharing, asymmetric operating conditions, and grid disturbances can lead to DC-link voltage imbalance. Such imbalance increases semiconductor current stress, distorts the synthesized output voltage, degrades input current quality, and may adversely affect system stability and reliability.

The primary control which is responsible to generate the per phase output voltage is realized by implementing voltage-oriented control (VOC), which alone is insufficient to assure DC-link voltage regulation in CHB converters; thus, an extra control layer devoted to DC-link voltage balancing is necessary to maintain the DC_link voltage at predefined reference value and for stable operation of multilevel converter [61]. Consequently, effective DC-link voltage balancing is crucial not only for the safe and efficient operation of CHB converters, but also for attaining high power quality, minimal current harmonic distortion, and unity power factor at the grid interface.

This section examines DC-link voltage balancing strategies especially designed for CHB converters, focusing on modulation-based and redundant switching- state-based methods documented in the literature. The primary categories of multilevel modulation techniques utilized in CHB converters are depicted in fig. 2.8, classified by switching frequency and modulation principle, which includes selective harmonic elimination, multicarrier PWM, and space-vector modulation. This section discusses the operational principles, benefits, and limits of various approaches.

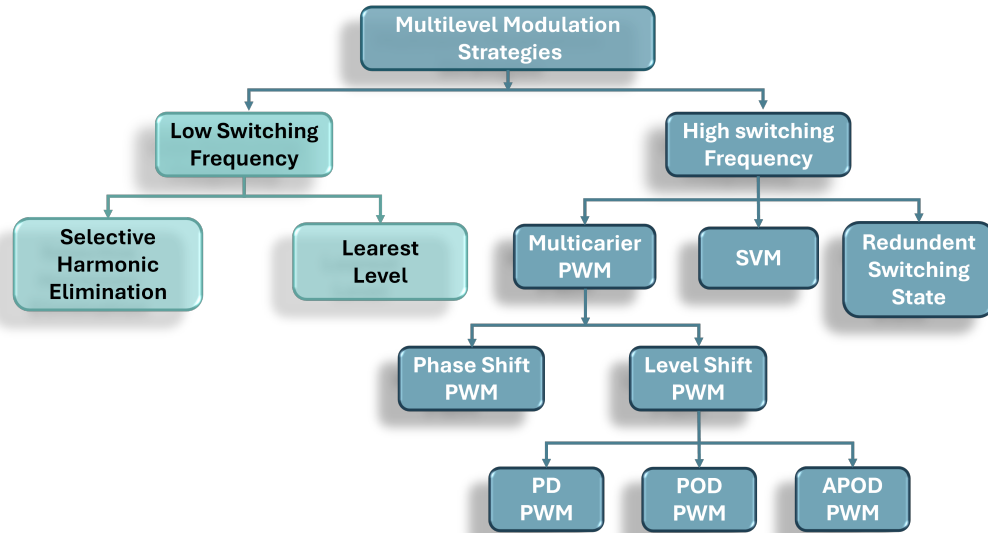


Figure 2.8: Multilevel Modulation strategies

2.6.1 Phase-Shifted Pulse-Width Modulation for Multilevel Converters

High-frequency modulation techniques for multilevel converters are typically implemented through multicarrier pulse-width modulation (PWM), utilizing several carrier signals alongside a shared modulating reference to produce the switching signals for power semiconductor devices available in a single cell of a modular converter. Phase-shifted pulse-width modulation (PS-PWM) has been thoroughly examined and utilized for multilevel converters comprising series-connected power modules, especially for cascaded H-bridge (CHB) converters, owing to their modular architecture, advantageous harmonic characteristics, and straightforward implementation [60].

In PS-PWM, a single sinusoidal reference waveform is equally transmitted to all power modules; however, the carrier signals for each module are phase-shifted relative to each other. Each H-bridge cell is regulated autonomously; nevertheless, the synchronized phase displacement of the carriers guarantees that the switching behaviors of the cells are uniformly distributed across the carrier period. Consequently, the combined output voltage waveform demonstrates a greater effective switching frequency than any single cell, despite the fact that each semiconductor device switches at a very low switching frequency.

In CHB converters, PS-PWM is often realized as unipolar PWM, applied individually to each H-bridge cell [61]. In this arrangement, each cell utilizes complementary switching

functions based on the comparison of a shared sinusoidal reference and a triangular waveform used as a carrier. The carriers related to neighboring cells are phase-shifted by a fixed angle specified by

$$\Delta\phi = \frac{\pi}{M}, \quad (2.3)$$

The systematic carrier phase displacement results in the interleaving of individual cell switching instants repeatedly over the carrier period, consequently multiplying the switching frequency at both the phase and line voltage levels .

The key feature of PS-PWM lies in its harmonic properties. Even though all H-bridge cell switches are synchronized to the base carrier frequency, the interleaved switching mechanism generates a composite output voltage waveform with predominant harmonic components displaced toward higher frequencies. As a result, low-order harmonics are considerably reduced, and the perceived switching frequency of the generated phase voltage approaches Mf_c , with f_c being the carrier frequency [62, 63]. This feature is especially advantageous in high-power CHB systems, where elevating the switching frequency of individual devices is unfavorable owing to significant switching losses.

Besides its advantageous harmonic performance, PS-PWM provides significant adaptability and scalability. As all H-bridge cells use the same reference waveform and vary solely in the phase of their carrier signals, the modulation scheme can be easily adapted to converters with several cascaded cells without necessitating major structural modifications. This modular feature also enables fault-tolerant operation, allowing individual cells to be bypassed or reinserted with little effect on the entire modulation system.

In spite of these benefits, PS-PWM demonstrates intrinsic restrictions when used in cascaded H-bridge rectifiers operating with floating DC-link capacitors. The modulation mechanism does not directly control the individual DC-link voltages, and during rectifier operation, imbalanced charging and discharging of the capacitors may arise from parameter deviations, non-ideal switching patterns, or dynamic operating conditions. Over time, these imbalances become evident, leading to distorted voltage waveforms, diminished voltage utilization, and elevated voltage stress on certain H-bridge cells.

To address this problem, PS-PWM is often augmented by supplementary control mechanisms, such as power-sorting algorithms, which reallocate active power across the H-bridge cells [64]. The use of these balancing solutions increases control complexity and

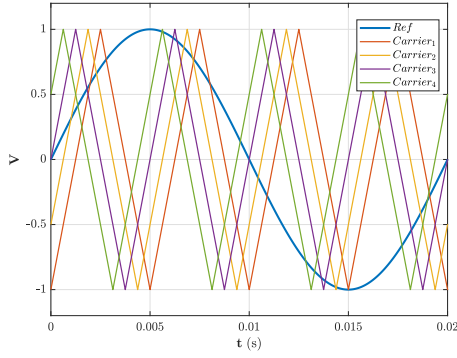
may negatively impact dynamic performance, especially under transient conditions or across extensive operating ranges.

Moreover, the fixed phase relation among carrier signals in PS-PWM constrains the attainable degrees of freedom for sophisticated control purposes. In contrast to space-vector modulation or selective harmonic elimination PWM, PS-PWM provides limited adaptability for selective harmonic shaping or direct use of switching-state redundancies for DC-link voltage stabilization [65, 66]. Additional difficulties for real-time digital implementation arise from the growing need for carrier synchronization and timing precision as the number of cascaded cells increases.

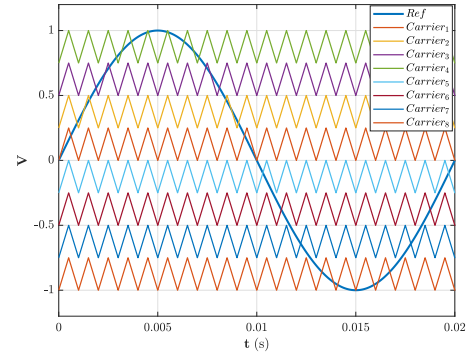
In conclusion, phase-shifted PWM is a recognized and advantageous modulation technique for cascaded H-bridge converters, providing an effective balance between harmonic performance, reduction of switching losses, and ease of implementation. Through the use of carrier phase displacement, PS-PWM effectively enhances the perceived switching frequency of the generated output voltage while preserving low switching stress on individual semiconductor components. Due to its modular architecture and scalability, PS-PWM has been extensively used in multilevel converter applications, including series-connected power cells. Nonetheless, the attributes of PS-PWM also encourage the investigation of alternative multicarrier modulation schemes that provide varying compromises among harmonic performance, control flexibility, and voltage utilization. Fig. 2.9a shows the PS-PWM working principle applied to a CHB converter with four H-bridge cells per phase under unipolar modulation.

2.6.2 Level-Shifted Pulse-Width Modulation for Multilevel Converters

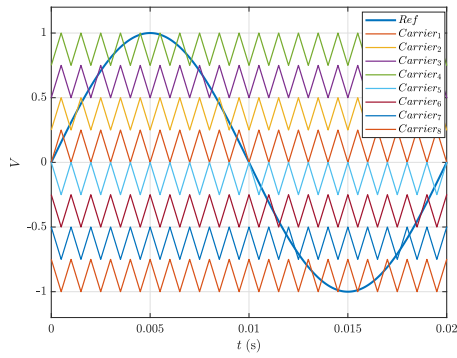
Level-shifted pulse-width modulation (LS-PWM) is a widely utilized high switching frequency modulation technique for multilevel power converters. Like other multicarrier PWM methods, LS-PWM generates multilevel voltage waveforms by comparing a single modulating reference with multiple triangular carrier signals. In contrast to phase-shifted PWM, LS-PWM utilizes carrier signals that are shifted vertically in amplitude while maintaining phase. The carriers are organized into adjacent bands that together cover the entire modulation range, with each carrier band corresponding to a particular voltage level of the converter.



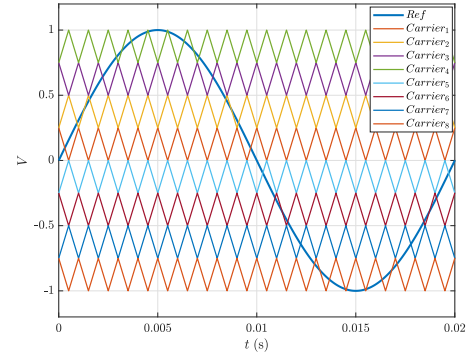
(a) Phase-shift PWM for 9-level CHB



(b) Level-shift PWM for 9-level CHB



(c) Phase opposition LSPWM for 9-level CHB



(d) Alternative phase opposition LSPWM for 9-level CHB

Figure 2.9: Carrier based modulation strategies for multilevel CHB converter

The core operating concept of LS-PWM relies on the direct amplitude comparison between the reference signal and a series of carrier waveforms. As the sinusoidal reference moves through the carrier bands, switching transitions occur at the intersection points between the reference and the carriers, resulting in stepped output voltage waveforms. This modulation technique allows LS-PWM to generate multilevel voltages in a clear and methodical way, making it especially appropriate for converters with distinct voltage levels and centralized DC-link topologies.

According to the relative phase relationships of the carrier signals above and below the zero reference, LS-PWM may be categorized into three prominent schemes: phase disposition (PD-PWM), phase opposition disposition (POD-PWM), and alternative phase opposition disposition (APOD-PWM). In PD-PWM, all carrier signals are phase-aligned over the full modulation spectrum, leading to a symmetrical carrier configuration. In POD-PWM, the carriers positioned above the zero reference are phase-shifted by 180°

in relation to the ones below it, whereas in APOD-PWM, each vertical adjacent carrier is phase-shifted by 180° with respect to its adjoining carrier [67, 68]. The carrier distribution techniques affect the harmonic spectrum of the generated output voltage, especially for common-mode voltage components and low-order harmonics. Figure 2.9b depicts the fundamental notion of level-shifted PWM, while fig. 2.9c, fig. 2.9d provide POD-PWM, and APOD-PWM strategies, respectively.

The selection of carrier placement directly influences the harmonic performance of LS-PWM. PD-PWM is often preferred for line-to-line voltage quality because of its symmetrical configuration, although POD-PWM and APOD-PWM are frequently used to mitigate certain harmonic components or common-mode voltage impacts. With an increase in voltage levels, the harmonic spectrum becomes more concentrated around multiples of the carrier frequency, enhancing waveform quality but complicating carrier management.

LS-PWM provides a straightforward and intuitive modulation framework for cascaded H-bridge (CHB) converters, which can potentially be implemented using conventional PWM hardware and digital control system [69]. The direct correlation between carrier bands and voltage levels enables clear mapping of modulation signals to switching states. At reasonable switching frequencies and a limited number of cascaded cells, LS-PWM may attain acceptable harmonic performance without imposing a significant computational load.

In contrast to phase-shifted PWM, LS-PWM does not intrinsically allocate switching actions uniformly across the cascaded H-bridge cells. As all carriers are phase-synchronized, switching events often occur simultaneously across several cells, consequently diminishing the beneficial interleaving of switching activities. The observed switching frequency of the generated output voltage does not increase proportionately with the number of series-connected cells, and the harmonic advantages gained by natural interleaving are restricted.

Moreover, LS-PWM lacks inherent DC-link voltage balancing functionality in CHB converters equipped with floating DC-link capacitors. During rectifier operation, non-uniform power processing across the cells can result in persistent voltage imbalance, adversely impacting voltage level uniformity and diminishing output waveform quality [70]. As

a result, LS-PWM-based CHB systems typically necessitate auxiliary voltage balancing mechanisms to ensure stable operation.

Numerous balancing techniques have been documented in the literature to mitigate this issue. These includes reference signal alteration methodologies, wherein the modulation reference is individually modified to control distinct DC-link voltages. Despite their effectiveness, these additional control layers complicate the system and may generate increased dynamic interactions.

Moreover, LS-PWM encounters difficulties with carrier generation, synchronization, and computational cost as the number of voltage levels increases [71]. The exact alignment of multiple carrier signals and the precise identification of reference crossings become more challenging, especially in high-power applications where strict timing is required. These factors may restrict the scalability of LS-PWM in converters including several cascaded H-bridge cells.

In conclusion, level-shifted PWM is a straightforward and proven multicarrier modulation technique for multilevel converters, providing simplicity of implementation and satisfactory harmonic performance under moderate operating conditions. However, its limited inherent DC-link voltage control and natural switching interleaving capabilities encourage the need for additional balancing methods when used in cascaded H-bridge rectifiers. These factors establish LS-PWM as a realistic modulation choice for certain CHB applications, while also emphasizing the trade-offs that differentiate it from other high-frequency and fundamental frequency modulation techniques discussed in the literature.

LS-PWM provides simple implementation and adequate harmonic performance for cascaded H-bridge (CHB) converters, especially at modest switching frequencies. In contrast to phase-shifted PWM, LS-PWM does not automatically allocate switching actions uniformly across cascaded cells, thereby limiting its intrinsic capacity to balance DC-link capacitor voltages. Consequently, LS-PWM is often integrated with supplementary balancing mechanisms—such as reference signal adjustment, redundant switching state selection, or outer-loop voltage balancing controllers—to ensure uniform DC-link voltages across CHB cells.

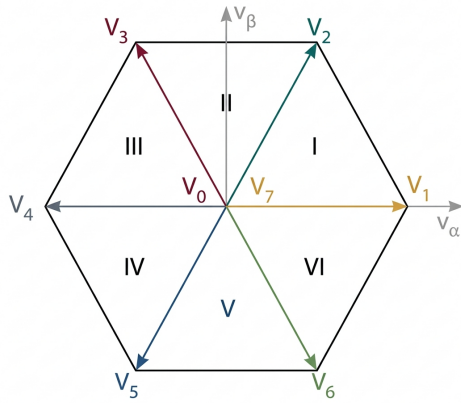
2.6.3 Space Vector Modulation

Space-vector modulation (SVM) is a discrete-time modulation technique extensively used in three-phase power electronic converters. Instead of separately controlling each phase leg, SVM identifies the optimum switching state of the entire three-phase converter by representing the reference voltage vector and the converter's switching states within a unified vector space. The final choice of switching states is determined by a mathematical transformation that correlates the required reference voltage with the line-to-line voltage vectors produced by the converter. Thus, in contrast to carrier-based modulation approaches that directly generate phase voltages, space-vector modulation (SVM) primarily emphasizes line voltages, with the associated phase voltage waveforms emerging implicitly from the chosen switching sequence.

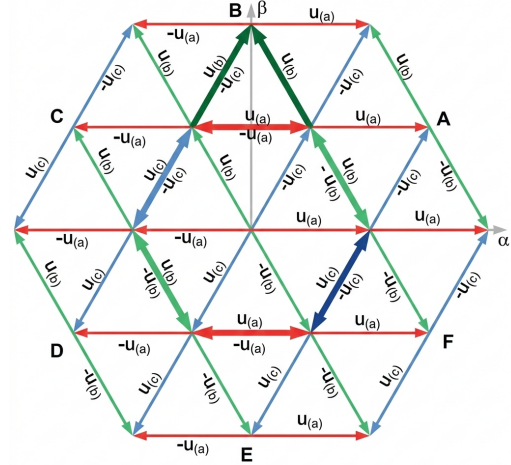
The primary concept of space-vector modulation is the graphical representation of three-phase converter switching states in the stationary α - β reference plane. The switching state of a three-phase converter is characterized by a set of normalized switching functions (s_a, s_b, s_c) , which represent the output states of the different phase legs in relation to the DC-link capacitor voltages [72]. For a two-level, three-phase inverter, the entire set of possible switching states can be represented on the α - β plane, where the contributions from phases a , b , and c provide vector components oriented along axes that are 120° apart.

The switching state $(s_a, s_b, s_c) = (1, 1, 0)$ generates a voltage vector including a component aligned with the a -axis and another component oriented at 120° from it along the b -axis. The combination of these components yields a space vector of unit magnitude positioned at an electrical angle of 60° . Thus, the eight potential switching states of a three-phase, two-level inverter constitute the vertices of a regular hexagon in the space-vector diagram. Within these states, $(0, 0, 0)$ and $(1, 1, 1)$ indicate zero-voltage vectors, both located at the origin. States that are responsible for the same position in the space-vector plane are generally termed redundant switching states.

Figure 2.10 depicts the three-phase reference voltage vector, $\mathbf{V}^*$, which traverses a circular path in the space-vector plane. The aim of space-vector modulation is to provide discrete-time approximations of the continuously rotating reference vector by properly choosing and ordering the limited set of switching vectors attainable by the converter.



(a) Space vector modulation for 2-level Converter



(b) Space vector modulation for 3-level Converters

Figure 2.10: Space vector modulation for converters. [73]

The switching states of multilevel converters can be shown within the same space-vector framework, as illustrated for two-level and three-level topologies in Fig. 2.10a and Fig. 2.10b, respectively. In each arrangement, the possible switching states occupy a hexagonal area formed by distinct voltage vectors positioned at the vertices of linked triangular sectors. Raising the number of voltage levels broadens the permissible switching states and the density of accessible switching vectors, consequently improving the accuracy of the voltage synthesis process.

In addition, the degree of switching-state redundancy grows in direct proportion to the number of voltage levels. Numerous unique switching states may produce equivalent voltage vectors within a certain region of the space-vector diagram. The modulation process gains extra degrees of freedom due to this redundancy in the space-vector formulation and the intrinsic redundancy in the phase-leg configurations [74, 75]. The flexibility of space-vector modulation provides a significant benefit, enabling advanced control purposes such as DC-link voltage balancing, reduction of switching losses, and redistribution of thermal stress in high-power multilevel converter systems.

The first phase of space-vector modulation involves sampling the rotating reference voltage vector, $\vec{v}^*$, and determining its location within the space-vector diagram in relation to the available converter switching vectors. According to this position, the space-vector modulator identifies the set of switching vectors that most accurately replicate

the reference vector [76]. Suitable redundant switching states are then identified, and the selected vectors are implemented over designated time intervals within the sampling period to ensure that their time-averaged impact replicates the intended reference voltage vector. This situation can be defined as

$$\sum_{r=1}^n d_r \vec{s}_r = \vec{v}^* \quad (2.4)$$

Here, $\vec{s}_r$ signifies the r^{th} switching vector utilized during the sampling interval, d_r indicates the proportion of the sampling period during which that vector is in use, and n specifies the total number of switching vectors utilized in the modulation sequence.

Notwithstanding its extensive use and advantageous characteristics, space-vector modulation has intrinsic limitations when utilized in high-power multilevel converters. The growing number of switching states and duplicated vectors at higher voltage levels significantly increases the computational complexity of real-time implementation and complicates the optimization of switching sequences[73]. Furthermore, the need for accurate timing computations and sector identification becomes progressively more burdensome as the number of converter levels increases. These issues prompt the exploration of alternative modulation schemes that provide reduced computational demands while preserving satisfactory harmonic performance.

2.6.4 Redundant Switching-State-Based DC-Link Voltage Balancing

The redundant switching-state-based method utilizes the intrinsic modularity of cascaded H-bridge (CHB) converters to attain DC-link voltage balancing. In multilevel CHB converters, various switching state configurations can provide identical output voltage levels owing to the existence of separate H-bridge cells. Although these duplicate states are equivalent to the synthesized phase voltage, they differ in the instantaneous current flowing through each DC-link capacitor. The charging and discharging of capacitors can be controlled by properly choosing one of these redundant switching arrangements, depending on the observed DC-link voltages.

The literature has investigated DC-link voltage balancing using several redundant switching-state approaches. A notable method attains voltage balancing by splitting the converter's operational range into multiple voltage regions. In each region, the suit-

able switching state is determined by the instantaneous voltage level and the direction of the grid current, facilitating efficient management of the DC-link voltages.

A different approach presents a redundant switching-state-based balancing technique that combines a voltage-sorting algorithm with real-time voltage-level calculations during the modulation process. This method effectively preserves cell voltage balancing under fluctuating load conditions by dynamically allocating switching states based on the observed DC-link voltages. Nonetheless, the corresponding control logic becomes more complicated as the number of cascaded cells increases, potentially limiting its scalability for advanced CHB converters [77, 78].

Alternative research has suggested using redundant switching states based on defined charging and discharging criteria while considering the direction of grid current flow. Expanding on this idea, a low-switching-frequency redundant-state-based voltage balancing method has also been documented. In this method, redundant switching arrangements are used to maintain DC-link voltage balance while synthesizing the AC output voltage [79].

Although redundant switching-state-based voltage balancing approaches are effective, their scalability to converters with several cells is problematic owing to elevated control complexity and the restricted capacity to optimize multiple objectives simultaneously. Furthermore, the majority of current methodologies depend on predetermined modulation rules and fail to exploit system predictions for the efficient management of DC-link voltage balance under dynamic operating conditions. In practical applications, these restrictions are intensified by limited sampling frequency, computational delays, and the exponential increase in permissible switching states as the number of submodules rises. Due to the consequent increase in real-time computational load, heuristic simplifications are often required, which may jeopardize dynamic performance and optimality.

2.6.5 SHE based Modulation Strategies for Multilevel Converter

Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) is categorized as a low switching frequency modulation strategy, essentially distinct from carrier-based and space-vector modulation approaches. Instead of generating the reference voltage

using high-frequency switching and time-averaged accumulation of discrete voltage vectors, SHE-PWM directly establishes the converter switching intervals to systematically remove specified low-order harmonics from the output voltage.

This feature makes SHE-PWM especially suitable for high-power cascaded H-bridge (CHB) converters, where thermal constraints and switching losses severely restrict the switching frequency of semiconductor devices. SHE-PWM facilitates harmonic reduction by using optimized switching angles instead of elevated switching frequencies, thereby ensuring compliance with harmonic standards while preserving minimal switching losses.

In SHE-PWM the multistep output waveform of a CHB converter is attained by using quarter and half-wave symmetries. The phase voltage can be represented as a Fourier series, with harmonic coefficients being nonlinear functions of a limited set of switching angles α_k , shown in equation 2.5. The SHE problem is therefore expressed as a series of transcendental equations, whereby the fundamental voltage magnitude is controlled while certain low-order harmonics—commonly the 5th, 7th, 11th, and 13th—are constrained to zero, represented by equation 2.6 [80]. In contrast to space-vector modulation, which operates in the stationary α - β reference frame and emphasizes instantaneous line-voltage synthesis, SHE-PWM is fundamentally a modulation approach that acts directly in the time domain at the fundamental frequency.

$$v(\omega t) = \sum_{\substack{n=1 \\ n=3,5,7,\dots}}^{\infty} \frac{4V_{dc}}{n\pi} \left(\sum_{k=1}^m \cos(n\alpha_k) \right) \sin(n\omega t). \quad (2.5)$$

$$\begin{aligned} \sum_{k=1}^m \cos(\alpha_k) &= M, \\ \sum_{k=1}^m \cos(5\alpha_k) &= 0, \\ \sum_{k=1}^m \cos(7\alpha_k) &= 0, \\ \sum_{k=1}^m \cos(11\alpha_k) &= 0. \end{aligned} \quad (2.6)$$

SHE-PWM presents a significant issue in cascaded H-bridge rectifiers that is absent in traditional two-level converters: the control and balancing of individual DC-link capacitor voltages. As each H-bridge cell contributes individually to the output voltage, unbal-

anced capacitor voltages effectively distort the desired voltage levels and influence harmonic performance. Furthermore, during rectifier operation, bidirectional power flow and fluctuating grid conditions can result in a persistent imbalance among the DC links in the absence of a specific balancing mechanism. Consequently, in the absence of explicit DC-link voltage balancing, SHE-driven modulation cannot guarantee accurate voltage synthesis or consistent harmonic performance in CHB-AFE systems.

Initial SHE implementations for CHB converters mostly depended on waveform symmetry and inherent charge redistribution to achieve approximate voltage balance. Although self-balancing behavior could potentially be observed under restricted operating conditions, it has proven inadequate for practical rectifier applications, especially during dynamic load fluctuations, extensive modulation index variations, or non-unity power factor operation. These limitations motivated the development of advanced SHE-PWM techniques that explicitly incorporate DC-link voltage management into the modulation process [81, 82].

A comprehensive categorization of DC-link voltage balancing schemes compatible with SHE-PWM has been presented in [83], which rigorously evaluates their suitability for application to multilevel converters, including cascaded H-bridge configurations. In the context of CHB rectifiers, these strategies can generally be described as methods that utilize supplementary degrees of freedom incorporated in SHE formulations or in the modular architecture of the converter.

A specific group of strategies enhances the SHE formulation by explicitly controlling the total net charge of each DC-link capacitor across one fundamental period. These approaches expand the Fourier series equations by including charge-balance requirements, consequently ensuring that the average capacitor current remains zero. This can be mathematically represented as equation 2.7. Despite its mathematical elegance, this method limits the number of harmonics that can be eliminated, since voltage balancing requires the sacrifice of certain degrees of freedom [84, 85, 86]. Therefore, charge-regulation-based SHE is often used in systems with a considerable number of voltage levels, where sufficient degrees of freedom are preserved.

$$\bar{i}_{C_i} \triangleq \frac{1}{T} \int_0^T i_{C_i}(t) dt = 0, \quad (2.7)$$

where T denotes the fundamental period and $i_{C_i}(t)$ represents the current of the i -th DC-link capacitor.

Another group of approaches incorporates regulated zero-sequence harmonics into the SHE formulations. Injecting certain triplen harmonics can affect the charging and discharging characteristics of individual H-bridge cells while barely impacting the line-to-line voltage quality. Although successful in certain circumstances, zero-sequence-based methods are limited by grid regulations, modulation range, and converter architecture, resulting in their infrequent use in CHB-AFE rectifiers designed for grid-connected applications [87, 88].

In terms of practicality, strategies that take advantage of redundancies in the switching-angle solutions or the converter switching states are more applicable to cascaded H-bridge rectifiers. The modular design of CHB converters allows for various switching configurations to provide identical output voltage levels. SHE-PWM naturally produces stepped voltage waveforms with repeating voltage levels, facilitating the selection of redundant switching states that influence the charging or discharging of certain DC-link capacitors. The redundant-state adjustment method has become one of the most efficient and commonly used balancing approaches for CHB rectifiers operating under SHE-PWM.

In redundancy-driven SHE mechanisms, the switching angles dictate the timing of voltage level variations, while a secondary selection logic allocates participating H-bridge cells to each voltage level according to their instantaneous DC-link voltages. It is possible to charge cells with lower voltages more frequently and discharge those with higher voltages more slowly without changing the resulting waveform of the synthesized signal. This method maintains the harmonic elimination characteristics of SHE while facilitating active adjustment of the DC-link voltage. Different implementations of this approach varies in the frequency of updating the redundancy choice; some are half-cycle-based, others are fundamental-period-based, or switching-angle-triggered.

The effectiveness of redundant-state-driven SHE-PWM for CHB rectifiers has been confirmed in several specialized investigations. Further advancements are made in this approach by incorporating redundant switching selection decisions with SHE-PWM for CHB active rectifiers, showcasing rapid voltage balancing and resilient performance dur-

ing rectifier operation in [89, 90]. These studies demonstrate that redundancy exploitation is especially advantageous for CHB-AFE systems, since it utilizes the converter's intrinsic modularity while preserving minimal switching losses.

Recent investigations have explored hybrid methodologies that integrate SHE-PWM with predictive control principles, whereby a restricted optimization problem determines switching states that correspond to a SHE waveform while reducing variations in DC-link voltage [91]. Although SHE-MPC schemes enhance dynamic performance, their computational cost escalates significantly with the number of cascaded cells, limiting their feasibility in real-time applications for high-level CHB rectifiers.

In conclusion, SHE-PWM serves as an efficient modulation foundation for cascaded H-bridge rectifiers operating in high-power, low-switching-frequency applications. Despite its fundamental-frequency operation presenting challenges in DC-link voltage balancing, the presence of extra degrees of freedom—particularly switching-state redundancy—facilitates successful voltage control when used appropriately.

2.6.6 Nearest-Level Modulation for Multilevel Converters

Nearest-level modulation (NLM), also known as nearest-level control (NLC), is a fundamental-frequency modulation technique extensively used in multilevel power converters, especially in modular multilevel converters (MMC) and cascaded H-bridge (CHB) architectures. In contrast to high-frequency PWM approaches, NLM produces stepped voltage waveforms by choosing the discrete voltage level that most accurately corresponds to the instantaneous amplitude of a sinusoidal reference signal. This feature enables the converter to function at a significant lower switching frequency, leading to decreased switching losses and enhanced efficiency in medium- and high-power applications [92, 93].

The NLM operates on the basis of a direct comparison between the reference voltage and the available discrete voltage levels that are created by the cascaded converter cells. At each sample time, the control algorithm calculates the required number of submodules or H-bridge cells to be integrated into the circuit to ensure that the generated output voltage approximately aligns with the reference waveform. The quantity of inserted cells can be calculated by applying a rounding operation to the ratio of the reference volt-

age to the DC-link voltage of each cell [94]. This technique generates a staircase output voltage waveform, with the number of levels contingent upon the quantity of cascaded cells in the converter. A CHB converter with n cells can generally produce $2n + 1$ distinct voltage levels, varying between $-nV_{dc}$ to $+nV_{dc}$.

A primary advantage of NLM is its very low switching frequency. Switching events occur only after the reference signal intersects the thresholds between neighboring voltage levels, resulting in each power device commutating only a limited number of times in each fundamental cycle. This significantly decreases the switching losses and thermal stress on semiconductor components, making NLM especially appealing for high-power converters, including medium-voltage drives, and grid-connected renewable energy converters [95, 96].

A notable attribute of NLM is its ease of implementation. The modulation technique fundamentally depends on mathematical operations like rounding, sorting, and level selection, which may be effectively executed in digital control systems. Conversely, modulation schemes like selective harmonic removal need the resolution of nonlinear transcendental equations, complicating real-time implementation. Due to its simplicity, NLM has been extensively used for converters with several voltage levels, where conventional PWM algorithms are computationally expensive [96].

Notwithstanding its simplicity and effectiveness, traditional NLM has several limitations that have spurred much study in the literature. The main concern is the modulation error caused by the converter's discrete voltage increments. Due to the output voltage being restricted to discrete values, a discrepancy always occurs between the intended reference voltage and the produced staircase waveform. This mistake is exacerbated when the quantity of accessible voltage levels is limited, resulting in higher harmonic distortion in the output voltage [97]. The modulation error is more apparent when the reference waveform nears its peak value, at which point the converter's voltage resolution is inadequate for accurately reproducing the sinusoidal waveform.

To resolve this problem, many enhanced NLM approaches have been suggested. In [98] presented an improved nearest-level modulation (INLM) technique that minimizes modulation error by modifying the operational duration of the last inserted submodule. The suggested method alters the conduction duration of the ultimate voltage level

to more accurately resemble the region of the reference sine wave, thereby enhancing voltage tracking precision and minimizing the system's power error.

A further area of study focuses on altering the switching architecture of NLM to enhance harmonic performance. The research study represented in [92] introduced a variable-structure nearest-level modulation (VSNLM) technique for cascaded H-bridge multilevel inverters. This method replaces the constant threshold used in traditional NLM for transitioning between voltage levels with an adjustable parameter that can be tuned to reduce total harmonic distortion (THD). The suggested technique enhances output voltage quality relative to standard NLM by establishing suitable switching boundaries based on the modulation index across various operating situations.

Besides harmonic performance, voltage balancing of the DC-link capacitors or energy storage modules is a crucial consideration when implementing NLM in cascaded converter configurations. Imbalances in capacitor voltage may develop over time due to varying conduction durations across various submodules during each fundamental cycle. To address this problem, sorting and selection algorithms are often included with NLM to identify which submodules should be introduced at each switching instant. These algorithms often prioritize modules with elevated or reduced voltages based on the operational mode, thereby facilitating efficient capacitor voltage balancing and enhancing converter dependability.

In Applications that utilize integrated energy storage components like supercapacitors or batteries, NLM may be modified to manage current distribution and energy allocation among submodules. Modified nearest-level control techniques have been suggested to equalize current stress among converter cells by altering the sequence of submodule activation during each fundamental cycle [99]. These methods mitigate heat stress on individual cells and enhance the longevity of energy storage components.

In summary, nearest-level modulation offers an exceptionally effective and computationally straightforward modulation approach for multilevel converters with several voltage levels. Its reduced switching frequency renders it especially appropriate for high-power applications where switching losses need to be minimized. The discrete characteristics of the produced voltage waveform result in intrinsic modulation errors and harmonic distortion, particularly when the number of levels is limited. As a result,

many enhanced NLM techniques have been developed to augment voltage tracking precision, reduce harmonic distortion, and optimize voltage equilibrium across converter cells.

In conclusion, NLM constitutes a pragmatic and extensively used modulation technique for cascaded multilevel converters, attributed to its minimal switching losses and uncomplicated implementation. Nonetheless, its constraints concerning harmonic performance and voltage balance persist in driving the development of sophisticated NLM variants and hybrid modulation approaches designed to enhance waveform quality and overall converter efficiency.

2.7 Summary

This chapter examined the scientific foundations and principal issues related to electric vehicle (EV) fast and extreme fast charging (XFC) infrastructure, focusing specifically on medium-voltage (MV) power conversion and cascaded H-bridge (CHB) active front-end (AFE) converters. The discussion was motivated by the shortcomings of traditional Level-1 and Level-2 charging systems, which are unable to satisfy the increasing demand for rapid charging intervals associated with high-capacity electric vehicle batteries. Consequently, high-power DC fast charging and XFC stations have become vital elements of future transportation electrification, necessitating converter topologies that guarantee high efficiency, scalability, and grid compatibility.

The chapter examined the XFC station topologies, including AC-bus and DC-bus systems, along with transformer-based and solid-state transformer (SST) architectures. A comparative evaluation highlighted the trade-offs among efficiency, power density, system complexity, and grid impact. Modular and distributed architectures were recognized as advantageous options for high-power charging applications because of their scalability, redundancy, and suitability for partial-power processing. In this context, multilevel converters are identified as pivotal technologies for medium-voltage front-end stages, since they enable direct medium-voltage interfacing, reduce semiconductor stress, and enhance power quality.

A comprehensive evaluation was conducted on neutral-point-clamped (NPC), flying-

capacitor (FC), and cascaded H-bridge (CHB) converters within multilevel topologies. Although each topology offers unique benefits, the CHB converter is particularly appealing for XFC applications because of its intrinsic flexibility, fault tolerance, and ability to utilize low-voltage semiconductor devices in medium-voltage systems. The existence of several independent DC connections in CHB converters presents considerable challenges in power management and DC-link voltage control, especially under the highly dynamic and uneven loading conditions typical of multi-port XFC stations.

This chapter offers an in-depth investigation of DC-link voltage balancing solutions for CHB-based AFEs, emphasizing modulation-oriented methods for addressing these challenges. High-switching-frequency multicarrier approaches, such as phase-shifted and level-shifted PWM, were examined for their harmonic performance, scalability, and intrinsic balancing capabilities. Space-vector modulation was analyzed as a versatile vector-based technique that utilizes switching-state redundancy to facilitate voltage balancing, albeit with increased computational complexity. Moreover, selective harmonic elimination PWM and nearest level modulation was introduced as a low-switching-frequency option suitable for high-power applications, where redundant switching states can be used to facilitate DC-link voltage management.

The literature demonstrates that while CHB-based XFC architectures with distributed battery energy storage provide distinct benefits—such as modular scalability, direct medium-voltage interfacing, and partial buffering of high-power transients—their operational effectiveness is significantly influenced by the employed control strategy. Architectures in which each CHB cell operates as an autonomous charging port following a DC–DC stage inevitably lead to unequal power distribution, resulting in voltage imbalances and increased stress on both power electronic devices and integrated energy storage systems. Consequently, there is a specific need for specialized control techniques designed for CHB-based XFC systems that ensure effective DC-link voltage regulation while reducing battery stress during highly dynamic multi-port charging scenarios. This need directly motivates the scientific contributions presented in the subsequent chapters.

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Chapter 3:

XFC Architecture and Mathematical Modeling

3.1 Introduction

Extreme fast-charging (XFC) stations require power conversion systems with high power density, medium-voltage grid integration capability, rapid dynamic response, and the ability to accommodate significant transient power demands arising from simultaneous multi-vehicle charging. To satisfy these requirements, multilevel converter topologies have emerged as a promising solution for next-generation fast-charging infrastructure.

Among these topologies, cascaded H-bridge (CHB) multilevel AC–DC converters integrated with distributed battery energy storage (BES) modules offer an attractive combination of modular scalability, flexible power routing, and localized energy buffering capability. In such configurations, each H-bridge cell is connected to an independent BES module, enabling the converter to operate as a set of synchronized single-phase rectifiers while partially isolating the medium-voltage grid from rapid power transients introduced by the charging ports.

This chapter investigates a three-phase star-connected multilevel cascaded H-bridge (CHB) AC–DC converter with integrated battery energy storage for extreme fast-charging (XFC) stations. The system under consideration serves as an active front-end (AFE) interface between the medium-voltage grid and the charging infrastructure, while providing distributed energy buffering through the integrated BES modules.

To this end, a control-oriented mathematical model of the CHB converter is first developed, followed by the modeling of the integrated battery energy storage modules. These models establish the foundation for the control design, DC-link voltage balanc-

ing strategy, optimization-based power management framework, and stability analysis presented in the subsequent sections.

3.2 Overview of the MV XFC Station Architecture

Figure 3.1 depicts the design of the extreme fast electric vehicle (EV) charging station examined in this study. The system is designed to interact directly with a three-phase medium-voltage (MV) grid while providing numerous high-power DC charging ports under highly dynamic operational circumstances. The station employs a cascaded H-bridge (CHB) multilevel AC-DC converter, coupled with distributed battery energy storage (BES), to meet the stringent requirements of extreme rapid charging, including high power density, flexible scalability, and minimal grid impact.

The CHB converter functions as a transformerless active front-end (AFE), synthesizing medium-voltage AC waveforms via series-connected low-voltage power cells. Each H-bridge submodule is connected to a separate battery energy storage unit, enabling localized energy buffering and partial decoupling between the grid and the charging ports. This distributed storage strategy mitigates grid-side power fluctuations caused by rapid and uneven EV charging, while also offering greater flexibility for power-flow regulation and state-of-charge (SoC) management.

Following the CHB-AFE and BES modules, isolated DC-DC conversion stages provide galvanic isolation and a regulated DC output suitable for electric vehicle battery charging. The modular design allows multiple charging ports to operate simultaneously, possibly at varying power levels, while maintaining grid current symmetry and compliance with power quality standards. Furthermore, the system's bidirectional power flow capabilities enable additional functions, including grid support and local energy management.

The integration of distributed battery energy storage (BES) modules into the cascaded H-bridge (CHB) converter significantly increases the system's complexity from both modeling and control perspectives. The presence of multiple independent DC links, combined with unequal port loading and dynamic power exchange among the converter cells, necessitates coordinated control strategies to ensure stable DC-link voltage regu-

lation, balanced power distribution, and proper battery operation.

This chapter presents a comprehensive mathematical model of the XFC station under examination. Initially, the CHB converter is represented in dq reference frames, subsequently leading to the formulation of a control-oriented averaged model appropriate for further linearization. Thereafter, the electrical and state-of-charge dynamics of the integrated battery energy storage modules are modeled, establishing the foundation for the stability analysis and control design discussed in the subsequent chapters.

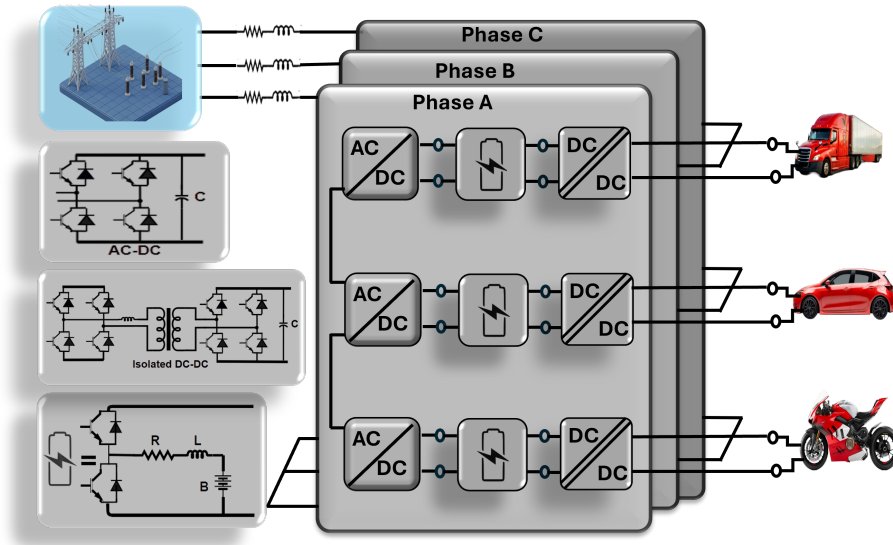


Figure 3.1: Multiport XFC charging station.

3.3 Multilevel Cascaded H-Bridge Rectifier

Figure 3.3 depicts the configuration of a three-phase 7level medium-voltage (MV) grid-connected cascaded H-bridge (CHB) rectifier, wherein each phase leg comprises 3 H-bridge cells arranged in series. Each H-bridge cell consists of four ideal power switches with antiparallel diodes, enabling bidirectional current flow and power exchange based on the applied switching state. Figure 3.2a, 3.2b, and 3.2c illustrate the switching arrangement of a single H-bridge cell for positive, negative, and zero current directions, respectively. Each H-bridge cell can produce three different voltage levels across its DC terminals: $+V_{dc}$, 0, and $-V_{dc}$, by selecting the appropriate switching states. The zero-voltage state can be attained through various redundant switching combinations, which can be used to achieve control objectives such as voltage balancing and loss reduction.

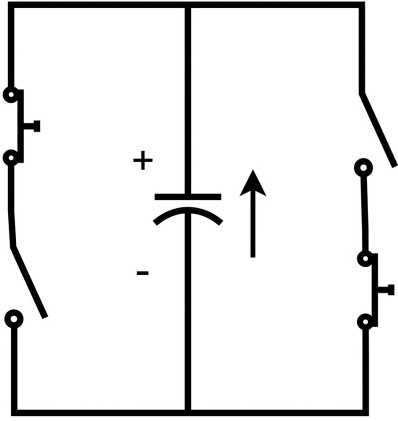
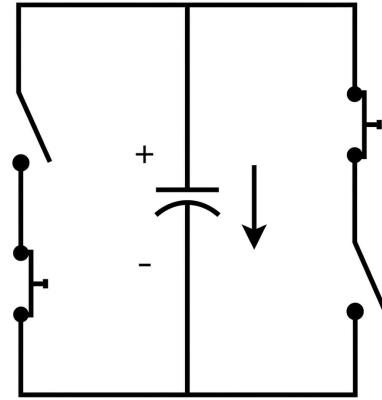
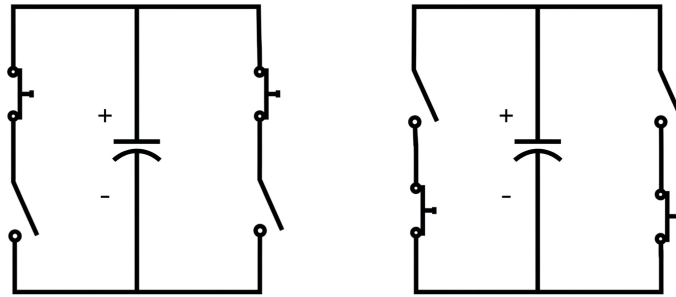
(a) Switching configuration for $+V_{dc}$ (b) Switching configuration for $-V_{dc}$ (c) Switching configuration for $0V_{dc}$

Figure 3.2: Switching configuration of CHB converter

Each Phase of the multilevel CHB converter can be modeled as a controllable voltage source that generates an alternating current (AC) waveform from a finite set of discrete voltage levels. Under balanced working conditions, each CHB cell receives an equal DC-link voltage, V_{dc} . Increasing the number of series-connected submodules improves the resolution of the generated phase voltage, yielding a waveform that more accurately resembles an ideal sinusoid.

The CHB topology has several substantial benefits. The voltage stress (dv/dt) for each semiconductor device is significantly reduced compared with a single high-voltage converter, resulting in lower switching losses and improved electromagnetic compatibility (EMC) [1]. The modular architecture enhances system maintainability and scalability, allowing individual submodules to be serviced or changed with minimum disruption. The series connection of submodules facilitates direct connecting to medium-voltage grids, eliminating the need for a heavy low-frequency transformer.

Furthermore, having the ability of various voltage levels at the converter output greatly minimizes the total harmonic distortion (THD) of the grid current. In an N -cell CHB converter, the generated phase voltage comprises $2N + 1$ unique voltage levels, considerably alleviating the filtering requirement while improving overall power quality [2, 3].

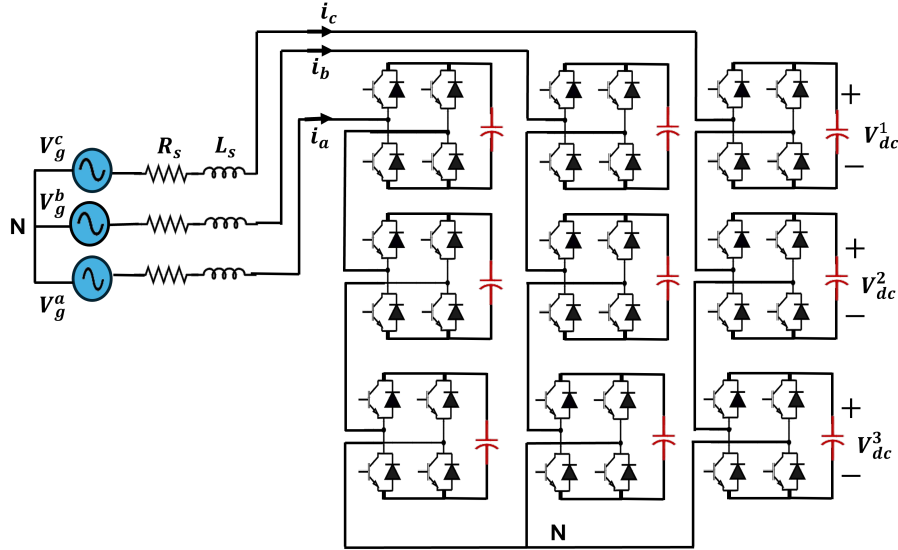


Figure 3.3: 7level CHB active front-end rectifier

3.4 Mathematical Modeling of the System

This section formulates a mathematical model for the three-phase CHB-AFE presented in Section 3.1. The developed model encapsulates the primary electrical dynamics of the AC grid-side filter, the multilevel converter, and their corresponding DC links. The formulation aims to provide a plant representation that enables the control design and closed-loop stability analysis discussed in the next chapter.

3.5 Reference Frame Transformation

For controller design, the three-phase (abc) model is transformed into the synchronously rotating (dq) reference frame using the Park transformation. This transformation converts sinusoidal variables into DC quantities under balanced operating conditions, thereby simplifying the control design. The computed (dq)-axis voltage references are subse-

quently transformed back into the three-phase (abc) reference frame using the inverse Park transformation for PWM signal generation.

3.5.1 ABC to Park Transformation

A direct transformation exists between the three-phase abc reference frame and the rotating $dq0$ reference frame. The Park transformation creates a linear correlation between instantaneous phase values and how they are represented in the rotating frame. The transition is articulated as follows;

$$\mathbf{x}^{dq0} = \mathbf{K}_p(\theta) \mathbf{x} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin \theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \mathbf{x}, \quad (3.1)$$

where $\mathbf{x} = [x_a \ x_b \ x_c]^T$ denotes the three-phase quantity in the abc reference frame.

The transformation matrix $\mathbf{K}_p$ is formulated to retain the magnitude of the space vector. Moreover, it can be shown that the determinant of $\mathbf{K}_p$ is consistently non-zero, hence guaranteeing the invertibility of the transformation. The inverse Park transformation, which translates the rotating-frame values to the phase domain, is therefore expressed as;

$$\mathbf{x} = \mathbf{K}_p^{-1}(\theta) \mathbf{x}^{dq0} = \begin{bmatrix} \cos \theta & -\sin \theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \mathbf{x}^{dq0}. \quad (3.2)$$

In balanced three-phase systems, the zero-sequence component can be ignored, as in prior transformations. Given this assumption, the Park transformation simplifies to

$$\mathbf{x}^{dq} = \mathbf{K}_p(\theta) \mathbf{x} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin \theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \mathbf{x}, \quad (3.3)$$

with the corresponding inverse relation given by

$$\mathbf{x} = \mathbf{K}_p^{-1}(\theta) \mathbf{x}^{dq} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \mathbf{x}^{dq}. \quad (3.4)$$

This dissertation will examine the Clarke and Park transformations, excluding the zero component.

3.6 Mathematical Model of CHB-AFE rectifier

This thesis examines a three-phase seven-level CHB-AFE rectifier, as shown in Fig. 2. The cascaded H-bridge converter interfaces with the three-phase AC grid via a coupling inductor and a parasitic resistance, denoted by L_{sm} and R_{sm} , respectively.

To formulate an appropriate mathematical model of the cascaded H-bridge rectifier, a simplified equivalent circuit is utilized as shown in Fig. 3.4. The AC phase voltages and currents on the grid side are represented by v_{sm} and i_{sm} , respectively, while the DC-side components are indicated by the DC-link capacitors C_{smi} and the corresponding load resistances R_{Lmi} . Based on these assumptions, the dynamic behavior of the CHB-AFE in the abc reference frame can be defined by the following set of differential equations:

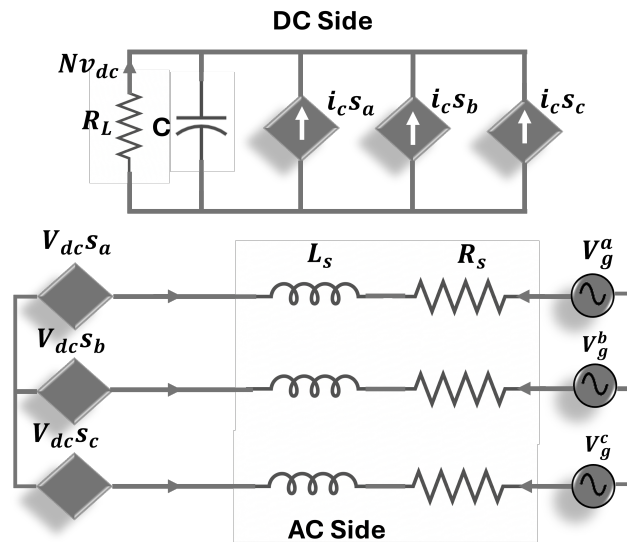


Figure 3.4: Simplified model of cascaded Hbridge

$$L_{sm} \frac{di_{sm}}{dt} = v_{sm} - R_{sm} i_{sm} - \sum_{i=1}^N s_{mi} v_{dc,mi} \quad (3.5)$$

$$C_i \frac{dv_{dc,mi}}{dt} = s_{mi} i_{sm} - \frac{v_{dc,mi}}{R_{L,mi}} \quad (3.6)$$

Where s_m denotes the continuous duty cycle associated with the H-bridge cells of the m^{th} phase, while the DC-link voltage of the i -th H-bridge cell in phase m is denoted by $v_{dc,mi}$, $m \in \{a, b, c\}$ and $i \in \{1, 2, \dots, N\}$, where N is the number of cascaded H-bridge cells per phase, which is set to $N = 3$ in this thesis. In order to facilitate the analysis of the given system, equations 3.5 and 3.6 will be transformed from the abc reference frame to the dq reference frame.

3.6.1 abc to dq Transformation of the CHB-AFE Model

The dynamic properties of the three-phase CHB-AFE are defined by (3.5). To apply dq -reference-frame transformation theory, it is crucial to represent the three-phase values (including voltages and currents) in vector form.

$$\mathbf{i}_s^{abc} = \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}, \quad \mathbf{v}_s^{abc} = \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix},$$

The synthesized phase voltages of the converter can be represented in vector form as follows:

$$\mathbf{v}_{\text{conv}}^{abc} = \begin{bmatrix} \sum_{i=1}^N s_{ai} v_{dc,ai} \\ \sum_{i=1}^N s_{bi} v_{dc,bi} \\ \sum_{i=1}^N s_{ci} v_{dc,ci} \end{bmatrix}.$$

Equation (3.5) can then be written compactly as

$$L_s \frac{d\mathbf{i}_s^{abc}}{dt} = \mathbf{v}_s^{abc} - R_s \mathbf{i}_s^{abc} - \mathbf{v}_{\text{conv}}^{abc}. \quad (3.7)$$

Introduce the Park transformation matrix to facilitate the direct transformation from

the abc to the $dq0$ reference frame. The function $\mathbf{K}_p(\theta)$ immediately translates phase values into the synchronously rotating reference frame.

$$\mathbf{I}_s^{dq0} = \mathbf{K}_p(\theta) \mathbf{i}_s^{abc}, \quad \theta = \omega t, \quad (3.8)$$

with

$$\mathbf{K}_p(\theta) = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin \theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}.$$

ignoring the zero-sequence component (balanced three-phase operation), the transformation simplifies to

$$\mathbf{I}_s^{dq} = \begin{bmatrix} I_{sd} \\ I_{sq} \end{bmatrix} = \mathbf{K}_{p,dq}(\theta) \mathbf{i}_s^{abc}.$$

Differentiating (3.8) with respect to time yields,

$$\frac{d\mathbf{I}_s^{dq}}{dt} = \mathbf{K}_{p,dq}(\theta) \frac{d\mathbf{i}_s^{abc}}{dt} + \dot{\mathbf{K}}_{p,dq}(\theta) \mathbf{i}_s^{abc}.$$

Since both the current vector and the transformation matrix are time-dependent, the product rule results in;

$$\dot{\mathbf{K}}_{p,dq}(\theta) \mathbf{K}_{p,dq}^{-1}(\theta) \mathbf{I}_s^{dq} = \omega \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} \mathbf{I}_s^{dq},$$

Likewise, the transformation is done to v_s^{abc} ; as v_s^{abc} does not contain any differential, no additional term will emerge.

$$\mathbf{V}_s^{dq} = \mathbf{K}_{p,dq}(\theta) \mathbf{v}_s^{abc} \quad (3.9)$$

The synthesized phase voltage in the abc frame must also be transformed into the dq frame. The converter voltage in the dq reference frame is derived directly as;

$$\mathbf{V}_{\text{conv}}^{dq} = \mathbf{K}_{p,dq}(\theta) \mathbf{v}_{\text{conv}}^{abc}.$$

Assuming that each cell in CHB rectifier producing the identical DC voltaeg ($V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$, which is the common average DC-link voltage V_{dc} .

$$v_{dc,mi} \approx V_{dc},$$

the phase converter voltages become

$$v_{\text{conv},m} = V_{dc} \sum_{i=1}^N s_{mi} = V_{dc} u_m, \quad m \in \{a, b, c\},$$

where u_m denotes the normalized duty cycle of a phase that is bounded between $[-3,3]$ in this case study.

Applying the Park transformation to the modulation vector

$\mathbf{u} = [u_a \ u_b \ u_c]^T$ yields

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \mathbf{K}_{p,dq}(\theta) \mathbf{u},$$

and therefore

$$v_{\text{conv},d} = V_{dc} u_d, \quad v_{\text{conv},q} = V_{dc} u_q. \quad (3.10)$$

Having transformed all three-phase values into the dq reference frame, placing these transformations into (3.7), the dq -frame current dynamics become

$$L_s \frac{d\mathbf{I}_s^{dq}}{dt} = \mathbf{V}_s^{dq} - R_s \mathbf{I}_s^{dq} - \mathbf{v}_{\text{conv}}^{dq} + L_s \omega \begin{bmatrix} I_{sq} \\ -I_{sd} \end{bmatrix}. \quad (3.11)$$

Further simplification and substitution of (3.10) into (3.11) provide the final dq -frame model:

$$L_s \dot{I}_{sd} = V_{sd} - R_s I_{sd} - V_{dc} u_d + \omega L_s I_{sq} \quad (3.12)$$

$$L_s \dot{I}_{sq} = V_{sq} - R_s I_{sq} - V_{dc} u_q - \omega L_s I_{sd}. \quad (3.13)$$

Now in (3.12) and (3.13) dividing L_s both sides yields,

$$\begin{aligned} \dot{I}_{sd} &= \frac{1}{L_s} V_{sd} - \frac{R_s}{L_s} I_{sd} - \frac{V_{dc}}{L_s} u_d + \omega I_{sq}, \\ \dot{I}_{sq} &= \frac{1}{L_s} V_{sq} - \frac{R_s}{L_s} I_{sq} - \frac{V_{dc}}{L_s} u_q - \omega I_{sd}. \end{aligned} \quad (3.14)$$

In order to obtain an accurate representation of how the capacitor voltages evolve and interact with the AC-side state variables, it is necessary to rewrite equation 3.6, even though the grid-side current dynamics can be easily presented in the synchronously rotating reference frame.

Averaged representation of the converter is used for control-oriented modeling at this level. The switching frequency is assumed to be much greater than the dominant electrical dynamics of the system, allowing for an accurate characterization of the converter's behavior via its basic components. Assuming this, the synthesized converter voltage is directly proportional to both the modulation index and the DC-link voltage. Thus, the modulation vector $\mathbf{u}_{dq}$ signifies the averaged control input inside the synchronously rotating reference frame, facilitating the implementation of the instantaneous power equilibrium between the AC and DC sides of the converter.

$$\mathbf{P}_{in} = \mathbf{P}_o \quad (3.15)$$

The instantaneous active power in the dq reference frame can be expressed as follows:

$$P_{in} = \frac{3}{2} (V_{sd} I_{sd} + V_{sq} I_{sq}) \quad (3.16)$$

Simultaneously, the cumulative active power output on the DC side can be expressed as follows:

$$P_o = N V_{dc} I_{dc} \quad (3.17)$$

Where, N is total number of H-bridges substituting (3.16) and (3.17) in (3.15) and solving for I_{dc} yields,

$$I_{dc} = \frac{\frac{3}{2} (V_{sd} I_{sd} + V_{sq} I_{sq})}{N V_{dc}} \quad (3.18)$$

In a multilevel converter, the amplitude of the fundamental reference voltage vector is directly proportional to the modulation index multiplied by the DC link voltage of the bridge. In a cascaded H-bridge inverter with N bridges per phase, the total phase fundamental voltage reference is the aggregate of all bridge contributions, resulting in;

$$V_{sd} = u_d V_{dc} N, \quad V_{sq} = u_q V_{dc} N \quad (3.19)$$

By inserting (3.19) into (3.18) and simplifying, (3.18) is transformed into

$$I_{dc} = \frac{3}{2} (u_d I_{sd} + u_q I_{sq}) \quad (3.20)$$

Given that the current across the capacitor is exactly proportional to the rate of change of voltage over time, equation (3.6) can be represented as follows:

$$C \frac{dv_{dc}}{dt} = I_{dc} - i_L \quad (3.21)$$

Where; i_L denotes the load current, and by inserting (3.20) into (3.21), results in the final transformation of the DC-link voltage dynamics in the dq reference frame.

$$\dot{V}_{dc} = \frac{3}{2C} (u_d I_{sd} + u_q I_{sq}) - \frac{V_{dc}}{R_L C} \quad (3.22)$$

Furthermore, given the constant power demand, which is assumed in this situation, the 3.22 can be expressed as

$$\dot{V}_{dc} = \frac{3}{2C} (u_d I_{sd} + u_q I_{sq}) - \frac{i_L}{C} \quad (3.23)$$

The complete CHB converter model in the synchronously rotating dq reference frame is delineated by (3.14) and (3.23).

A simplified averaged dynamic model of the cascaded H-bridge (CHB) converter has been derived from the following calculations. This model delineates the dynamics of

AC-side current and the progression of DC-link voltage, while neglecting the influence of switching harmonics.

3.7 Battery Energy Storage (BES) Module

The battery energy storage (BES) module, seen in fig 3.5, is connected into each cell of the multilevel cascaded H-bridge (CHB) converter via an auxiliary power electronic interface. This interface is often implemented as a non-isolated bidirectional DC-DC buck converter, as seen in Fig. 3.1.

A two-stage cascaded H-bridge (CHB) inverter configuration using bidirectional step-up DC-DC converters has been examined in the literature, as noted in [4]. This technique proposes a specialized control mechanism for DC-DC converters to mitigate DC-link voltage variations across diverse operating conditions. The system can accommodate the failure of individual submodules by supporting a variable DC-link voltage, enabling operation with fewer cells at elevated DC-link voltages.

A module-level cascaded H-bridge (CHB) inverter with integrated battery energy storage has been developed for distributed photovoltaic (PV) systems, in which a battery unit is placed in each power cell to facilitate distributed energy buffering and alleviate PV mismatch effects [5]. This design enhances power harvesting and mitigates the inherent intermittency of photovoltaic generation, yielding a more consistent output power profile.

These studies collectively illustrate that incorporating battery energy storage (BES) at the power-cell level is crucial for improving the operational flexibility, fault tolerance, and power quality of multilevel cascaded H-bridge (CHB) converter systems. Embedding energy storage in each converter cell enables the realization of sophisticated control functions—such as DC-link voltage regulation, power decoupling, and energy buffering—in a distributed manner via coordinated power electronic interfaces. The effectiveness of these systems fundamentally relies on precise battery modeling and reliable state-of-charge (SoC) prediction, since inadequate SoC management may lead to uneven power distribution, accelerated battery degradation, and reduced system longevity. This part delineates the battery modeling methodology and proposes a Coulomb-counting-based

State of Charge (SoC) estimation framework appropriate for real-time applications in Cascaded H-Bridge (CHB)- integrated Battery Energy Storage (BES) systems.

3.7.1 Battery Modeling and SoC Estimation

This thesis employs a simpler, control-oriented battery model, as seen in (??). The battery is modeled as a controlled open-circuit voltage source, referred to as U_{OC} , in series with an equivalent internal resistance R_{bat} . This model accurately represents the primary electrical characteristics of the battery during charging and discharging, while ensuring minimal computing complexity, thereby rendering it appropriate for real-time control and system-level evaluation.

The open-circuit voltage U_{OC} is often a nonlinear function of the battery state of charge (SoC), whereas the series resistance R_{bat} represents ohmic losses and voltage reductions due to current flow. This comparable circuit model, despite its simplicity, is extensively used in power electronic applications because of its effectiveness in representing the steady-state and low-frequency dynamic properties of battery energy storage systems [6].

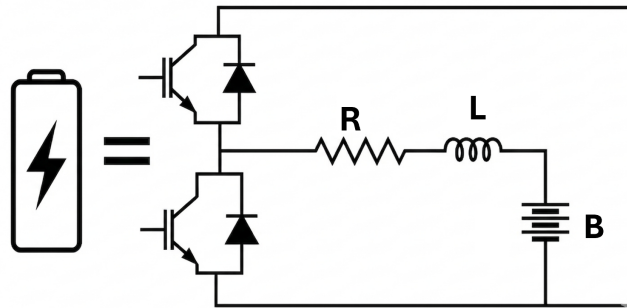


Figure 3.5: Battery energy storage module.

The state of charge is approximated using the Coulomb counting approach, which calculates the SoC by integrating the battery current over time, based on this battery representation [7]. This method is straightforward and especially appropriate for converter-interfaced battery systems, because the battery current is immediately observable and can be precisely regulated. The mathematical formulation for State of Charge (SoC) estimate using coulomb counting, assuming a room temperature of $25^{\circ}C$, is as follows:

$$s(t) = s(0) + \frac{\eta}{3600 C_{\text{batt}}} \int_0^t i(t) dt \quad (3.24)$$

where η is the Coulomb-counting efficiency, defined as

$$\eta = \begin{cases} \eta_c, & i(t) > 0 \\ \eta_d, & i(t) < 0, \end{cases} \quad (3.25)$$

Let t signify time in seconds, $i(t)$ denote the battery current in amperes (A) at time t , $s(0)$ represent the starting state of charge at $t = 0$, and $s(t)$ indicate the state of charge at time t . The parameter C_{batt} signifies the nominal battery capacity in ampere-hours (Ah), whereas η_c and η_d imply the Coulombic efficiencies throughout the charging and discharging processes, respectively.

3.8 Summary

This chapter presented the design and control-oriented mathematical modeling of a medium-voltage extreme fast-charging (XFC) station based on a cascaded H-bridge (CHB) active front-end rectifier with integrated battery energy storage. The system architecture was first introduced, emphasizing the role of distributed battery modules in enabling modular scalability, grid decoupling, and flexible power-flow regulation. A comprehensive mathematical model of the CHB-AFE was then developed and expressed in the synchronously rotating (dq) reference frame for control design and dynamic analysis. The DC-link voltage dynamics were derived using an averaged power-balancing approach. In addition, a control-oriented battery model and a Coulomb-counting-based state-of-charge estimation approach were introduced to describe the electrical and energy dynamics of the integrated BES modules. The developed models provide the analytical foundation for the small-signal stability analysis and the optimization-based control strategy presented in the following chapter.

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Chapter 4:

Optimal Control of Cascaded Hbridge with Integrated BES For XFC Station

4.1 Introduction

This chapter presents the control architecture developed for the cascaded H-bridge (CHB)-based extreme fast-charging (XFC) station with integrated battery energy storage (BES). The proposed control system is based on the control-oriented mathematical models obtained in Chapter 3; it aims to stabilize grid interfacing, regulate DC-link operation, and provide coordinated control of the distributed BES modules under extremely dynamic charging conditions.

Because of the modular design of the CHB converter and the existence of a series of independent DC links with embedded energy storage, a hierarchical control structure is used. At the primary control level, a fast inner current control loop and an outer average DC-link voltage control loop are used to ensure the quality of the grid current, unity power factor operation, and stable power exchange with the medium-voltage grid. Small-signal modeling is used to analyze the dynamic interaction between the grid-side control loops and the DC-link dynamics in order to determine closed-loop stability and select appropriate control parameters.

In addition to the primary control, the distributed characteristics of the BES provide additional degrees of freedom for power flow and energy management. A secondary control layer is therefore designed to provide optimal battery power to each BES module integrated with the CHB while considering CHB operational limits. This is formulated as a constrained optimization problem, and its solution is determined through quadratic programming (QP), which allows systematic minimization of battery stress and SoC imbalance without compromising overall system feasibility.

The chapter proceeds by first establishing a hierarchical control structure that coordinates the operation of the grid-side converter and the distributed battery energy storage modules. Based on this, the structure of the main control loops that regulate grid current and are responsible for stabilizing the average DC-link voltage is formulated, and the closed-loop dynamics are studied using small-signal stability analysis. Lastly, an optimum energy management scheme for the BES modules is developed, where battery power references are calculated within operational constraints through a quadratic programming-based optimization model.

4.2 Equilibrium Points and Steady-State Conditions

To examine the steady-state behavior and stability characteristics of the CHB-based active front-end (CHB-AFE) for an extreme fast-charging (XFC) station, it is essential to describe the system's equilibrium points. The equilibrium points represent stable operating conditions when the converter delivers the necessary active power to the load while sustaining the DC-link voltage at its designated reference level.

The averaged modeling framework established in Chapter 3 captures the dynamics of the CHB-AFE in the synchronous (d, q) reference frame, effectively representing the low-frequency behavior of the converter for steady-state and small-signal analysis. Figure 4.1 illustrates the corresponding averaged model of the CHB-AFE.

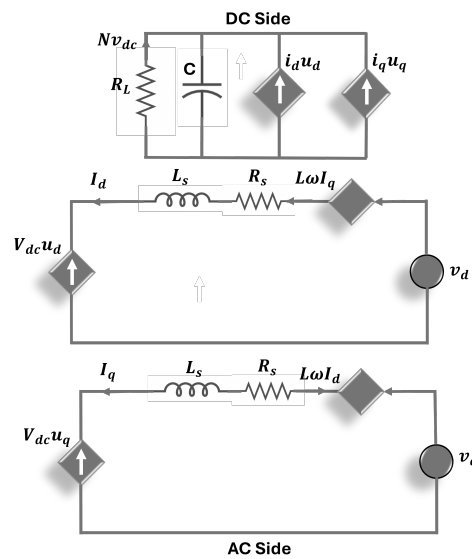


Figure 4.1: Average model of CHB-AFE in dq reference frame

$$\begin{aligned}
\dot{I}_{sd} &= -\frac{R_s}{L_s} I_{sd} + \omega I_{sq} - \frac{V_{dc}}{L_s} u_d + \frac{V_{sd}}{L_s}, \\
\dot{I}_{sq} &= -\frac{R_s}{L_s} I_{sq} - \omega I_{sd} - \frac{V_{dc}}{L_s} u_q + \frac{V_{sq}}{L_s}, \\
\dot{V}_{dc} &= \frac{3}{2C} (u_d I_{sd} + u_q I_{sq}) - \frac{i_L}{C}.
\end{aligned} \tag{4.1}$$

Since the average model of the CHB converter has been established to represent the cascaded H-bridge at its reference values, it is essential to determine the steady-state values. An equilibrium point is characterized as a stable operating condition of the system in which the time derivatives of all state variables are equal to zero. Identifying these operating points is crucial for defining the nominal behavior of the system and serves as the foundation for further small-signal modeling, linearization, and stability analysis.

The steady-state operating values of I_{sd} , u_d , and u_q can be obtained by substituting the reference values of V_{sd} , V_{sq} , I_{sq} , and V_{dc} into (4.1) and by imposing the equilibrium condition, specifically by equating all state derivatives to zero.

$$\begin{aligned}
0 &= \frac{1}{L_s} V_{sd}^* - \frac{R_s}{L_s} I_{sd} - \frac{V_{dc}^*}{L_s} u_d \\
0 &= \frac{1}{L_s} V_{sq}^* - \frac{R_s}{L_s} I_{sq}^* - \frac{V_{dc}^*}{L_s} u_q - \omega I_{sd}. \\
0 &= \frac{3}{2} (u_d I_{sd} + u_q I_{sq}^*) - \frac{i_L}{C}
\end{aligned} \tag{4.2}$$

Given that the XFC station is mostly intended to operate at a unity power factor, the q -axis voltage and current components are zero, namely, $V_{sq} = 0$ and $I_{sq} = 0$. When these conditions are substituted into (4.2), the equilibrium equations can be simplified to this form:

$$\begin{aligned}
0 &= \frac{1}{L_s} V_{sd}^* - \frac{R_s}{L_s} I_{sd} - \frac{V_{dc}^*}{L_s} u_d, \\
0 &= -\frac{V_{dc}^*}{L_s} u_q - \omega I_{sd}. \\
0 &= \frac{3}{2} u_d I_{sd} - \frac{i_L}{C}
\end{aligned} \tag{4.3}$$

The steady-state values I_{sd} , u_d , and u_q can be determined by directly resolving the system of equations (4.3).

$$u_{d,ss} = \frac{1}{2V_{dc}^*} \left(V_{sd}^* + \sqrt{(V_{sd}^*)^2 - \frac{8}{3}R_s V_{dc}^* i_L} \right) \quad (4.4)$$

$$u_{q,ss} = -\frac{L_s \omega}{2R_s V_{dc}^*} \left(V_{sd}^* - \sqrt{(V_{sd}^*)^2 - \frac{8}{3}R_s V_{dc}^* i_L} \right) \quad (4.5)$$

$$I_{sd,ss} = \frac{V_{sd}^* \pm \sqrt{(V_{sd}^*)^2 - \frac{8}{3}R_s V_{dc}^* i_L}}{2R_s} \quad (4.6)$$

Determining the steady-state equilibrium equations produces a quadratic expression in I_{sd} , as shown in (4.6), which yields two analytical solutions. The steady-state modulation variables $u_{d,ss}$ and $u_{q,ss}$ are specified in (4.4) and (4.5), respectively. Nevertheless, not all mathematical solutions correspond to physically permissible operating points of the converter.

While the steady-state equations provide two algebraic solutions for $I_{sd,ss}$, only one is physically acceptable. In particular, the modulation variables u_d and u_q are inherently bounded by the converter structure; that is, $|u_d| \leq 1$ and $|u_q| \leq 1$. Substituting the solution corresponding to the positive root of $I_{sd,ss}$ into the steady-state modulation equation results in a modulation requirement that violates these structural limitations by exceeding the permissible range. This situation corresponds to over-modulation and is therefore not physically achievable. Consequently, the equilibrium associated with the positive root cannot be achieved in practice and is excluded from further analysis, while the remaining solution is retained as the physically meaningful steady-state operating point.

by substituting the steady-state values stated by equations (4.4), (4.5), and (4.6) into the system equations from (4.1), the average model of the CHB-AFE in steady states can be expressed as follows:

$$\begin{aligned} \dot{I}_{sd} &= -\frac{R_s}{L_s} I_{sd,ss} + \omega I_{sq} - \frac{V_{dc}}{L_s} u_{d,ss} + \frac{V_{sd}}{L_s}, \\ \dot{I}_{sq} &= -\frac{R_s}{L_s} I_{sq} - \omega I_{sd,ss} - \frac{V_{dc}}{L_s} u_{q,ss} + \frac{V_{sq}}{L_s}, \\ \dot{V}_{dc} &= \frac{3}{2C} (u_{d,ss} I_{sd,ss} + u_{q,ss} I_{sq}) - \frac{i_L}{C}. \end{aligned} \quad (4.7)$$

4.3 Nonlinearity of the Averaged Model

The averaged equivalent circuit model of the CHB converter shown in ??, although simplified relative to the switching model, retains its intrinsic nonlinearity. This nonlinearity arises from the inclusion of multiplicative terms that include state variables and control inputs in both the ac and dc subsystems, as seen in equations 4.7.

On the ac side, the modulation process generates the converter output voltages in the synchronous reference frame as follows: $v_{d,q} = u_{d,q,ss} V_{dc}$, where V_{dc} is the dc-link voltage and $u_{d,ss}$, $u_{q,ss}$ are the modulation variables. The modulation variables multiply a state variable, resulting in bilinear dynamics that violate the superposition principle, which is essential for linear systems. At the same time, on the DC side, the dynamics of the DC-link capacitor are determined by the power balance between the AC and DC subsystems. The current flowing into the dc-link capacitor can be articulated as $i_{dc} = \frac{3}{2} (u_{d,ss} I_{sd,ss} + u_{q,ss} I_{sq,ss})$, which incorporates further multiplicative factors between the modulation variables and the ac-side currents. The dynamics of the dc-link voltage exhibit nonlinear coupling between state and input variables.

Due to the presence of these bilinear terms, the averaged model cannot be represented as a linear time-invariant system. Therefore, to facilitate the implementation of classical and optimization-based control methods, the nonlinear system must be linearized around a steady-state operating point.

4.3.1 Linearization Theory

Consider the general nonlinear system model shown below:

$$\begin{aligned}\dot{x}_1 &= f_1(x_1, x_2, \dots, x_m, u_1, u_2, \dots, u_n, d_1, d_2, \dots, d_p), \\ \dot{x}_2 &= f_2(x_1, x_2, \dots, x_m, u_1, u_2, \dots, u_n, d_1, d_2, \dots, d_p), \\ &\vdots \\ \dot{x}_m &= f_m(x_1, x_2, \dots, x_m, u_1, u_2, \dots, u_n, d_1, d_2, \dots, d_p).\end{aligned}\tag{4.8}$$

The system of equations presented in (4.8) consists of m state equations, n reference

inputs, and d disturbance inputs. It may be expressed in a more concise manner as;

$$\dot{x} = f(x, u, d). \quad (4.9)$$

When the system delineated in (4.9) achieves equilibrium, the state derivatives become zero, and the system is said to be in a state of equilibrium. This situation can be articulated as

$$0 = f(\bar{x}, \bar{u}, \bar{d}), \quad (4.10)$$

where the overline signifies steady-state values.

If the variables x , u , and d are sufficiently close to their steady-state values $\bar{x}$, $\bar{u}$, and $\bar{d}$, they can be expressed as

$$x = \bar{x} + \Delta x, \quad u = \bar{u} + \Delta u, \quad d = \bar{d} + \Delta d. \quad (4.11)$$

Substituting (4.11) into (4.9) yields

$$\frac{d}{dt}(\bar{x} + \Delta x) = f(\bar{x} + \Delta x, \bar{u} + \Delta u, \bar{d} + \Delta d). \quad (4.12)$$

Recalling the steady-state condition in (4.10) and applying a first-order Taylor expansion of the nonlinear function $f(\cdot)$ around the equilibrium point $(\bar{x}, \bar{u}, \bar{d})$, (4.12) can be represented as

$$\Delta \dot{x} = \bar{A} \Delta x + \bar{B} \Delta u + \bar{G} \Delta d. \quad (4.13)$$

The matrices $\bar{A}$, $\bar{B}$, and $\bar{G}$ are the Jacobian matrices of the system determined at the steady-state operating point, defined as follows

$$\bar{A} = \left[\begin{array}{ccc} \frac{\partial f_1}{\partial x_1} & \cdots & \frac{\partial f_1}{\partial x_m} \\ \vdots & \ddots & \vdots \\ \frac{\partial f_m}{\partial x_1} & \cdots & \frac{\partial f_m}{\partial x_m} \end{array} \right] \bigg|_{(\bar{x}, \bar{u}, \bar{d})}, \quad (4.14)$$

$$\bar{B} = \left[\begin{array}{ccc} \frac{\partial f_1}{\partial u_1} & \cdots & \frac{\partial f_1}{\partial u_n} \\ \vdots & \ddots & \vdots \\ \frac{\partial f_m}{\partial u_1} & \cdots & \frac{\partial f_m}{\partial u_n} \end{array} \right] \bigg|_{(\bar{x}, \bar{u}, \bar{d})}, \quad (4.15)$$

$$\bar{G} = \left[\begin{array}{ccc} \frac{\partial f_1}{\partial d_1} & \cdots & \frac{\partial f_1}{\partial d_p} \\ \vdots & \ddots & \vdots \\ \frac{\partial f_m}{\partial d_1} & \cdots & \frac{\partial f_m}{\partial d_p} \end{array} \right] \bigg|_{(\bar{x}, \bar{u}, \bar{d})}. \quad (4.16)$$

The system is linearized around the steady-state operating point, and its local stability is determined by examining the eigenvalues of the matrix $\bar{A}$ [1]. The derived linearized model is valid only within the vicinity of the chosen equilibrium point. Consequently, the Jacobian matrix $\bar{A}$ must be recalculated if the steady-state operating point changes.

4.3.2 Operating Point of the CHB Converter

As explained previously, the CHB-AFE converter model is nonlinear; therefore, classical control techniques can only be used after linearizing the model around a selected steady-state operating point. Consequently, small-signal perturbations are applied to the state, input, and disturbance variables of the CHB-AFE converter. The state vector of the CHB-AFE converter is defined as

$$x = \begin{bmatrix} I_{sd} & I_{sq} & V_{dc} \end{bmatrix}^T. \quad (4.17)$$

Small-signal perturbations around the steady-state operating point are introduced as

$$x = \bar{x} + \Delta x, \quad (4.18)$$

where

$$\Delta x = \begin{bmatrix} \Delta I_{sd} & \Delta I_{sq} & \Delta V_{dc} \end{bmatrix}^T, \quad (4.19)$$

and $\bar{x}$ denotes the steady-state value of the state vector. Similarly, the control input and disturbance vectors are defined as

$$u = \begin{bmatrix} u_d & u_q \end{bmatrix}^T, \quad d = \begin{bmatrix} V_{sd} & V_{sq} \end{bmatrix}^T, \quad (4.20)$$

with the corresponding small-signal perturbations

$$u = \bar{u} + \Delta u, \quad d = \bar{d} + \Delta d, \quad (4.21)$$

where

$$\Delta u = \begin{bmatrix} \Delta u_d & \Delta u_q \end{bmatrix}^T, \quad \Delta d = \begin{bmatrix} \Delta v_{sd} & \Delta v_{sq} \end{bmatrix}^T. \quad (4.22)$$

Inserting the aforementioned expressions into the averaged nonlinear model and discarding higher-order terms results in the linearized small-signal representation of the CHB-AFE converter, which can be expressed as.

$$\begin{aligned} \Delta \dot{I}_{sd} &= -\frac{R_s}{L_s} \Delta I_{sd} + \omega \Delta I_{sq} - \frac{\bar{u}_d}{L_s} \Delta V_{dc} - \frac{\bar{V}_{dc}}{L_s} \Delta u_d + \frac{1}{L_s} \Delta v_{sd}, \\ \Delta \dot{I}_{sq} &= -\omega \Delta I_{sd} - \frac{R_s}{L_s} \Delta I_{sq} - \frac{\bar{u}_q}{L_s} \Delta V_{dc} - \frac{\bar{V}_{dc}}{L_s} \Delta u_q + \frac{1}{L_s} \Delta v_{sq}, \\ \Delta \dot{V}_{dc} &= \frac{3}{2C} \left(\bar{u}_d \Delta I_{sd} + \bar{u}_q \Delta I_{sq} + \bar{I}_{sd} \Delta u_d + \bar{I}_{sq} \Delta u_q \right) - \frac{P_L}{C \bar{V}_{dc}^2} \Delta V_{dc}. \end{aligned} \quad (4.23)$$

In a standard state-space form, the linearized small-signal model of the CHB-AFE converter can be expressed as

$$\Delta \dot{x} = \bar{A} \Delta x + \bar{B} \Delta u + \bar{G} \Delta d, \quad (4.24)$$

where

$$\Delta x = \begin{bmatrix} \Delta I_d \\ \Delta I_q \\ \Delta V_{dc} \end{bmatrix}, \quad \Delta u = \begin{bmatrix} \Delta u_d \\ \Delta u_q \end{bmatrix}, \quad \Delta d = \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix}. \quad (4.25)$$

The state matrix is given by

$$\bar{A} = \begin{bmatrix} -\frac{R_s}{L_s} & \omega & -\frac{\bar{u}_d}{L_s} \\ -\omega & -\frac{R_s}{L_s} & -\frac{\bar{u}_q}{L_s} \\ \frac{3}{2C}\bar{u}_d & \frac{3}{2C}\bar{u}_q & -\frac{P_L}{C\bar{V}_{dc}^2} \end{bmatrix}. \quad (4.26)$$

Considering $\bar{V}_{dc}^*$ and $\bar{I}_{sq}^*$ are reference value, the input matrix can be expressed as

$$\bar{B} = \begin{bmatrix} -\frac{\bar{V}_{dc}^*}{L_s} & 0 \\ 0 & -\frac{\bar{V}_{dc}^*}{L_s} \\ \frac{3}{2C}\bar{I}_{sd} & \frac{3}{2C}\bar{I}_{sq}^* \end{bmatrix}. \quad (4.27)$$

The disturbance matrix is

$$\bar{G} = \begin{bmatrix} \frac{1}{L_s} & 0 \\ 0 & \frac{1}{L_s} \\ 0 & 0 \end{bmatrix}. \quad (4.28)$$

4.4 Control Design of Linearized CHB-AFE System

A small-signal linear time-invariant (LTI) model that offers an appropriate framework for systematic controller synthesis was produced by linearizing the nonlinear dynamics of the CHB-AFE around a steady-state operating point in the earlier section. Classical linear control methods can be utilized to control the grid currents and the DC-link voltage, assuring closed-loop stability around the chosen operating point, as shown in (4.25).

The current dynamics and the DC-link voltage dynamics have different dynamic time scales, therefore a traditional Voltage-Oriented Control (VOC) approach is employed. This method utilizes a cascaded control architecture including an outer DC-link voltage control loop and an inner current control loop. The inner loop facilitates fast control of grid currents, while the outer loop sustains the average DC-link voltage at its prede-

fined reference value by producing the corresponding current reference. The design and analysis of each control loop are detailed in the subsequent subsections.

4.4.1 PI Controller

In CHB converter applications, whether functioning as a grid-connected Battery Energy Storage (BES) system or as an active front-end (AFE) rectifier, precise regulation of both the grid current and the DC-link voltage is essential for stable and reliable operation. The existing control ensures appropriate power transfer with the grid, while DC-link voltage regulation maintains the necessary energy balance inside the converter.

The control goals are accomplished by proportional–integral (PI) controllers, owing to their simplicity, robustness, and efficacy in controlling linearized converter dynamics. Consequently, before their implementation, the structure and dynamic attributes of the PI controllers are briefly examined to provide the groundwork for the ensuing control design.

A Proportional–Integral (PI) controller is a feedback control technique often used in power electronic converters because of its simplicity and efficacy in controlling linear time-invariant systems. The controller functions by processing the error signal, which is defined as a difference between a reference value and the measured output.

$$e(t) = r(t) - y(t), \quad (4.29)$$

where $r(t)$ denotes the reference signal and $y(t)$ represents the measured variable.

The control action produced by the PI controller has two elements: a proportional term and an integral term. The time-domain model of the Proportional-Integral controller is expressed as

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau, \quad (4.30)$$

where K_p and K_i represent the proportional and integral gains, respectively.

The proportional term, $K_p e(t)$, delivers an instantaneous response that is directly proportionate to the current error value, therefore improving transient response and strengthening system responsiveness. The integral term, $K_i \int e(t) dt$, aggregates the er-

ror across time and functions to completely eliminate steady-state offset by driving the average error towards zero.

Figure 4.2 illustrates the PI controller in the Laplace domain, while mathematically it can be represented as

$$G_{PI}(s) = K_p + \frac{K_i}{s} = \frac{K_p s + K_i}{s}. \quad (4.31)$$

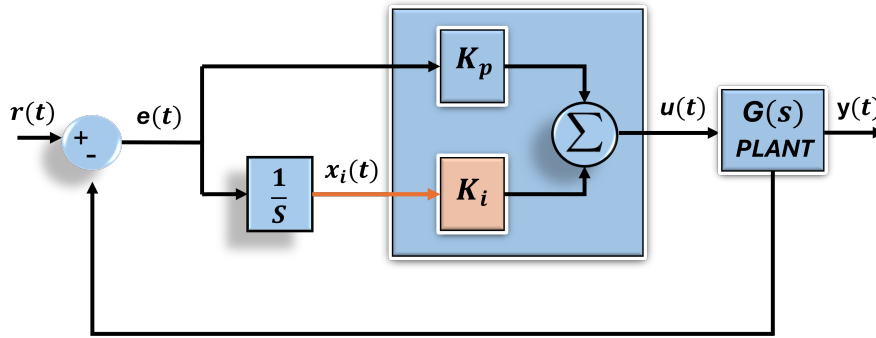


Figure 4.2: Block Diagram of the PI Controller

The transfer function indicates that the PI controller adds a pole at the origin and a zero at $s = -\frac{K_i}{K_p}$. The pole at the origin guarantees zero steady-state error for step references in stable closed-loop systems, while the zero can be strategically positioned to enhance dynamic performance and phase [2].

In the CHB-AFE rectifier, the DC-link voltage and current are attained by producing the control inputs u_d and u_q , which are used in the modulation stage. By appropriately regulating these control variables, the converter generates the necessary voltage components to attain the specified current references in a steady state.

Given that the converter functions with sinusoidal three-phase values, direct PI control in the stationary reference frame would provide inadequate performance. Consequently, the synchronous dq transformation is used, keeping the basic current components invariant under steady-state circumstances. This enables the PI controllers to manage the currents efficiently.

4.4.2 Inner Current Control Loop

The dq -axis currents i_d and i_q of the CHB-AFE converter are controlled to specified reference values using PI controllers. In the synchronous dq transformation, the d -axis is oriented with the grid voltage vector. The d -axis current i_d directly regulates the active power exchanged with the grid, whereas the q -axis current i_q is responsible for the reactive power component.

In grid-connected CHB-AFE systems, operation at unity power factor is often required. Consequently, the reference value for the q -axis current is established at zero, i.e., $i_q^* = 0$. However, this reference may be modified if reactive power assistance is necessary.

The inner current control loop regulates the dq -axis currents to their predefined reference values. The dynamic behavior of the currents is regulated by the small-signal state equations previously established in (4.23). To provide clarity, these equations are reformulated in the Laplace domain.

Under the assumption of small perturbations and the use of the Laplace transform, the dynamics of the d - and q -axis currents can be articulated as

$$sL_s\Delta I_{sd}(s) = -R_s\Delta I_{sd}(s) + \omega\Delta I_{sq}(s) - \bar{u}_d\Delta V_{dc} - \bar{V}_{dc}\Delta U_d(s) + \Delta v_{sd} \quad (4.32)$$

$$sL_s\Delta I_{sq}(s) = -\omega\Delta I_{sd}(s) - R_s\Delta I_{sq}(s) - \bar{u}_q\Delta V_{dc} - \bar{V}_{dc}\Delta U_q(s) + \Delta v_{sq} \quad (4.33)$$

For the current controller design, the DC-link voltage is assumed to be a constant value, so that $\Delta V_{dc} \approx 0$. Furthermore, the grid voltage disturbances Δv_{sd} and Δv_{sq} are considered external disturbances and are, therefore, excluded in the formulation of the control-oriented plant model.

Additionally, typical decoupling compensation is used to eliminate the cross-coupling terms $\omega\Delta I_{sq}$ and $\omega\Delta I_{sd}$. This is accomplished by including the relevant feedforward terms into the control law. Given these assumptions, the dynamics of the d - and q -axis currents become decoupled and can be analyzed separately as first-order systems for the purpose of controller design.

Under these assumptions, the d -axis current dynamics reduce to

$$\left(s + \frac{R_s}{L_s}\right) \Delta I_{sd}(s) = -\bar{v}_{dc} \Delta U_d(s), \quad (4.34)$$

The plant demonstrates a negative static gain as seen in (4.34,) because of the chosen sign convention in the converter voltage equation. The negative sign does not impact the system dynamics or pole placement; instead, it affects the feedback polarity inside the control loop.

For convenience in controller design, the control input is redefined as

$$\bar{V}_{dc} = -\bar{V}_{dc} u_d, \quad (4.35)$$

such that the small-signal model can be expressed with positive gain. According to this formulation, the open-loop transfer function relating the control input $\Delta U_d(s)$ to the output current $\Delta I_{sd}(s)$ is derived as

$$G_{id}(s) = \frac{\Delta I_{sd}(s)}{\Delta U_d(s)} = \bar{V}_{dc} \frac{1}{s + \frac{R_s}{L_s}}. \quad (4.36)$$

Similarly, the q -axis open-loop transfer function is given by

$$G_{iq}(s) = \frac{\Delta I_{sq}(s)}{\Delta U_q(s)} = \bar{V}_{dc} \frac{1}{s + \frac{R_s}{L_s}}. \quad (4.37)$$

These formulae indicate that, after decoupling, the current dynamics can be modeled as first-order systems with a pole situated at $-\frac{R_s}{L_s}$. This simplified depiction serves as the foundation for the construction of the PI current controllers. The transfer function of the q -axis current $G_{iq}(s)$ is identical to that of the d -axis current $G_{id}(s)$, therefore, the open-loop and closed-loop configurations are consistent for both axes.

The d -axis current is controlled to its specified reference value using a proportional-integral (PI) controller, as described by the transfer function in (4.31). The output of the PI controller directly specifies the duty cycle implemented in the converter, which can be represented as

$$\Delta U_d^*(s) = K_p (I_{sd}^* - I_{sd}) + \frac{K_i}{s} (I_{sd}^* - I_{sd}) \quad (4.38)$$

$$\Delta U_q^*(s) = K_p (I_{sq}^* - I_{sq}) + \frac{K_i}{s} (I_{sq}^* - I_{sq}) \quad (4.39)$$

By inserting (4.38) and (4.39) into the open-loop current dynamics described in (4.36) and (4.37), the resultant closed-loop current dynamics are derived. The resultant closed-loop control configuration for I_{sd} is shown in figure 4.3. The transfer function for I_{sq} has the same form, resulting in a block diagram with a similar structure. The corresponding closed-loop transfer function can therefore be defined as

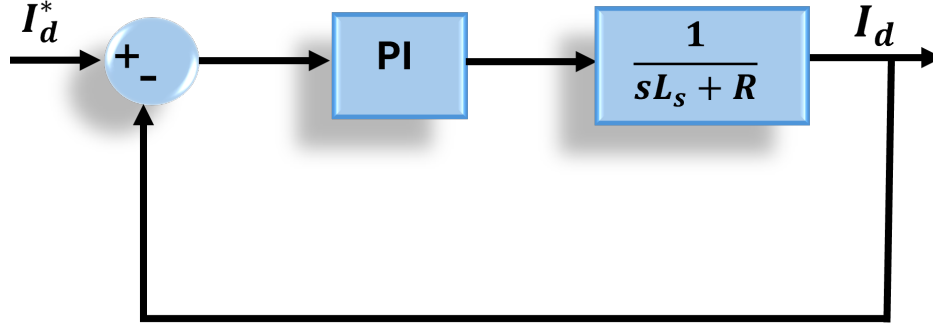


Figure 4.3: I_{sd} current control loop

$$I_{sd}(s) = G_{cl}(s) I_{sd}^*(s) \quad (4.40)$$

$$I_{sd}(s) = G_{cl}(s) I_{sq}^*(s) \quad (4.41)$$

where;

$$G_{cl}(s) = \frac{\frac{sK_p + K_i}{L_s}}{s^2 + \frac{K_p + R_s}{L_s}s + \frac{K_i}{L_s}} \quad (4.42)$$

4.4.3 PI Controller Parameter Tuning

Accurate tracking of the current reference values necessitates the precise adjustment of the proportional and integral gains, K_p and K_i . Inappropriate selection of these gains can result in diminished tracking performance or potential instability of the closed-loop system. To enable a systematic tuning methodology, the closed-loop transfer function derived in (4.42) is identical to a standard second-order system.

$$G(s) = \frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} \quad (4.43)$$

where ω_c and ξ are the control bandwidth and damping ratio, respectively. The

damping factor ξ quantifies the degree of damping in a dynamic system and substantially affects its transient response. In the absence of a damping factor, the system exhibits persistent oscillations when subjected to a disturbance. A damping factor of one indicates a severely damped system, which attains fastest settling time without oscillations. For values of ξ between zero and one, the system is underdamped, leading to oscillations that progressively diminish with time.

In contrast, when the damping factor exceed unity, the system is considered overdamped, resulting in a diminished dynamic responsiveness. Alongside the damping properties, the control bandwidth ω_c signifies the frequency range in which the control system can effectively follow reference signals and mitigate disturbances.

At this point, the controller gains can be evaluated by coefficient comparison using the resulting second-order dynamic model shown in (4.42). This method enables the explicit expression of the integral and proportional gains as functions of the control bandwidth, damping factor, and system [3]. The control bandwidth is specified using the standard second-order form identified in as follows (4.43);

$$\omega_c^2 = \frac{K_i}{L_s}. \quad (4.44)$$

It is worth noting that the numerator of the closed-loop transfer function includes the expression $(sK_p + K_i)/L_s$, which introduces a zero into the system due to the PI controller structure. Although the constant factor $1/L_s$ does not affect the root position, the zero can be determined from the polynomial.

$$sK_p + K_i = 0 \quad (4.45)$$

This yields a zero when $s = -K_i/K_p$. Since both controller gains K_p and K_i are positive, the zero resides in the left half-plane and hence does not influence the stability of the system, which is determined by the closed-loop poles. However, this zero significantly influences the transient response by generating a phase-lead effect that elevates the dynamic performance of the current control loop and improves reference tracking accuracy.

The integral gain K_i can be simply derived from this relationship.

$$K_i = \omega_c^2 L_s. \quad (4.46)$$

Additionally, by comparing the coefficients of the s term in the denominators of the closed-loop transfer function and the standard second-order model, the proportional gain K_p can be determined as

$$K_p = 2\xi\omega_c L_s - R_s. \quad (4.47)$$

The PI controller gains are calculated to ensure that the closed-loop transfer function demonstrates the specified damping factor ξ and control bandwidth ω_c . An examination of the closed-loop poles, as shown in Fig. 2.14, verifies that the positions of the complex-conjugate poles are directly determined by the selected values of ξ and ω_c .

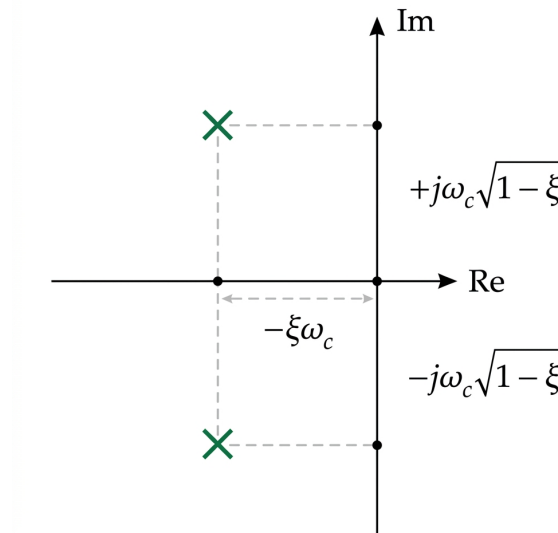


Figure 4.4: closed-loop poles of transfer function

Depending on the chosen damping factor, control bandwidth, and system characteristics, the gain calculation may result in a negative value of the proportional gain K_p . This scenario occurs when

$$2\xi\omega_c L_s - R_s < 0 \quad (4.48)$$

By defining the damping factor as $\xi = 1$, the aforementioned condition is simplified to

$$\omega_c < \frac{R_s}{2L_s}. \quad (4.49)$$

Consequently, if the chosen control bandwidth ω_c is less than $\frac{R_s}{2L_s}$, the proportionate gain derived from the tuning formula becomes negative. Given that a negative proportional gain is undesirable for current control loop, it is advisable to set the proportional gain K_p to zero and calculate the controller parameters by a different tuning method.

Under this condition, the closed-loop dynamics depend only on the integral gain K_i and the system parameters. By examining the denominator of (4.43), it can be observed that when $K_p = 0$, the pole locations of the closed-loop system are determined solely by K_i . Consequently, the characteristic equation becomes

$$s^2 + \frac{R_s}{L_s}s + \frac{K_i}{L_s} = 0 \quad (4.50)$$

The explicit assignment of the damping factor is no longer feasible; yet, the control bandwidth may still be established by the appropriate selection of the integral gain. According to the characteristic equation (4.50), the closed-loop pole positions can be determined as

$$s_{1,2} = \frac{-\frac{R_s}{L_s} \pm \sqrt{\left(\frac{R_s}{L_s}\right)^2 - \frac{4K_i}{L_s}}}{2}. \quad (4.51)$$

The dominating pole of the closed-loop system can be explicitly determined as a function of the integral gain K_i , based on the characteristic equation established in the previous section. In a transfer function, the dominant pole is characterized as the pole nearest to the imaginary axis, since it mostly dictates the system dynamics. To get the intended dynamic response, the dominating pole is thus chosen to be real, negative, and equivalent to the specified control bandwidth. The remaining pole is real and negative, positioned further from the imaginary axis, consequently exhibiting a minor impact on the system dynamics.

To establish the preferred position of the dominating pole, the further criterion is specified:

$$-\omega_c = \frac{-\frac{R_s}{L_s} + \sqrt{\left(\frac{R_s}{L_s}\right)^2 - \frac{4K_i}{L_s}}}{2}. \quad (4.52)$$

Determining the integral gain from the aforementioned equation results in

$$K_i = \omega_c R_s - \omega_c^2 L_s. \quad (4.53)$$

The resulting closed-loop pole locations obtained through this procedure are illustrated in figure 4.5.

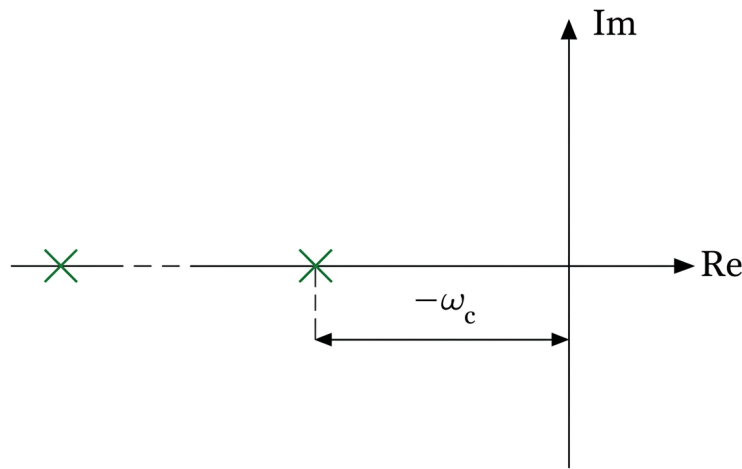


Figure 4.5: closed loop pole

In conclusion, with a damping factor of $\xi = 1$, the tuning methodology for the PI controller gains can be explained as follows:

$$\left\{ \begin{array}{l} \text{if } \omega_c < \frac{R_s}{L_s}, \\ \text{if } \omega_c > \frac{R_s}{L_s}, \end{array} \right\} \left\{ \begin{array}{l} K_p = 0, \\ K_i = \omega_c R_s - \omega_c^2 L_s, \\ K_p = 2\xi\omega_c L_s - R_s, \\ K_i = \omega_c^2 L_s. \end{array} \right. \quad (4.54)$$

Finally, the schematic illustration of the output current control algorithm is shown in figure 4.6. The measured output currents are first converted into the synchronous reference frame and then transmitted to the controller. The PI controllers analyze the

difference between the reference and measured current components, producing the associated voltage control signals $\Delta U_d^*(s)$ and $\Delta U_q^*(s)$. The reference voltages v_{sd}^* and v_{sq}^* are derived by the incorporation of the decoupling terms. The resultant dq -axis voltage reference vector is then converted back into the three-phase reference frame, and the associated signals are ultimately applied to the modulation stage.

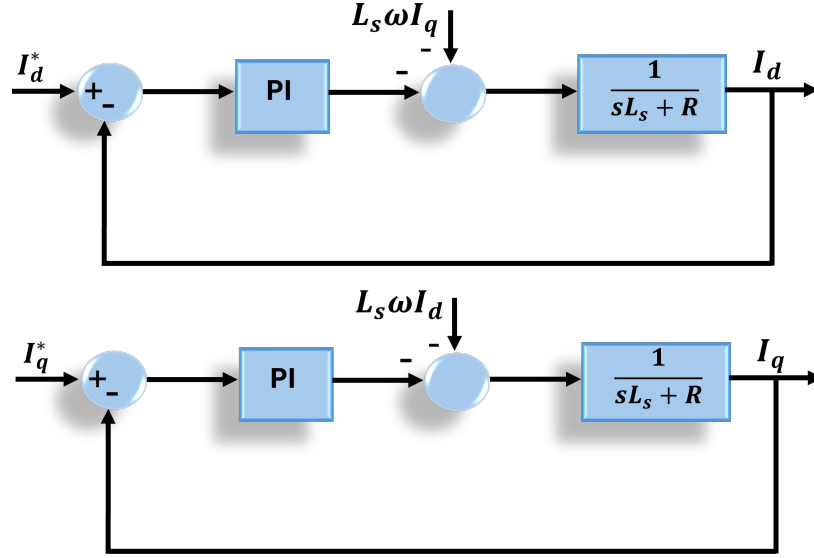


Figure 4.6: I_{sd} and I_{sq} closed-loop current control

4.5 Average DC-Link Voltage Control

The average DC-link voltage is controlled by an external loop that maintains power balance between the AC and DC sides of the converter. Given that the dynamics of the DC-link voltage are intrinsically slower than those of the current, the voltage controller is structured as an outside loop that produces the reference for the inner d -axis current controller. For control design, the dynamic properties of the DC-link capacitor, as represented by (4.1), are used, with the DC-side load considered an external disturbance and consequently omitted from the nominal plant model.

In a grid-connected converter operating under voltage-oriented control, the d -axis is aligned with the grid voltage vector. As a result, the q -axis voltage component fulfills $\Delta u_q = 0$, and the q -axis current reference is established at zero to attain unity power factor operation. Under these circumstances, the dynamics of the DC-link voltage are only influenced by the d -axis current component, thus encapsulating the primary en-

ergy storage characteristics of the DC-link capacitor while ensuring resilience to load variations.

Consequently, Dc-link voltage dynamics can be simplified to the following expression:

$$\Delta \dot{V}_{dc} = \frac{3}{2C} \bar{u}_d \Delta I_{sd} \quad (4.55)$$

To get the open-loop transfer function, it is advantageous to apply the Laplace transform on (4.55), resulting in the following expression.

$$s \Delta V_{dc}(s) = \frac{3}{2C} \bar{u}_d \Delta I_{sd}(s) \quad (4.56)$$

In the cascaded control structure, the DC-link voltage controller serves as an external loop and produces the reference for the inner d -axis current controller. The inner current loop is designed to operate at significantly higher speed than the voltage loop, allowing it to reliably follow the current reference. Assuming this, the variation in the d -axis current, ΔI_{sd} , can be considered the effective control input for the dynamics of the DC-link voltage, while the variation in the DC-link voltage, ΔV_{dc} , signifies the system output. According to this formulation, the open-loop transfer function relating the control input $\Delta i_{sd}(s)$ to the output $\Delta v_{dc}(s)$ is derived as

$$G_v(s) = \frac{\Delta V_{dc}(s)}{\Delta I_{sd}(s)} = \frac{3 \bar{u}_d}{2Cs} \quad (4.57)$$

A proportional-integral (PI) controller is used in the outer voltage control loop to maintain the DC-link voltage at a specified reference value. The PI controller evaluates the DC-link voltage error and produces the reference for the inner d -axis current controller. The closed-loop DC-link voltage dynamics can be expressed based on this control structure as follows.

$$\Delta I_{sd}^*(s) = K_{pv} (V_{dc}^* - V_{dc}) + \frac{K_{iv}}{s} (V_{dc}^* - V_{dc}) \quad (4.58)$$

By substituting the output of the voltage controller as specified in (4.58) into equation (4.57), the closed-loop transfer function of the DC-link voltage control system is derived

and expressed as follows:

$$\frac{\Delta V_{dc}(s)}{\Delta V_{dc}^*(s)} = \frac{\frac{3\bar{u}_d}{2C} (K_{pv}s + K_{iv})}{s^2 + \frac{3\bar{u}_d}{2C} K_{pv}s + \frac{3\bar{u}_d}{2C} K_{iv}} \quad (4.59)$$

Figure 4.7a illustrates the closed-loop configuration of the average DC-link voltage control loop using a PI controller. The denominator of the closed-loop transfer function in (4.59) is a second-order polynomial in the Laplace variable s , signifying that the DC-link voltage dynamics during closed-loop operation are dictated by a second-order system. The closed-loop behavior may be articulated in the usual second-order form presented in (4.43).

By equating the coefficients of the denominator of (4.59) with those of the normal second-order system, the proportional and integral gains of the voltage PI controller can be correlated with the required natural frequency ω_c and damping ratio ξ

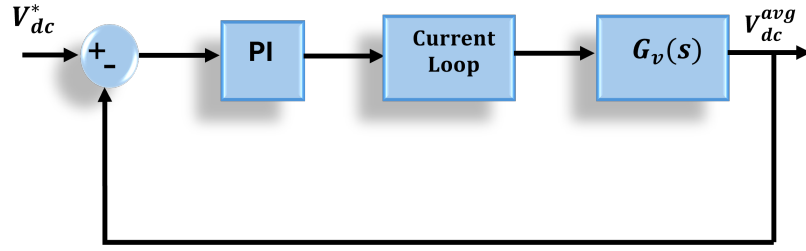
$$\omega_n^2 = \frac{3U_d}{2C} K_i, \quad 2\zeta\omega_n = \frac{3U_d}{2C} K_p. \quad (4.60)$$

Here, U_d represents the steady-state d -axis voltage component, which is determined by the modulation process and can be expressed as a duty-cycle between $-N$ to N . Since the methodology for tuning the PI controller gains has already been discussed in detail in the previous section, it is not repeated here.

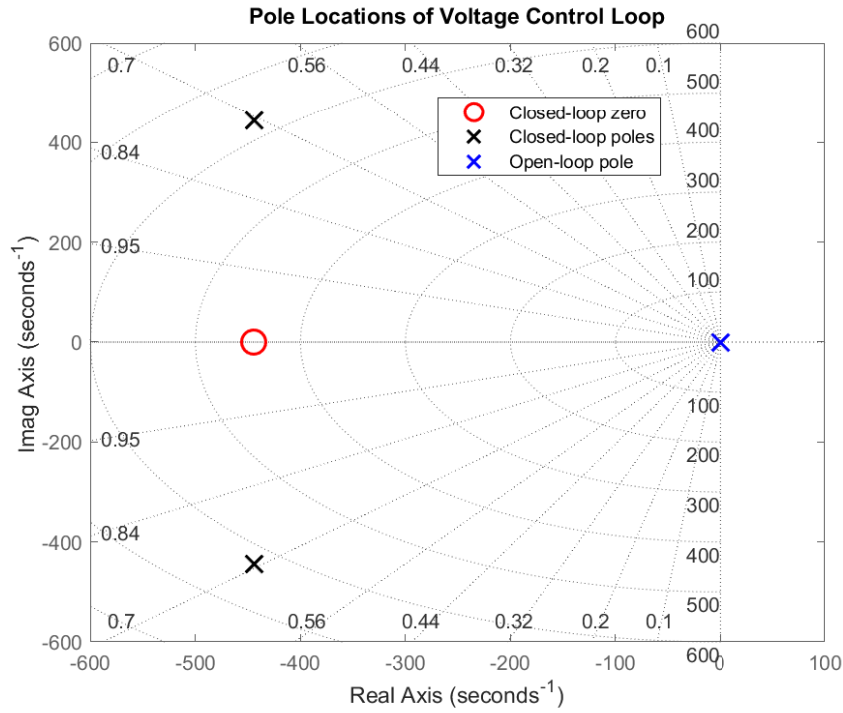
The resulting closed-loop pole locations corresponding to the selected controller gains are illustrated in figure 4.7b. It can be observed that all poles are located in the left-half of the complex plane, thereby confirming the stability of the average DC-link voltage control loop.

4.6 Complete Voltage-Oriented Control

A complete block diagram of the entire control system is shown in figure 4.8. The control strategy utilizes voltage-oriented control (VOC) and includes inner current control loops alongside an outer DC-link voltage control loop. The observed three-phase voltages and currents are first converted into the synchronous (d, q) reference frame by Park and Clarke transformations, enabling separate regulation of active and reactive



(a) Block diagram of average DC-link voltage



(b) Close-loop pole position of DC-link voltage controller

Figure 4.7: DC-Link voltage controller along with close-loop pole position

power components.

To further examine the stability of the proposed control architecture, the eigenvalues of an entire closed-loop system matrix are analyzed under both light and heavy-load operating environments and is presented in 4.9 and in 4.10, respectively. The calculated eigenvalues are situated in the left half of the complex plane for both scenarios, affirming that the whole system is asymptotically stable within the specified operating range. Furthermore, figure. 4.9(b) and 4.10(b) demonstrate that the dominant poles exhibit slight movement in location between light-load and heavy-load circumstances. In particular, the dominant poles migrate somewhat along the real axis under heavy-load conditions, indicating a change in system dynamics. This shift indicates a change in the

system's time constants and effective damping as a result of load variation. However, the system ensures sufficient damping and dynamic performance without any concern of instability since the dominant poles stay fixed within the left half-plane and do not approach the imaginary axis.

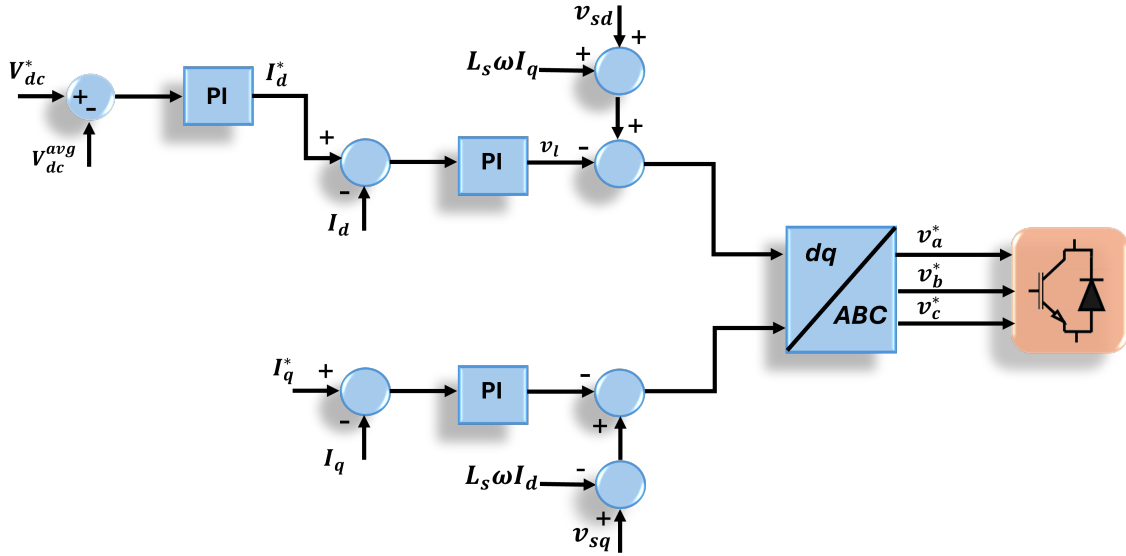


Figure 4.8: Voltage-oriented control of 7-level CHB-AFE converter

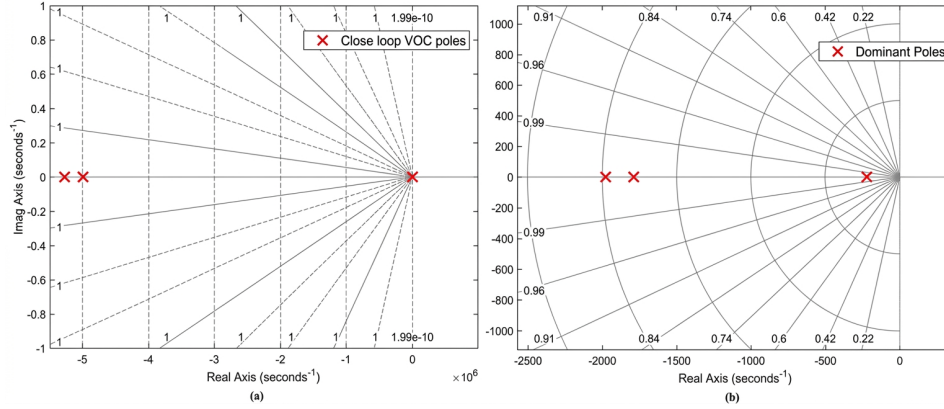


Figure 4.9: Close-loop pole position of CHB-AFE under light load

The effectiveness of the resulting average and switching models under voltage-oriented control is further analyzed by simulation experiments performed for both heavy and light load operating circumstances, as seen in figures 4.11a and 4.11b, respectively. The parameters used to validate both the average and switching models are summarized in table 4.1. The findings indicate that the cascaded H-bridge active front-end (CHB-AFE) functions reliably, attains precise reference tracking, and maintains the stability over wide range of load operation.

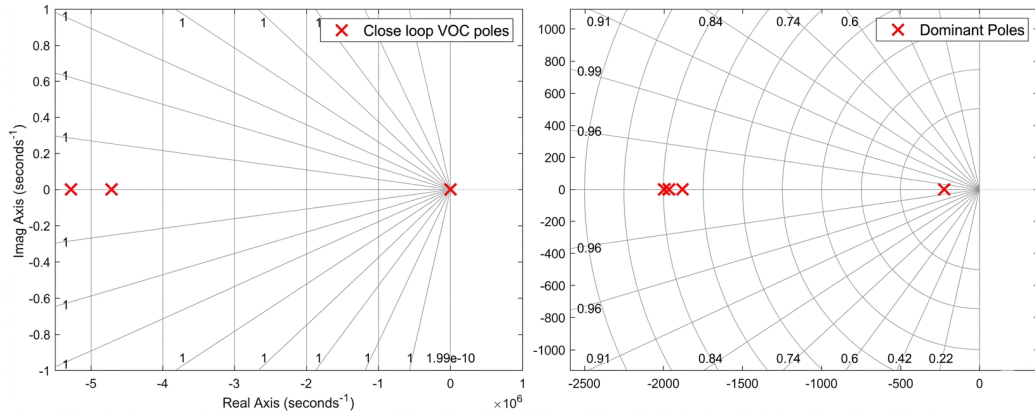


Figure 4.10: Close-loop pole position of 7-level CHB-AFE under heavy load

Table 4.1: Simulation Setup Parameters

Parameters	Values
V_{URMS}	3.3 kV
f	50 Hz
f_{sw}	10 kHz
L_s	0.2 mH
R_s	0.1 m Ω
C	3700 $\mu\mu\text{F}$
V_{dc}^*	1050 V
P_{L1}	450 kW
P_{L2}	900 kW

4.7 DC-Link Voltage Balancing

Despite voltage-oriented control (VOC) facilitates precise reference tracking and balanced grid currents under optimal circumstances, it does not intrinsically provide equal power distribution across the various cells and phases of a cascaded H-bridge (CHB) converter. In real time operation, unbalanced loads, parameter deviations, and modulation limitations produce a deviation from optimal power distribution, resulting in internal power imbalances inside the converter. These imbalances immediately impact the control of DC-link voltages and, if improperly managed, can compromise grid current quality and overall system reliability.. Consequently, specialized DC-link voltage balancing solutions are essential to guarantee reliable and grid-compliant functioning of CHB-based systems.

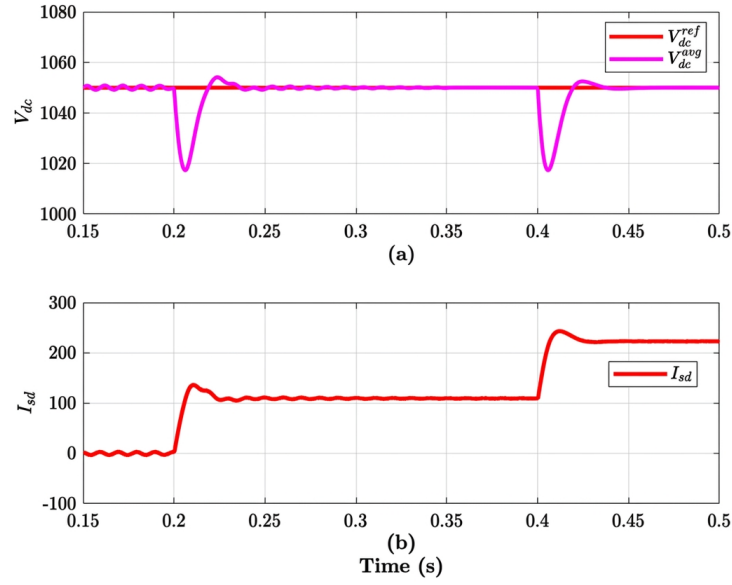
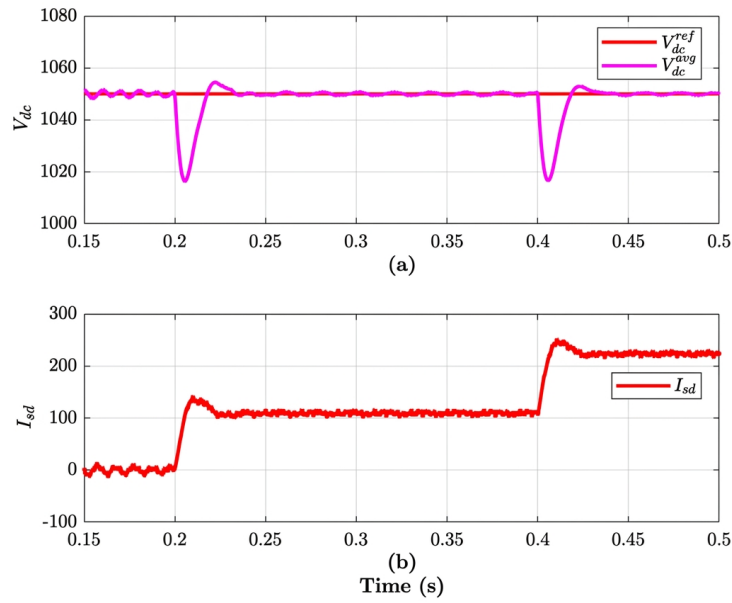
(a) Average DC-link voltage and I_{sd} of Average model(b) Average DC-link voltage and I_{sd} of switching model

Figure 4.11: Validation of VOC in average and switching model

The power imbalance in CHB converters can be systematically categorized into two types depending on its origin and effect: per-cell imbalance and per-phase imbalance. Per-cell imbalance denotes the uneven distribution of power among the H-bridge cells within a single phase, resulting in disparate power processing by individual cells (e.g., $P_{a1} \neq P_{a2} \neq P_{a3}$ for a three-cell CHB). Per-phase imbalance arises when the total power handled by each phase of the converter is uneven (i.e., $P_a \neq P_b \neq P_c$).

The two types of power imbalance affect the converter control system in fundamentally distinct manners. The per-cell imbalance mostly impacts the DC-link voltage control loop, resulting in the voltages of individual DC-link capacitors deviating from their reference values. Voltage variations can cause waveform distortion and, in extreme instances, affect the reliable operation of the converter. Conversely, per-phase imbalance primarily affects the current control loop, leading to imbalanced grid currents throughout the phases.

The VOC method produces a singular balanced voltage reference for all phases, consequently lacking the capability to independently address unequal power distribution among Hbridge cells of each phase. Consequently, any persistent power imbalance typically manifests as asymmetrical phase currents. However, this existing imbalance violates grid code requirements and is therefore undesirable in grid-connected systems. The inherent constraint of VOC necessitates the creation of a supplementary DC-link voltage balancing algorithm that can regulate individual cell voltages while maintaining balanced grid currents.

4.7.1 Model Predictive Based Voltage Balancing Algorithm

Chapter 2 outlines that current DC-link voltage balancing solutions for CHB-AFE converters, especially those utilizing redundant switching states and low-switching-frequency modulation, encounter scalability and control complexity issues when applied to systems with several cells. This section introduces a model predictive control (MPC)-based algorithm for DC-link voltage balancing, designed to leverage system predictions for fast and resilient voltage equilibrium while ensuring a low switching frequency. The comprehensive control architecture of the proposed 7-level CHB-AFE converter, which includes the MPC-based DC-link voltage balancing algorithm, is illustrated in figure 4.12.

In a CHB-AFE, the instantaneous reference voltage v_{ref}^* as established by the VOC scheme, must be generated utilizing the discrete voltage levels obtainable in each phase, commonly represented as integer multiples of the DC-link voltage, i.e., $k \cdot V_{dc}$. The distinct voltage levels are produced by the precise switching of separate H-bridge cells, each powered by an independently regulated DC-link capacitor. To precisely replicate the reference voltage, two contiguous discrete voltage levels (e.g., $k \cdot V_{dc}$ and $(k - 1) \cdot V_{dc}$)

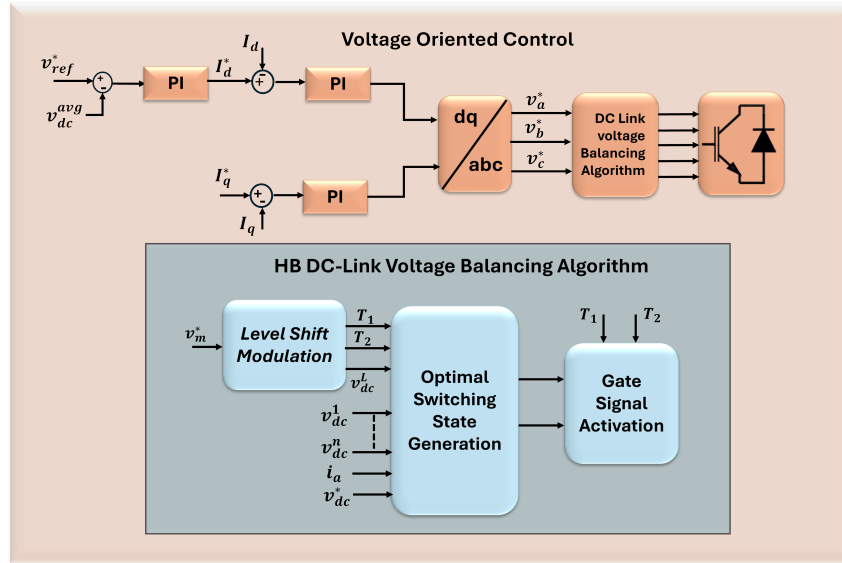


Figure 4.12: VOC with DC-link voltage balancing of 7-level CHB-AFE

are identified within a single sampling period (T_s), and their corresponding time durations are computed so that the time integral of the reference voltage is equivalent to the aggregate of the time integrals of the selected discrete voltages. Consequently, the subsequent relation can be expressed as

$$\int_{T_s} v_{ref}^* dt = k \cdot V_{dc,i} \cdot T_{on} + (k-1) \cdot V_{dc,i} \cdot (T_s - T_{on}),$$

Here, $k \cdot V_{dc}$ and $(k-1) \cdot V_{dc}$ signify the two discrete voltage levels adjacent the reference voltage v_{ref}^* , while T_{on} denotes the time interval during which the voltage level $k \cdot V_{dc}$ is enforced. The generation of a continuous reference voltage utilizing neighboring discrete voltage levels within a single sampling period is depicted in Fig. 4.13.

The electrical model corresponding to a single H-bridge cell is depicted in Fig. 4.14. According to this model, the voltage dynamics of the DC-link capacitor in the i -th cell can be articulated as

$$C \frac{dv_{dc}}{dt} = i_s \cdot S_i - i_{L_i}, \quad i \in \{1, 2, \dots, N\}, \quad (4.61)$$

where C denotes the DC-link capacitance, i_s signifies the grid-side AC current, $S_i \in \{-1, 0, 1\}$ indicates the switching state of the i -th H-bridge cell, and i_{L_i} represents the load-side current. Due to the necessity for DC-link voltage equalization across all cells,

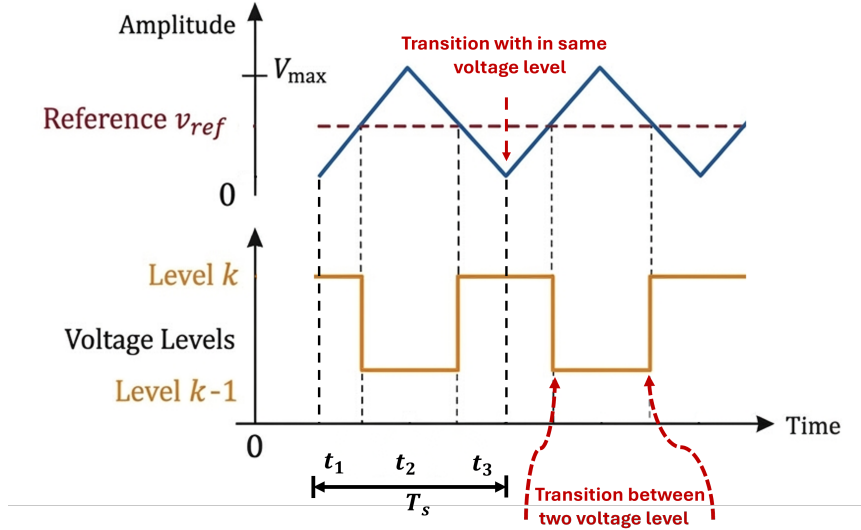


Figure 4.13: discrete voltage synthesis

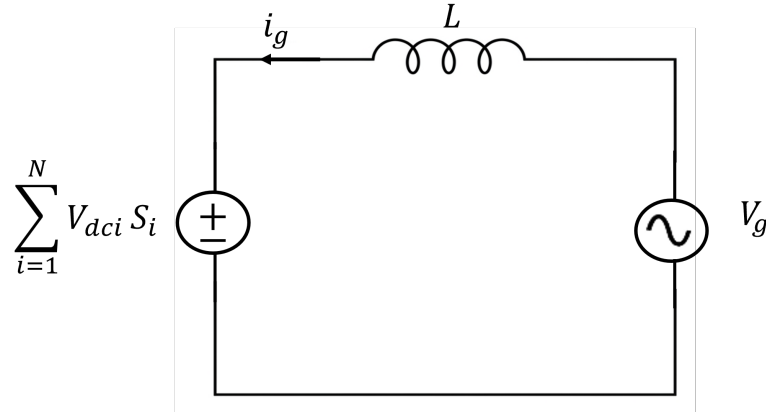


Figure 4.14: Equivalent Model of one Phase of CHB-AFE

it is assumed that the capacitances are similar, specifically, $C_1 = C_2 = \dots = C_N = C$. Moreover, the load currents i_{L_i} are considered as disturbances and discarded to simplify the predictive model.

Utilizing the forward Euler discretization approach on (4.61), the discrete-time predictive model for the DC-link voltage is derived as

$$v_{dc_i}^p(k+1) = v_{dc_i}(k) + \frac{1}{C} (\alpha_{1i}T_1 + \alpha_{2i}T_2) i_s \quad (4.62)$$

Here, $v_{dc}(k)$ and $v_{dc}(k+1)$ represent the current and predicted DC-link voltages, respectively, while T_i signifies the time interval allocated to the i -th discrete voltage level within a single sampling period. The permissible switching states analyzed in the predic-

Table 4.2: Switching States for 7-Level CHB-AFE

Vdc Level	Switching States						
+3Vdc	1 1 1						
+2Vdc	1 1 0 1 0 1 0 1 1						
+Vdc	-1 1 1	1 -1 1	1 1 -1	1 0 0	0 1 0	0 0 1	
0Vdc	1 -1 0 1 0 -1 0 1 -1 0 -1 1						
	-1 1 0 -1 0 1 0 0 0						
-Vdc	-1 -1 1	-1 1 -1	1 -1 -1	0 -1 0	0 0 -1	-1 0 0	
-2Vdc	-1 -1 0 -1 0 -1 0 -1 -1						
-3Vdc	-1 -1 -1						

tive optimization, along with their associated output voltage levels for the 7-level CHB-AFE, are included in Table 4.2. A multilevel converter can produce equal output voltage levels through various combinations of H-bridge switching states, offering redundancy that can be utilized for balancing the DC-link voltage.

The proposed MPC-based voltage balancing algorithm initially maps the continuous reference voltage v_{ref}^* produced by the VOC scheme to its two neighboring discrete voltage levels during each PWM sampling period via level-shifted PWM. Consequently, the time intervals T_1 , T_2 , and T_3 corresponding to these voltage levels are determined based on the relative placement of v_{ref}^* inside the discrete voltage range. The DC-link voltages of all CHB-AFE cells are anticipated for each permissible switching state based on (4.62) using these durations.

DC-link voltage balancing is accomplished by evaluating a cost function for all potential switching states during each PWM cycle. The switching state that minimizes the cost function is designated as the ideal state and implemented for the relevant switching time. The cost function is delineated as

$$J_{m,z} = \sum_{j=1}^N \left(v_{dc_ref} - v_{dc,m,j}^{P,z} \right)^2, \quad (4.63)$$

where v_{dc_ref} represents the reference DC-link voltage, and $v_{dc,m,j}^{P,z}$ signifies the predicted DC-link voltage of the j -th cell for phase m in the z -th switching state. In this context, $m \in \{a, b, c\}$ indicates the phase index, while z indicates the switching-state index.

4.7.2 Reduction of Switching Frequency

The proposed MPC-based voltage balancing algorithm ensures DC-link voltage equalization among the CHB-AFE cells; however, it may result in elevated switching frequency if not well controlled. To calculate the necessary discrete voltage within a single sample period, a standard carrier-based level-shift pulse-width modulation (LSPWM) utilizing triangle carrier waveforms is commonly utilized. When such carriers are used, the beginning of a new switching period generally starts at the same discrete voltage level as that applied at the end of the previous switching period, as depicted in figure 4.13.

The unwanted rise in switching events can be efficiently reduced by altering the configuration of the carrier signals employed in the modulation process. Figure 4.15 depicts the scenario in which sawtooth carriers are utilized in place of traditional triangle carriers. In compared to triangular carriers, which exhibit symmetry and restore to the same voltage level at beginning of each switching period, sawtooth carriers present a continuous monotonic increase throughout the whole sampling interval.

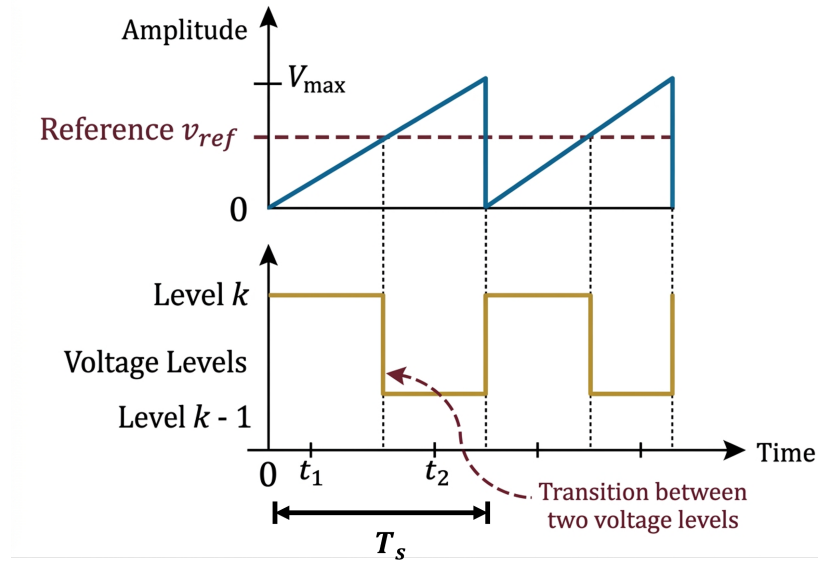


Figure 4.15: Transition between voltage level using Saw-tooth carrier

As illustrated in figure 4.15, the switching period consistently starts at a specified boundary of the sawtooth carrier waveform. Therefore, the output voltage at the beginning of a new switching period cannot maintain the same discrete voltage level as that of the previous one unless specifically dictated by the reference voltage trajectory. Consequently, transitions inside redundant switching states at identical voltage levels are

naturally prevented. Instead, transitions occur exclusively between neighboring discrete voltage levels (i.e., from level $(k - 1)$ to level k , or vice versa).

This attribute is particularly beneficial inside the proposed MPC-based voltage balancing system. The cost function is assessed during the previous sampling interval and implemented in next switching period; therefore, utilization of sawtooth carriers guarantees that the chosen switching state inherently facilitates level-to-level transitions .

Alongside the lowering of the carrier-based switching frequency, a switching cost parameter is also incorporated into the cost function presented in equation 4.63 to further mitigate unwanted commutations. This supplementary term penalizes state transitions that lead to an increased number of device changes between consecutive sample intervals, consequently explicitly penalizing excessive switching activity. By including the switching effort directly into the optimization problem, the controller can effectively balance the trade-off between DC-link voltage regulation performance and the minimization of switching frequency. The resultant altered cost function is delineated as follows:

$$J_{m,z} = \sum_{j=1}^N \left(v_{dc,m,j}^{P,z} - v_{dc_ref} \right)^2 + \lambda_{sw} \sum_{j=1}^N \left| S_j^z(k) - S_j(k-1) \right| \quad (4.64)$$

The second term represents the switching penalty, where $S_j^z(k)$ is the candidate switching state of the j -th cell at the current sampling instant k , and $S_j(k-1)$ is the switching state applied in the previous sampling instant. The weighting factor λ_s determines the trade-off between DC-link voltage balancing performance and switching frequency reduction.

By restricting switching transitions to occur only between consecutive voltage levels, the total number of commutations per sampling period is significantly reduced. This directly lowers switching losses and thermal stress in the power devices, improves overall converter efficiency, and enhances the reliability and lifetime of the CHB-AFE system, particularly under high-power operating conditions.

4.8 DC Link Voltage Balancing Limits

The DC-link voltage balancing algorithm can efficiently regulate the DC-link voltages to their reference values; however, its balancing capability is fundamentally constrained by the permissible power imbalance among the H-bridges within the same phase leg. When this limits over stepped, the balancing algorithm is unable to maintain a DC-link voltage balancing, potentially resulting in improper converter performance. Consequently, it is imperative to determine these operational limits and ensure that they are respected during converter operation. To facilitate the analysis, each H-bridge is assumed to be connected to a distinct resistive load. Given that the limits are independent for each CHB leg, only phase— a will be examined in the subsequent study.

The simplified average model of a single-phase leg of the CHB converter, comprising N cascaded H-bridge cells, as depicted in figure 4.14, is used to evaluate the DC-link voltage balancing limitations of the CHB converter. In the equivalent model, the total average duty cycle has been divided into distinct duty cycles S_n , each linked to a specific H-bridge cell.

Moreover, owing to the intrinsic power conversion attributes of the CHB converter, current is provided to the DC-link side while voltage is transmitted to the AC grid side via regulated current and voltage sources, respectively. Under steady-state operating conditions, the balancing of DC-link voltage necessitates that the average power handled by each H-bridge cell be equivalent. This condition enables the derivation of DC-link voltage balancing limits directly from the power equations of an individual H-bridge cell, utilizing the average model representation. This modeling approach offers a definitive mathematical framework for establishing the feasible operating range of individual cell powers while ensuring DC-link voltage balance.

The average AC-grid power in an individual system is denoted as

$$P_g = \frac{V_s I_g \cos(\theta)}{2} \quad (4.65)$$

The power handled by a single H-bridge cell in a cascaded H-bridge converter can be articulated as a function of its respective duty cycle and is represented by

$$P_n = \frac{S_n I_g V_{dcn}}{2} \quad (4.66)$$

Let P_n signifies the average power processed by the n^{th} H-bridge cell ($n \in \{1, 2, \dots, N\}$), S_n represent the corresponding average duty cycle of the n^{th} cell, I_g denote the grid-side current, and V_{dcn} denote the DC-link voltage of the n^{th} H-bridge cell.

The total average power in a grid can be determined by summing the individual power of the CHB; consequently, the equation 4.66, assuming a unity power factor, can be formulated as follows:

$$P_g = P_1 S_1 + P_2 S_2 + P_3 S_3 + \dots P_n S_n \quad (4.67)$$

Balancing algorithms govern the allocation of power among the individual H-bridge cells, whilst the overall duty cycle S_t of the phase leg is determined by external power requirements. The overall duty cycle can be represented as the sum of the individual cell duty cycle indices.

$$S_t = S_1 + S_2 + S_3 + \dots S_n = \frac{V_g}{V_{dc}} \quad (4.68)$$

Where, S_n represents the duty cycle of the n^{th} H-bridge cell, V_g signifies the amplitude of the grid-side voltage, and V_{dc} specifies the nominal DC-link voltage. Under steady-state conditions for DC-link voltage balancing, the DC-link voltages of all H-bridge cells are equal, i.e.,

$$V_{dc1} = V_{dc2} = \dots = V_{dcn} \quad (4.69)$$

Using the average power model represented in equation 4.66, the DC-link voltage of the n^{th} H-bridge cell can be expressed as

$$V_{dcn} = \frac{2P_n}{S_n I_g}, \quad n \in \{1, 2, \dots, N\}. \quad (4.70)$$

By equating the DC-link voltage expressions of the 1^{st} and 2^{nd} H-bridge cells, the subsequent relation is obtained:

$$\frac{2P_1}{S_1 I_g} = \frac{2P_2}{S_2 I_g}. \quad (4.71)$$

Simplifying (4.71) yields

$$S_2 = S_1 \frac{P_2}{P_1}. \quad (4.72)$$

Likewise, comparing the DC-link voltage equations of the first and third H-bridge cells yields

$$\frac{2P_1}{S_1 I_g} = \frac{2P_3}{S_3 I_g}. \quad (4.73)$$

which leads to

$$S_3 = S_1 \frac{P_3}{P_1}. \quad (4.74)$$

Generally, under conditions of DC-link voltage balance, the duty cycle of the n -th H-bridge cell can be described in relation to the first cell as

$$S_n = S_1 \frac{P_n}{P_1}, \quad n \in \{2, 3, \dots, N\}. \quad (4.75)$$

The total duty cycle of a phase leg in a 7-level CHB converter, comprising three cascaded H-bridge cells, is determined by the sum of the individual cell duty cycles as expressed in (4.68). Under conditions of DC-link voltage balance, the duty cycles of the second and third cells can be defined in relation to the duty cycle of the first cell, utilizing the power-based equations established in (4.72) and (4.74).

By inserting these equations into the total duty cycle ((4.68)), the subsequent relation is derived:

$$S_t = S_1 + S_1 \frac{P_2}{P_1} + S_1 \frac{P_3}{P_1}. \quad (4.76)$$

Factorizing the S_1

$$S_t = S_1 \left(1 + \frac{P_2}{P_1} + \frac{P_3}{P_1} \right). \quad (4.77)$$

Now, multiplying both sides by P_1

$$P_1 S_t = S_1 (P_1 + P_2 + P_3). \quad (4.78)$$

After solving for the 1st cell duty cycle

$$S_1 = \frac{P_1}{P_1 + P_2 + P_3} S_t. \quad (4.79)$$

Equation (4.79) indicates that, under conditions of DC-link voltage balance, the duty cycle of each H-bridge cell is directly proportional to its processed power in relation to the total power of the phase leg. This outcome ensures uniform average DC-link voltages while satisfying to the comprehensive duty cycle constraint required by the grid voltage requirements.

In a cascaded H-bridge converter, the greatest attainable duty cycle of a single cell is achieved when the cell operates in a square-wave mode, generating an output voltage that oscillates straight between $+V_{dc}$ and $-V_{dc}$ without intermediary zero states. Under this operational condition, the fundamental component of the square-wave voltage reaches its maximum amplitude in relation to the DC-link voltage. Thus, the modulation index of the n -th H-bridge cell is intrinsically constrained by the fundamental component of a square wave, thereby imposing an upper limit on the attainable modulation depth. Consequently, the duty cycle of each individual cell must respect to the following constraint:

$$S_n \leq \frac{4}{\pi}, \quad n \in \{1, 2, \dots, N\}. \quad (4.80)$$

By implementing the modulation index restriction specified in (4.80) to the duty-cycle expression in (4.79), the ensuing inequality is derived:

$$P_1 \left(\frac{\pi}{4} S_t \right) \leq P_1 + P_2 + P_3 \quad (4.81)$$

By rearranging this expression, the inequality can be reformulated as (4.82), which directly correlates the power processed by the initial H-bridge cell to the combined power of the remaining cells.

$$P_1 \left(\frac{\pi}{4} S_t - 1 \right) \leq P_2 + P_3. \quad (4.82)$$

This constraint can be imposed to each H-bridge cell to delineate the permissible operating region of the converter. The resultant power restrictions for the 7-level CHB converter are depicted in figure 4.16 and can be represented as follows:

$$\begin{aligned} P_{HB}^{a2} + P_{HB}^{a3} &> k P_{HB}^{a1}, \\ P_{HB}^{a1} + P_{HB}^{a3} &> k P_{HB}^{a2}, \\ P_{HB}^{a1} + P_{HB}^{a2} &> k P_{HB}^{a3}. \end{aligned} \quad (4.83)$$

where $k = (\frac{\pi}{4} S_t - 1)$, and P_{HB}^{ai} denotes the average power corresponding to the i -th H-bridge cell.

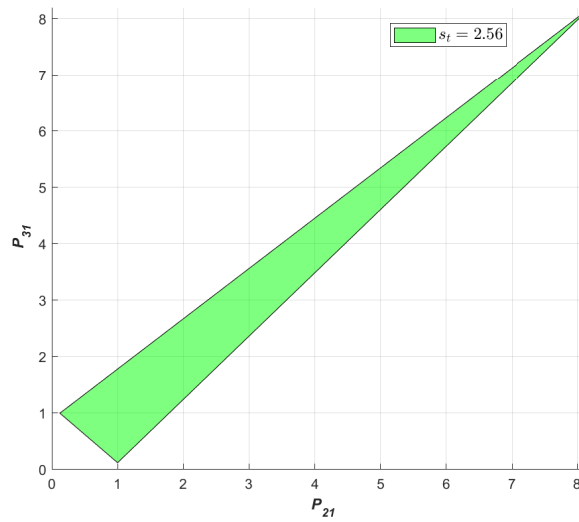


Figure 4.16: DC-link voltage balancing limits for 7-level CHB-AFE

4.9 Optimal Management of Battery Energy Storage System

In extreme fast charging (XFC) stations, the charging demand from electric vehicles is highly dynamic and intrinsically uncertain, as vehicles may connect to or disconnect from various charging ports with differing power requirements. This behavior leads to rapid and unpredictable load variations at the converter DC-link. Under such conditions, a DC-link voltage balancing method alone is insufficient to ensure stable voltage reg-

ulation. In particular, when the operating point moves outside the permissible region established in the previous section, the DC-link voltages deviate from their reference values, resulting in degraded performance or even instability of the CHB-AFE converter.

To address this limitation, a battery energy storage system (BES) module is integrated with each CHB cell through a non-isolated buck converter. The BES modules provide local energy buffering, enabling each cell to compensate for transient power imbalances caused by sudden load variations. This distributed architecture reduces the burden on the DC-link voltage balancing mechanism and ensures reliable converter operation by either supplying or absorbing power as required. Furthermore, it guarantees that the CHB converter operates within the feasible region defined in the preceding section, as illustrated in Fig. 4.16.

Although the inclusion of BES modules enables operation which can handle all kind of power imbalance on the XFC station ports, frequent charging and discharging cycles can accelerate battery degradation. Therefore, the BES should be utilized only when necessary, while simultaneously regulating the state-of-charge (SoC) of each module toward a predefined reference.

To achieve these objectives, the following cost function is formulated:

$$J = \sum_{i=1}^3 \left(P_{BES}^{ai} \right)^2 + \lambda \left(SoC^* - SoC^{ai} \right)^2 \quad (4.84)$$

Here, SoC^{ai} denotes the state of charge of the i^{th} BES module, while SoC^* represents the desired reference value. The first term penalizes excessive BES power usage, thereby reducing unnecessary battery cycling, whereas the second term enforces SoC regulation. The weighting factor λ balances these two objectives. Moreover, the λ also determines the allowable deviation of the state-of-charge (SoC) from its reference value.

To examine the interaction between the CHB converter and the integrated battery energy storage system, the power balance of each H-bridge cell is evaluated. Without loss of generality the analysis is carried out for phase a . Ignoring converter losses, the power needed by the electric vehicle connected to the i -th H-bridge cell port, as illustrated in figure 1.21, can be represent as

$$P_{EV}^{ai} = P_{HB}^{ai} - P_{BES}^{ai}, \quad i \in \{1, 2, 3\} \quad (4.85)$$

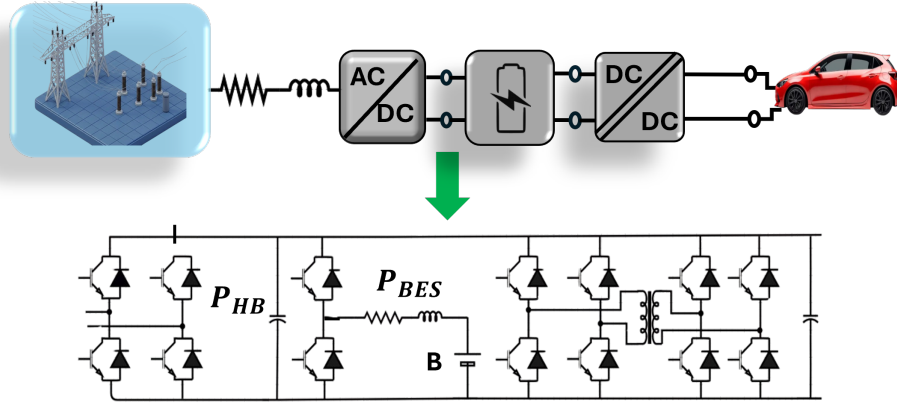


Figure 4.17: Power conversion chain in XFC station

Rearranging, the H-bridge power becomes

$$P_{HB}^{ai} = P_{EV}^{ai} + P_{BES}^{ai} \quad i \in \{1, 2, 3\} \quad (4.86)$$

Substituting (4.86) into the CHB power inequality constraints yields

$$\begin{aligned} P_{EV}^{a2} + P_b^{a2} + P_{EV}^{a3} + P_b^{a3} &> k(P_{EV}^{a1} + P_b^{a1}), \\ P_{EV}^{a1} + P_b^{a1} + P_{EV}^{a3} + P_b^{a3} &> k(P_{EV}^{a2} + P_b^{a2}), \\ P_{EV}^{a1} + P_b^{a1} + P_{EV}^{a2} + P_b^{a2} &> k(P_{EV}^{a3} + P_b^{a3}). \end{aligned} \quad (4.87)$$

Rearranging the inequalities to isolate the BES powers gives

$$\begin{aligned} -kP_b^{a1} + P_b^{a2} + P_b^{a3} &< -kP_{EV}^{a1} + P_{EV}^{a2} + P_{EV}^{a3}, \\ -kP_b^{a2} + P_b^{a1} + P_b^{a3} &< -kP_{EV}^{a2} + P_{EV}^{a1} + P_{EV}^{a3}, \\ -kP_b^{a3} + P_b^{a1} + P_b^{a2} &< -kP_{EV}^{a3} + P_{EV}^{a1} + P_{EV}^{a2}. \end{aligned} \quad (4.88)$$

In real-time operation, different BES modules may require opposite power directions to regulate their SoC. Under such conditions, the above constraints may become infeasible due to the implicit assumption of unidirectional power flow.

To ensure feasibility, an additional constraint is introduced:

$$-P_b^{a1} - P_b^{a2} - P_b^{a3} < P_{EV}^{a1} + P_{EV}^{a2} + P_{EV}^{a3}. \quad (4.89)$$

Combining these constraints, the system can be expressed in matrix form:

$$\begin{bmatrix} k & -1 & -1 \\ -1 & k & -1 \\ -1 & -1 & k \\ -1 & -1 & -1 \end{bmatrix} \begin{bmatrix} P_b^{a1} \\ P_b^{a2} \\ P_b^{a3} \end{bmatrix} < \begin{bmatrix} -kP_{EV}^{a1} + P_{EV}^{a2} + P_{EV}^{a3} \\ P_{EV}^{a1} - kP_{EV}^{a2} + P_{EV}^{a3} \\ P_{EV}^{a1} + P_{EV}^{a2} - kP_{EV}^{a3} \\ P_{EV}^{a1} + P_{EV}^{a2} + P_{EV}^{a3} \end{bmatrix} \quad (4.90)$$

For compact representation, the above inequalities can be written as

$$\mathbf{Ax} < \mathbf{B} \quad (4.91)$$

where $\mathbf{x}$ denotes the BES power vector, while $\mathbf{A}$ and $\mathbf{B}$ define the constraint matrix and limits, respectively.

To formulate the optimization problem, the cost function in (4.84) is expressed in quadratic form as

$$J = \frac{1}{2} \mathbf{x}^\top \mathbf{H} \mathbf{x} + \mathbf{f}^\top \mathbf{x} + c \quad (4.92)$$

where

$$\mathbf{x} = \begin{bmatrix} P_b^{a1} & P_b^{a2} & P_b^{a3} \end{bmatrix}^\top$$

and the Hessian matrix is given by

$$\mathbf{H} = \mathbf{I}_{3 \times 3}. \quad (4.93)$$

The vector $\mathbf{f}$ is derived from the SoC regulation term, while c is a constant independent of $\mathbf{x}$ and can be neglected.

The resulting quadratic programming (QP) problem is formulated as

$$\begin{aligned} \min_{\mathbf{x}} \quad & \frac{1}{2} \mathbf{x}^\top \mathbf{H} \mathbf{x} + \mathbf{f}^\top \mathbf{x} \\ \text{subject to} \quad & \mathbf{Ax} \leq \mathbf{B} \end{aligned} \quad (4.94)$$

However, under certain operating conditions, the constraint set in equation (4.91) may become infeasible. To address this, an alternative formulation is introduced with the following formulation:

$$-\mathbf{Ax} < -\mathbf{B} \quad (4.95)$$

Now, after introducing equation (4.95) the optimization problem represented by equation (4.94) no longer hold a single QP problem and can be represented as,

$$\begin{aligned} \min_{\mathbf{x}} \quad & \frac{1}{2} \mathbf{x}^\top \mathbf{H} \mathbf{x} + \mathbf{f}^\top \mathbf{x} \\ \text{subject to} \quad & \mathbf{Ax} \leq \mathbf{B}, \\ & -\mathbf{Ax} \leq -\mathbf{B} \end{aligned} \quad (4.96)$$

Since two optimization problems, namely QP_1 and QP_2 , are formulated and can easily solved in MATLAB/Simulink by using quadprog function. However, the selection of the active optimization problem is determined based on the comparison of their respective cost function values. At each sampling instant, both optimization problems are evaluated, and the one provides the lower cost is selected as the optimal solution. The corresponding BES power references are then applied for that sampling interval.

However, this selection mechanism may introduce undesired switching between QP_1 and QP_2 , particularly when their cost values are comparable. For instance, the optimal solution may alternate between QP_1 and QP_2 in consecutive sampling instants, resulting in oscillatory behavior in the BES power references, commonly referred to as chattering.

To mitigate this issue, a dwell-time constraint can be introduced, ensuring that once a particular optimization problem is selected, it remains active for a predefined duration before allowing a transition to the alternative formulation. This approach effectively reduces high-frequency switching between optimization solutions and improves overall system stability. A detailed discussion of the dwell-time implementation is provided in the subsequent chapter.

The proposed optimization-based BES management strategy enables the CHB-AFE converter to operate reliably under highly dynamic charging conditions. By incorporating converter limits and SoC regulation, the method ensures stable operation while minimizing battery stress, making it suitable for real-time implementation in XFC systems.

4.10 Summary

This chapter introduced a comprehensive control architecture for a cascaded H-bridge active front-end (CHB-AFE) converter with integrated battery energy storage (BES), specifically designed for extreme fast charging (XFC) station applications. The main goal was to guarantee stable grid integration, effective DC-link voltage regulation, and synchronized energy management in highly dynamic and uncertain charging environments.

The chapter commenced with formulating a control-oriented averaged model of the CHB-AFE system within the synchronous dq reference frame. The steady-state operating points of the converter were analytically determined from this model, and their physical admissibility was assessed. It was demonstrated that only a subset of the mathematical equilibrium solutions satisfies with the duty cycle limits imposed by the converter architecture. These equilibrium points served as the foundation for further small-signal modeling and control design.

A systematic linearization approach was implemented around the chosen steady-state operating point due to the intrinsic bilinear characteristics of the averaged CHB-AFE dynamics. The resultant small-signal model facilitated local stability analysis and offered an appropriate framework for controller synthesis. Consequently, a hierarchical voltage-oriented control (VOC) architecture was implemented, comprising fast inner current control loops and a slower outer DC-link voltage control loop. Proportional–integral (PI) controllers were formulated for both loops, and a definitive tuning methodology based in second-order system characteristics was defined. The impact of controller parameters on closed-loop pole positions and dynamic performance was analytically examined, guaranteeing stable and well-damped operation.

Although VOC provides precise current monitoring and average DC-link voltage management, it does not intrinsically provide equitable power distribution across the individual H-bridge cells. To mitigate this constraint, the chapter examined the mechanisms of DC-link voltage imbalance and differentiated between per-cell and per-phase power imbalances. A approach for balancing DC-link voltage based on model predictive control (MPC) was subsequently introduced. The proposed MPC strategy attained fast and robust voltage balancing by utilizing predictive models and redundant switching states, while

maintaining balanced grid currents. Additionally, strategies for minimizing switching frequency were implemented via carrier waveform selection and the integration of a switching penalty term in the MPC cost function, significantly decreasing unnecessary commutations and related losses.

The inherent power balancing constraints of the CHB converter were then established utilizing an average power model. These constraints define the permissible operational region wherein DC-link voltage balance is attainable. Analytical expressions were derived that connect individual cell powers to overall phase power and duty cycle limits, offering significant understanding of the inherent limitations of CHB systems under uneven loading conditions.

From these findings, the chapter presented an optimization-based energy management strategy for the integrated BES modules. A quadratic cost function was developed to minimize BES power exchange, which decreases battery deterioration, while simultaneously managing the state of charge (SoC) of each module towards a specified reference. The permissible power limitations of the CHB converter, along with the EV charging requirements, were integrated as linear inequality constraints. This resulted in a quadratic programming (QP) problem, the solution of which provides optimal BES power references in real time. The suggested formulation guarantees that the CHB-AFE functions within its feasible region, even during extreme and rapidly varying charging circumstances.

This chapter provides an unified control and optimization system that integrates classical voltage-oriented control, predictive DC-link voltage balancing, and optimal battery energy storage management. The proposed methodology facilitates reliable, effective, and scalable operation of the CHB-based XFC stations, while specifically addressing converter limitations, battery longevity factors, and real-time operation requirements.

References 4

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Chapter 5:

Simulation and Experimental Results

5.1 Introduction

This chapter presents a comprehensive validation of the proposed control strategy for the cascaded H-bridge (CHB) rectifier integrated with battery energy storage (BES) for XFC station. The performance of the system is evaluated through detailed MATLAB/Simulink simulations and supported by experimental observations.

The analysis is structured to progressively assess the effectiveness of the developed control framework under both steady-state and dynamic operating conditions. First, the DC-link voltage balancing capability is examined, with particular emphasis on the imposed balancing limits and the performance of the proposed voltage balancing algorithm. This evaluation verifies the controller's ability to maintain voltage stability across all CHB cells under varying load conditions.

Subsequently, a comparative analysis of switching frequency is conducted to highlight the advantages of the proposed modulation and control approach in terms of switching stress and efficiency. The results demonstrate how the control strategy achieves an improved trade-off between performance and switching losses.

Finally, the "The optimal control strategy developed for the BES module, as described in the previous chapter, is validated through MATLAB/Simulink simulations for a 7-level CHB-AFE system..."battery energy storage (BES) management strategy for XFC station application is analyzed under realistic operating scenarios, including electric vehicle (EV) arrival and departure events. A step-by-step analysis of system response is provided, detailing the evolution of BES power, CHB cell power distribution, and SoC dynamics. Furthermore, it is demonstrated that the proposed control strategy successfully maintains system operation within the defined admissible region, ensuring stable and reliable performance during transient conditions.

Overall, this chapter validates the robustness, efficiency, and practical applicability of the proposed control architecture for Extreme fast electrical vehicle charging station.

5.2 Simulation Results

This section presents the simulation-based validation of the proposed control architecture for the cascaded H-bridge (CHB) rectifier integrated with battery energy storage (BES). The results are organized to evaluate the effectiveness of the developed methods in terms of DC-link voltage balancing, switching comutation reduction, and optimal BES management.

The overall simulation model of the system under investigation is illustrated in figure 5.1. The model incorporates the CHB rectifier topology, the associated BES modules, and the complete control architecture including voltage regulation, current control, and the proposed balancing strategy.

The key simulation parameters used in this study are summarized in Table 5.1.

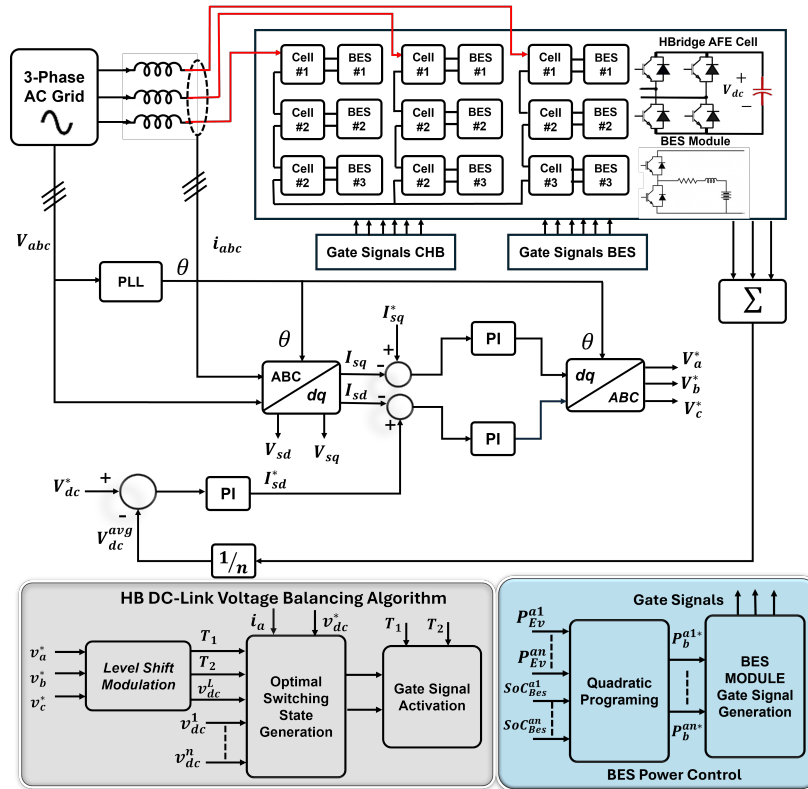


Figure 5.1: Block diagram for simulation setup of 7-level CHB-AFE with integrated BES

Table 5.1: Multilevel CHB-AFE and BES Module Simulation Setup Parameters

CHB-AFE Parameters		BES Parameters	
$V_{LL,rms}$	3.3 kV	L_f	2 mH
f	50 Hz	R_f	0.1 m Ω
f_{sw}	10 kHz	SoC*	50 %
L_s	2 mH	C_b	1.2 Ah
R_s	0.1 m Ω	V_b	400 V
C	3700 μ F	λ	10^4
V_{dc}^*	1050 V		
n	3		
S_t	2.56		
λ_{sw}	0.01		

Table 5.2: Simulation Control Parameters

Voltage PI		Current PI		BES (DC-DC) PI	
K_p	K_i	K_p	K_i	K_p	K_i
5	150	30	300	40	500

5.2.1 Validation of DC-link Voltage Algorithm and Balancing Limits

The effectiveness of the proposed control strategy and the associated analytical framework is validated through detailed simulations and depicted in figure 5.1. To clearly illustrate the behavior of the "The optimal control strategy developed for the BES module, as described in the previous chapter, is validated through MATLAB/Simulink simulations for a 7-level CHB-AFE system..." control algorithm, a 7-level cascaded H-bridge (CHB) rectifier is considered. It is important to note that the proposed control strategy is inherently scalable and can be extended to systems with a higher number of H-bridge cells. Moreover, without loss of generality, the analysis is carried out considering only phase- a , as all three phases exhibit identical behavior under balanced conditions.

In order to evaluate the performance of the DC-link voltage regulation and the proposed voltage balancing limits, four distinct operating points are selected and represented in figure 5.2. Initially, at $t = 0.1$ s, the CHB-AFE operates under balanced loading conditions, where each H-bridge cell processes an equal power of 50 kW. This operating point is indicated by the blue marker in figure 5.2, representing a nominal and symmetric

operating condition within the admissible region.

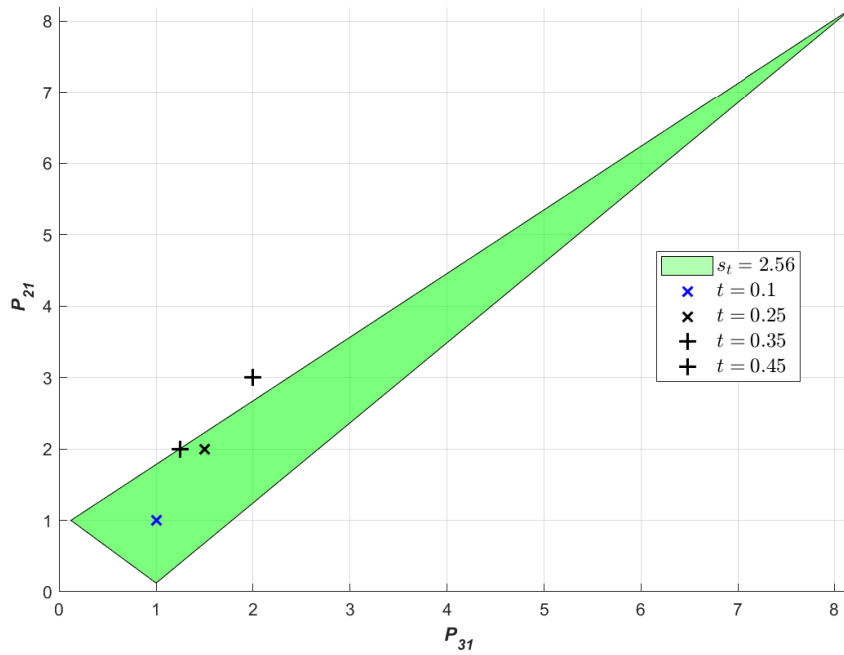


Figure 5.2: Voltage balancing limits of 7level CHB-AFE rectifier

Subsequently, the operating point of the CHB-AFE is intentionally perturbed to evaluate the dynamic response of the control system. Specifically, at $t = 0.25$ s, the operating condition transitions from the initial balanced point to a new operating point (black marker), where the individual H-bridge cells process unequal power levels of 50 kW, 100 kW, and 75 kW, respectively. This transition represents a non-uniform loading scenario, which challenges the voltage balancing mechanism and tests the robustness of the proposed control strategy.

It can be observed in figure 5.3 that, despite the abrupt change in power distribution among the cells, the DC-link voltages exhibit a well-damped transient response and rapidly converge to their respective reference values. This clearly demonstrates the effectiveness of the proposed voltage balancing algorithm in maintaining stable operation within the defined balancing limits.

Furthermore, the CHB-AFE maintains unity power factor operation at these operating points, as evidenced in figure 5.3(d), where the grid voltage and current remain in phase. This confirms that the proposed control strategy preserves input power quality while simultaneously achieving voltage balancing and power redistribution.

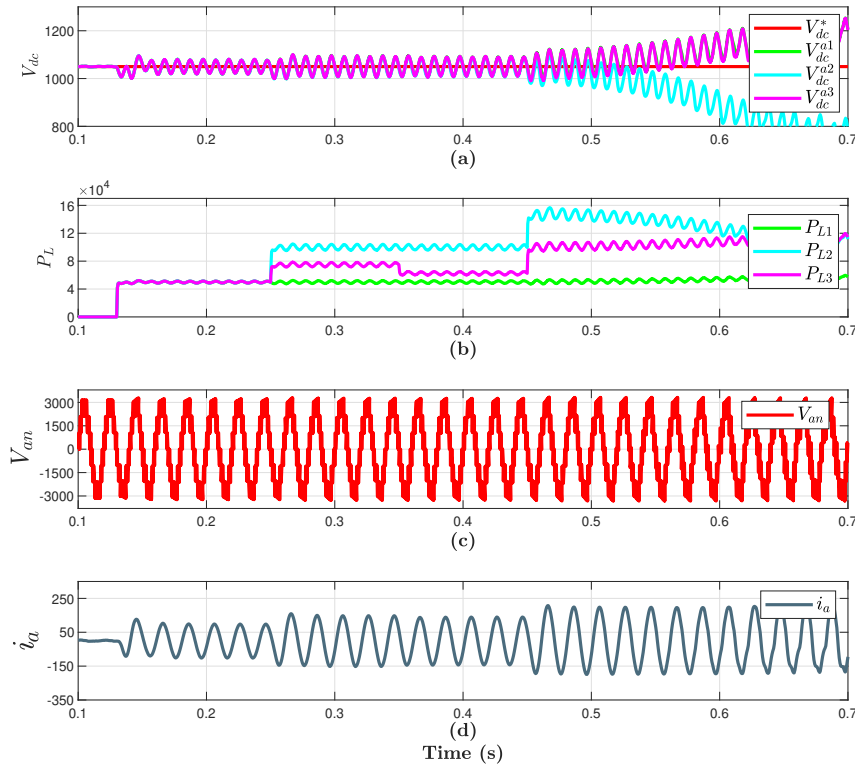


Figure 5.3: CHB-AFE behaviour under full load. a) DC-link voltage. b) Load Power. c) Phase to neutral voltage. d) Grid current

The resulting multistep output voltage waveform is illustrated in figure 5.3(C). The waveform exhibits the characteristic stepped structure of a multilevel converter, corresponding to the discrete voltage levels generated by the cascaded H-bridge cells. Each voltage level is synthesized through the appropriate combination of individual cell voltages, as dictated by the modulation and control strategy.

Notably, even under unbalanced power conditions, the multistep waveform retains its symmetry and quality, indicating that the proposed balancing algorithm does not distort the output voltage profile. The uniform distribution of voltage steps and the absence of irregular transitions confirm that the switching states are properly coordinated. This ensures low harmonic distortion and validates that the converter operates within its intended modulation range despite variations in cell power. Additionally, the preservation of the multilevel structure under dynamic conditions further highlights the robustness of the proposed control approach

Moreover, to further investigate the DC-link voltage balancing limits, two additional operating points located near and beyond the feasibility boundary are analyzed and in-

indicated by + marker in figure 5.2. At $t = 0.35$ s, the operating point is shifted towards the boundary of the feasible region (black + marker). It is observed that the proposed control algorithm is still capable of maintaining voltage balance under these boundary conditions, although with increased control effort and slightly degraded transient performance.

However, when the operating point is further pushed outside the feasible region at $t = 0.45$ s, the control algorithm is no longer able to regulate the DC-link voltages at their reference values. As a result, the voltages begin to diverge, clearly indicating the existence of physical and control-imposed limits of the system. This validates the analytical balancing limits derived earlier and highlights the importance of operating within the admissible region.

Finally, the switching commutation behavior of the proposed control strategy is evaluated for all operating scenarios. As shown in figure 5.4 by the red line, when a conventional triangular carrier-based implementation is used without incorporating a switching penalization term in the cost function, the resulting switching commutations are significantly high, where the average switching commutations are computed considering only switches 1 and 3 of each H-bridge in phase A.

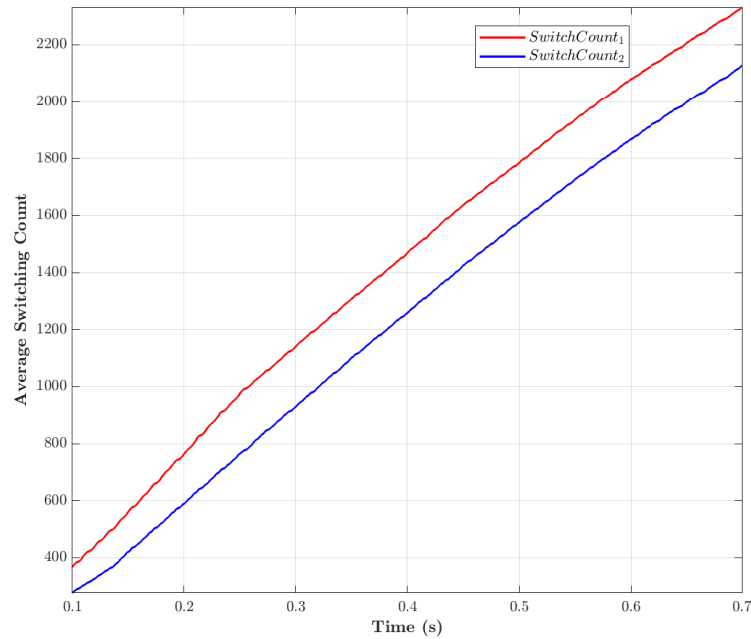


Figure 5.4: Average switching commutations of CHB-AFE

In contrast, by employing a sawtooth carrier along with the modified cost function presented in equation (4.64), a substantial reduction in switching transitions is achieved. The switching commutations are reduced by approximately 8.54%, while still preserving the voltage balancing performance and dynamic response. This demonstrates that the proposed modification effectively improves the overall efficiency of the system by reducing switching losses without compromising control objectives. The CHB-AFE rectifier behaviour under sawtooth carrier is illustrated in 5.5.

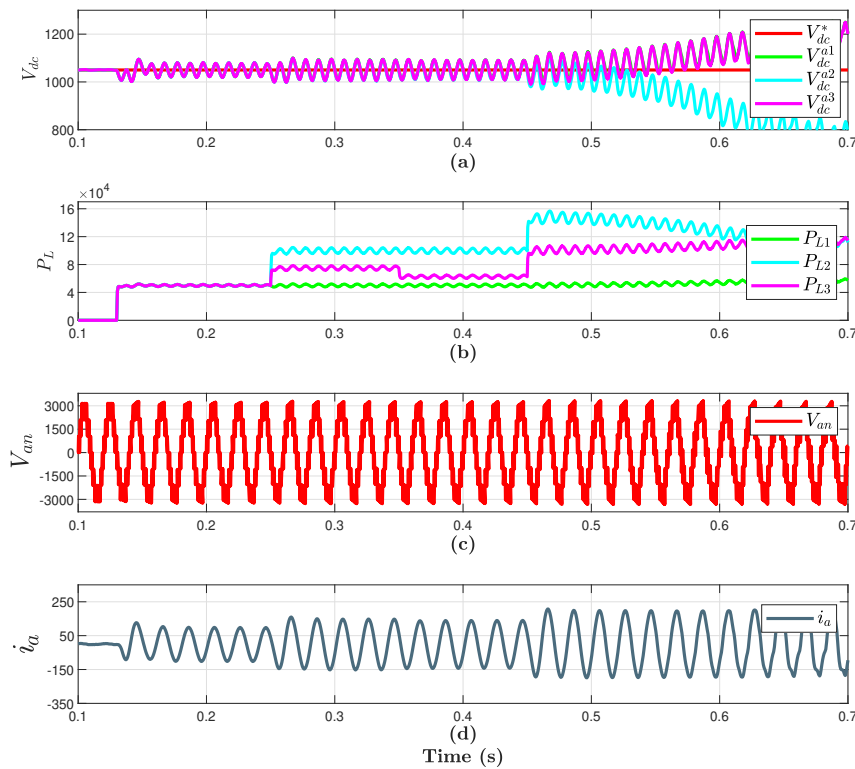


Figure 5.5: CHB-AFE behaviour under full load with sawtooth carrier

5.2.2 Validation of Optimal Management of BES Module

EV charging demand at stations is unpredictable and highly dynamic. This variability is primarily influenced by user behavior, dissimilarities in battery capacities, and the conditions in which the EV is connected to the charging station. For instance, domestic charging—usually conducted overnight—generally involves extended connection times at comparatively consistent, moderate power levels. Conversely, extreme fast charging during long-distance travel is characterized by short connection times yet considerably higher power requirements, often approaching the rated capacities of the charging in-

frastructure. In addition, variations in battery size, initial state of charge (SoC), and the irregular arrival of cars further increase the unpredictability of the total load profile.

Consequently, the power demanded from the grid-side converter could vary significantly over short intervals. The theoretical analysis and simulation findings in the preceding sections demonstrate that the CHB-AFE alone cannot reliably manage these variances. Instability arises when the system operates outside the feasible region defined by the DC-link voltage-balancing requirements.

As discussed earlier, to ensure that the operating point of the CHB-AFE remains within the feasible region—highlighted by the green-shaded area in Figure 4.16—a battery energy storage (BES) module is integrated into each H-bridge cell. This integration enables additional flexibility in power management and supports stable operation under extreme fast charging (XFC) conditions.

The optimal control strategy developed for the BES module, as described in the previous chapter, is validated through MATLAB/Simulink simulations for a 7-level CHB-AFE system. The overall simulation setup and control architecture are illustrated in Figure 5.1.

The optimal control strategy developed for the BES module, as described in the previous chapter, is validated through MATLAB/Simulink simulations for a 7-level CHB-AFE system. The overall simulation setup and control architecture are illustrated in Figure 5.1.

To evaluate the effectiveness of the proposed optimal BES power management method, identical operating scenarios with similar operational parameters are adopted. Consequently, any deviations observed in the BES power distribution, SoC progression, and operating point trajectory can be directly attributed to the proposed optimization technique rather than to variations in the simulation configuration. This section compares the simulation results with the control methodology presented in [1] to illustrate the benefits of the proposed method. However, the implementation details of the gain scheduling for the proportional gain of the SoC controller are not fully disclosed in [1]. Therefore, a fixed value of K_p is considered for this comparison throughout this thesis.

A low-capacity battery (1.2 Ah) is used for each battery energy storage (BES) module to provide faster observation of state-of-charge (SoC) dynamics within a shortened simulation duration. This selection is made exclusively for simulation purposes and does

not influence the core functionality of the proposed control method. The battery capacity predominantly affects the rate of State of Charge (SoC) variation, whereas the power reference for each Battery Energy Storage (BES) module is independently established by the quadratic programming (QP)-based control algorithm. Consequently, reducing the battery capacity facilitates a more rapid evolution of the SoC dynamics, thereby simplifying the assessment of the control strategy within a shorter simulation time.

A time-scaling approach is employed in the simulations to enhance computational efficiency and illustrate the system dynamics. For consistency and to ensure a fair comparison, the same time-scaling approach is adopted for both the proposed method and the reference control strategy presented in [1]. A scaling factor of 1:10 is employed, indicating that 1 s of simulation time corresponds to 10 min of actual operating time. This approach enables realistic EV charging scenarios, which typically span several minutes, to be represented within a practical simulation duration without compromising the fundamental control performance or system dynamics.

To conduct a fair comparison, it is assumed that multiple electric vehicles (EVs), characterized by different battery capacities and charging requirements, arrive at and depart from the charging station at identical time instants for both control strategies. Specifically, EVs arrive at charging ports 1, 2, and 3 at $t = 1.0$ min, $t = 6.0$ min, and $t = 8.0$ min, respectively, and depart at $t = 11.0$ min, $t = 13.0$ min, and $t = 14.0$ min in the same sequence.

The first EV remains connected for approximately 10 minutes, representing a high-energy-demand scenario in which the vehicle requires substantial charging. This results in a relatively high and sustained power demand from the charging station. The second EV arrives later and is assumed to require less energy, leading to a reduced charging power demand. The third EV arrives while the other vehicles are still being charged, creating a peak loading condition. However, it is characterized by a lower power requirement, which can correspond to a partial-charge scenario or a higher initial state of charge (SoC).

The combination of sequential arrivals, overlapping charging periods, and fluctuating power requirements generates an identical and highly dynamic loading profile for proposed control strategies, as depicted in Fig. 5.6(a).

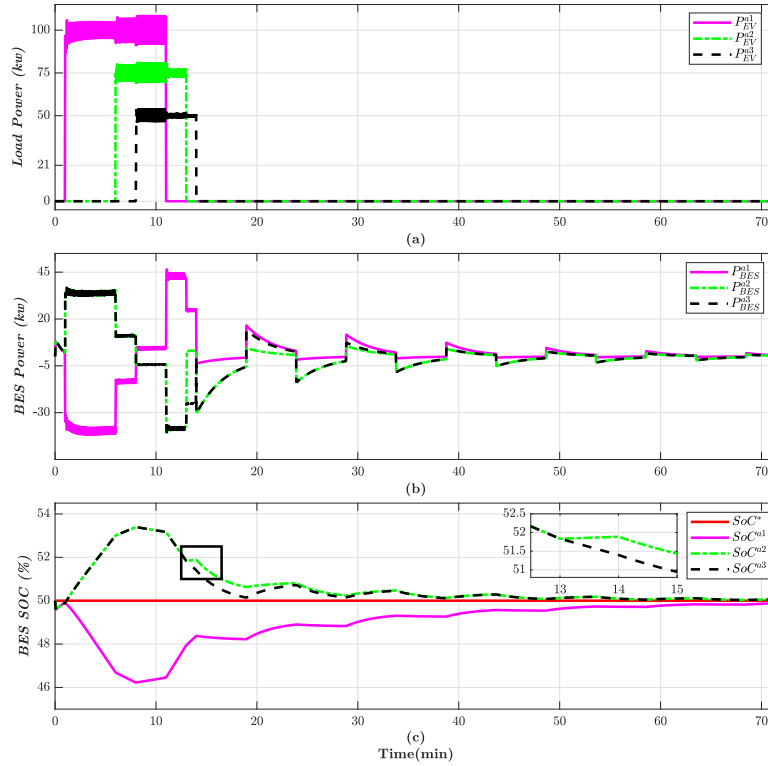


Figure 5.6: Simulation results of a hypothetical profile of a charging station. a) Power demand on the charging ports. b) Optimal power required to the BES. c) BES module SoCs.

As illustrated in figure 5.6 upon the connection of the initial EV with a power demand of 100 kW to the charging port, the associated BES module instantaneously shifts to discharging mode to provide the necessary power. The BES functions as a local power buffer, mitigating abrupt surges in load demand and ensuring that the CHB-AFE remains within its operational limits. Simultaneously, the remaining BES modules function in charging mode, absorbing surplus power and contributing to system level power balancing.

A similar behavior is observed with the introduction of the second and third electric vehicles, which have power requirements of 75 kW and 50 kW, respectively. The BES modules proficiently help to keep power within the feasible limits, alleviating stress on the CHB-AFE and ensuring stable operation.

Conversely, once the electric vehicles depart, the corresponding load demand is eliminated, prompting the associated battery energy storage modules to shift from discharging to charging mode. In this phase, the BES draws power from the grid to replenish its

state of charge (SoC). After all electric vehicles have left and the charging ports are vacant, the optimal control strategy allocate the BES module power references to equalize the state of charge of all modules, directing them towards their reference values until $t = 71$ min, while maintaining the CHB-AFE operating point within the permissible region.

To facilitate a more detailed analysis, Fig. 5.7 illustrates the investigated scenario during EV arrivals and departures, focusing on the first 20 minutes of operation.

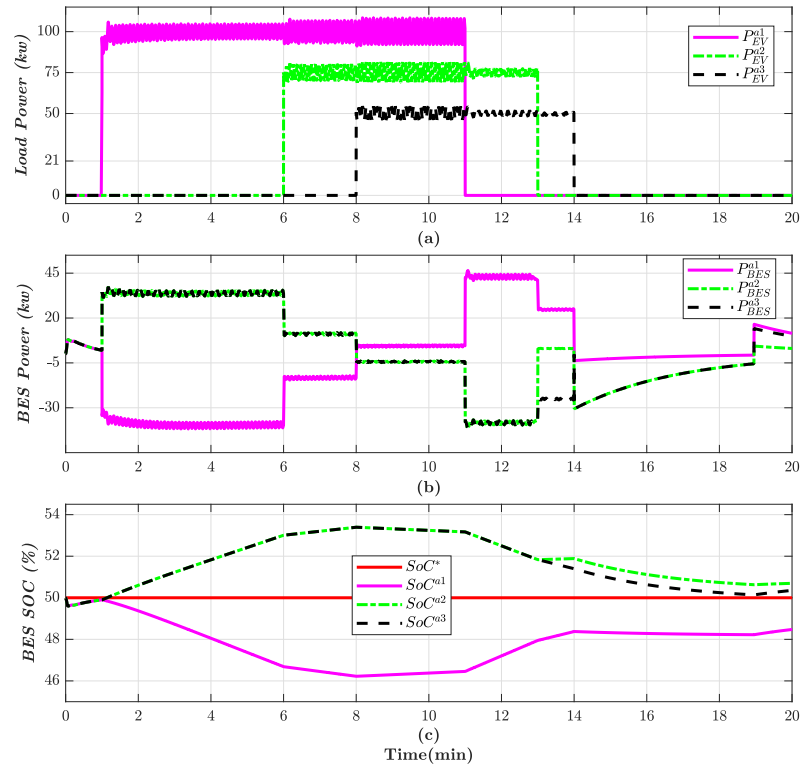


Figure 5.7: Zoom results of a hypothetical profile of a charging station. a) Power demand on the charging ports. b) Optimal power required to the BES. c) BES module SoCs.

This behavior highlights the effectiveness of the proposed control strategy for the BES modules, enabling the decoupling of highly fluctuating EV demand from the grid-side converter and using the BES module only when needed.

Figure 5.6b shows that chattering-like behavior appears in the BES power profiles starting at approximately $t = 19$ min. This behaviour is primarily associated with the intrinsic operational constraints of the CHB-AFE, as discussed earlier. In this operating region, the optimal BES power reference is determined using two quadratic programming formulations, denoted as QP_1 and QP_2 , corresponding to charging and discharg-

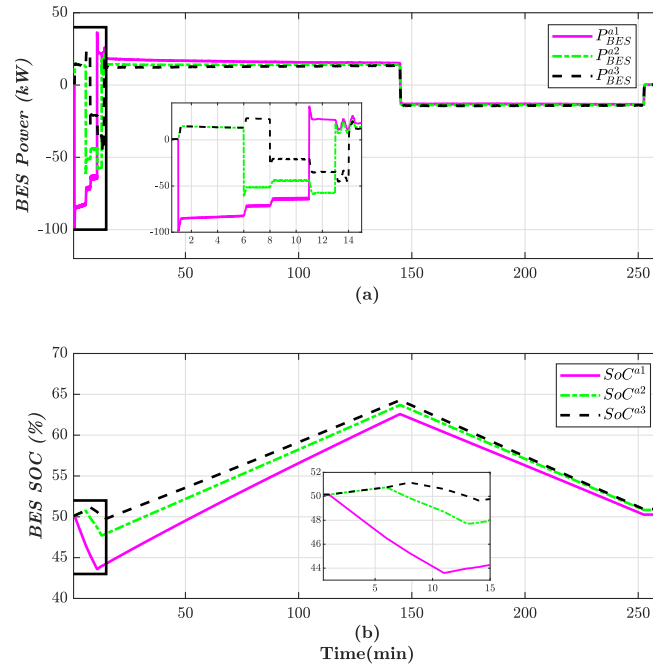


Figure 5.8: BES module response during the EV charging scenario: a)BES module power allocation.b)SoC evaluation

ing modes, respectively.

Under CHB-AFE constraints, the power flow within a given interval must remain unidirectional; that is, all cells must either absorb or deliver power simultaneously. As a result, mixed operation—where some cells charge while others discharge—is not permissible. Around $t \approx 19$ min, the SoC balancing term in the cost function drives the BES modules toward their reference values. However, this objective creates a conflicting requirement: for instance, one CHB cell may require positive power (charging), while others require negative power (discharging). Due to the unidirectional power flow constraint, such a condition cannot be satisfied simultaneously.

Consequently, the optimal solution alternates between QP_1 and QP_2 , leading to rapid switching in the BES power reference. To suppress this undesired behaviour, a dwell-time constraint is introduced. Once a QP formulation is selected, it is enforced for a minimum duration of 5 minutes before switching is permitted. For example, at $t \approx 19$ min, the solution transitions from QP_2 to QP_1 , after which QP_1 remains active for the specified interval.

Moreover, Figure 5.9 shows the activation of the proposed quadratic programming

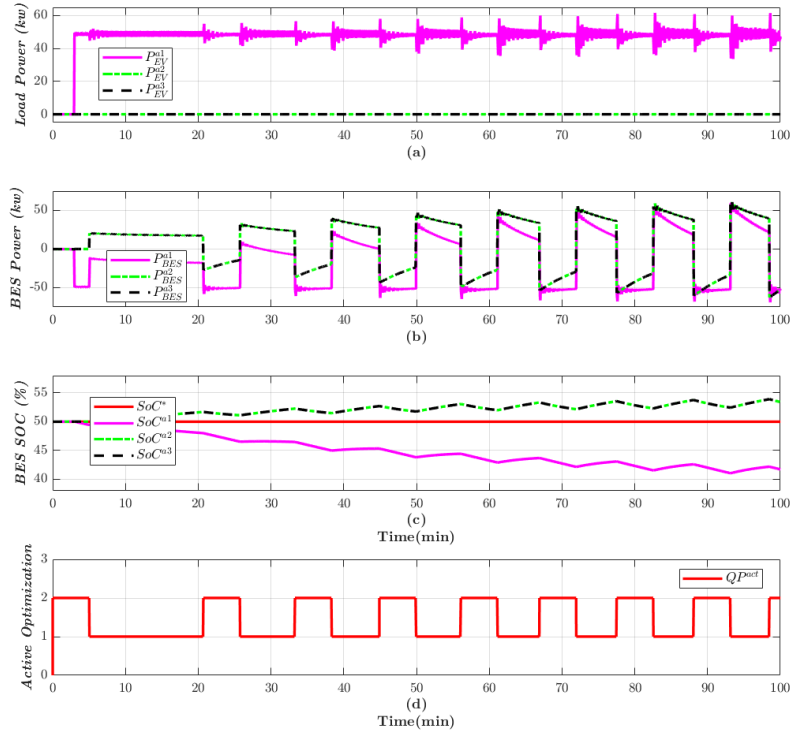


Figure 5.9: Simulation results of Active optimization and SoC behavior in worst-case scenario: a) EV Power, b) BES module Power, c) BES module SOC, d) ACTIVE QP

(QP) optimization under the worst-case scenario in which only one EV is connected to the XFC station for an extended period. The optimization objective is updated adaptively based on the BES modules' operational conditions. The SoC profiles show that the BES module associated with the corresponding charging port first provides the required power smoothly, causing its SoC to decrease continuously. When the SoC deviates sufficiently from the reference value, the optimization applies switching behavior to keep the battery SoCs as close as possible to the reference, thereby stabilizing them at the nearest optimal value. This optimal value is determined by λ , which defines the maximum allowable deviation of the stabilized SoC from the reference value.

This dwell-time mechanism effectively reduces high-frequency switching between optimization modes, thereby mitigating chattering and improving overall system stability. The dwell duration is a changeable parameter and can be adjusted based on system requirements and desired dynamic response.

For comparison, the BES power allocation and SoC evolution obtained using the control strategy presented in [1] are illustrated in Fig. 5.8. Since both control strategies are evaluated under identical loading conditions, the charging and discharging sequences

of the BES modules remain essentially the same. However, a noticeable difference is evident in the distribution of battery power among the BES modules. In the reference strategy, the BES module associated with the higher-power charging port is required to supply a larger portion of the charging demand, resulting in a significantly higher discharge than the other BES modules. Consequently, under prolonged operation or worst-case charging scenarios, where a single charging port remains active for an extended duration, the corresponding BES module may reach its minimum allowable SoC limit before the other modules. Such an imbalance reduces the affected BES module's available energy reserve and may limit the charging station's continuous operation. Moreover, as illustrated in Fig. 5.8, once all EVs have departed from the charging station, all BES modules are first charged using a predefined charging power and subsequently discharged to restore their nominal SoC reference. This additional charging and discharging process introduces unnecessary cycling of the BES modules, which may accelerate battery degradation and reduce their service life.

In contrast, the proposed QP-based power management strategy distributes the charging demand more effectively among the available BES modules by explicitly accounting for both the SoC-balancing objective and the CHB-AFE operating constraints. As a result, excessive depletion of an individual BES module is avoided, leading to a more balanced SoC evolution and improved utilization of the distributed energy storage system.

To further elucidate the behavior of the proposed control method, Figure 5.10 illustrates the evolution of the H-bridge power ratios during the analyzed scenario. This depiction plots the ratio $\frac{P_{HB}^{a2}}{P_{HB}^{a1}}$ on the horizontal axis and $\frac{P_{HB}^{a3}}{P_{HB}^{a1}}$ on the vertical axis, offering a normalized perspective of power distribution among the converter cells. It is worth noting that a total of 13 operating points are considered in the power-balancing analysis to avoid excessive overlap and improve visualization clarity. Furthermore, the BES power references are extracted under steady-state conditions rather than during transient intervals, ensuring a fair and consistent comparison of the system operating points. BES power profile showing the selected steady-state operating points (circled), from which power values are extracted to construct the points on operating limits in the CHB-AFE feasible region figure, is illustrated in Figure 5.11.

The shaded area delineates the feasible operational domain of the CHB-AFE, where

steady state operation and DC-link voltage equilibrium are guaranteed. The coloured markers denote the trajectory of the system's operating point over time in the hypothetical extreme fast charging (XFC) scenario.

For comparison, the corresponding operating-point trajectory obtained with the control strategy presented in [1] is shown in Fig. 5.12. Under identical charging conditions, the operating points remain concentrated near (1, 1) throughout the charging process because each BES module is managing average Phase power. Moreover, it can be seen that the points are not exactly at (1, 1) but near (1, 1), This behavior is primarily due to the use of a fixed proportional gain in the SoC controller, which results in a less adaptive redistribution of the BES power among the H-bridge cells. Consequently, only small variations in the H-bridge power ratios are observed.

To further elucidate the behaviour of the proposed control method, Fig. 5.10 illustrates the evolution of the H-bridge power ratios during the analysed scenario. The ratios $\frac{P_{HB}^{a2}}{P_{HB}^{a1}}$ and $\frac{P_{HB}^{a3}}{P_{HB}^{a1}}$ are plotted on the horizontal and vertical axes, respectively, providing a normalized representation of the power distribution among the converter cells. A total of 13 operating points are selected for the power-balancing analysis to avoid excessive overlap and improve visualization clarity. Furthermore, the BES power references are extracted under steady-state operating conditions rather than during transient intervals, ensuring a fair and consistent comparison of the system operating points. The corresponding BES power profile from which these steady-state operating points are extracted is illustrated in Fig. 5.11.

The shaded region represents the feasible operating domain of the CHB-AFE, within which steady-state operation and DC-link voltage balancing are guaranteed. The coloured markers indicate the trajectory of the operating point throughout the hypothetical extreme fast charging (XFC) scenario.

For comparison, the corresponding operating-point trajectory obtained using the control strategy presented in [1] is shown in Fig. 5.12. Under identical charging conditions, the operating points remain concentrated in the vicinity of (1, 1) throughout the charging process. This behaviour results from the use of a fixed proportional gain in the SoC controller, which provides limited adaptability in the redistribution of BES power among the H-bridge cells. Consequently, only small variations in the H-bridge power

ratios are observed, and the operating points remain clustered around the nominal operating point.

In contrast, the QP-based optimization redistributes BES power more effectively among the H-bridge cells by utilizing the entire available power imbalance range of CHB-AFE. Consequently, the operating points utilize a wider portion of the feasible operating region while remaining entirely within its admissible boundaries. This demonstrates the improved flexibility of the proposed control strategy in allocating power according to the system operating requirements without violating the analytical operating constraints of the CHB-AFE.

Despite the highly dynamic and stochastic nature of EV charging demand, all operating points remain within the feasible operating region throughout the charging process. These results confirm that the proposed optimization strategy efficiently distributes power among the H-bridge cells while preserving DC-link voltage balance and respecting the inherent operating limits of the CHB-AFE rectifier.

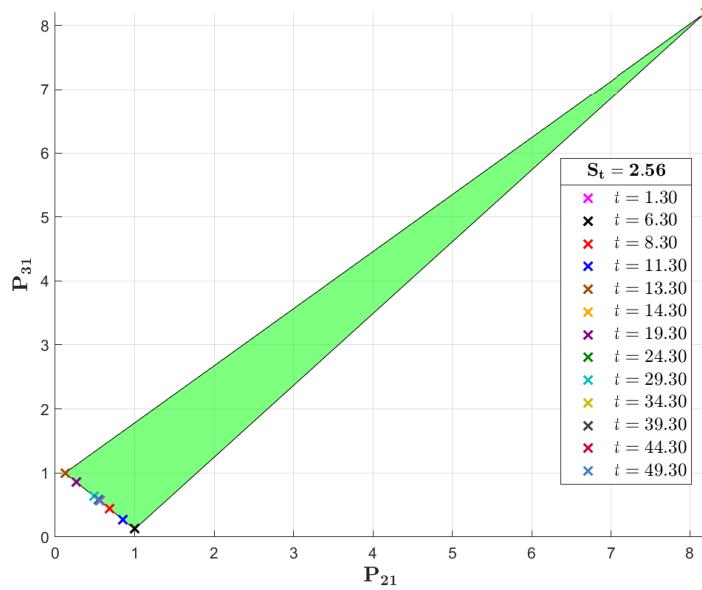


Figure 5.10: Operating points evolution of CHB-AFE rectifier under hypothetical scenario of EV XFC station

Figure 5.13 illustrates the steady-state performance of phase a of the CHB-AFE under full-load conditions with the proposed optimal control strategy. This operating position presents a challenging situation in which the converter must deliver maximum power while maintaining DC-link voltage balance and ensuring superior power quality at the

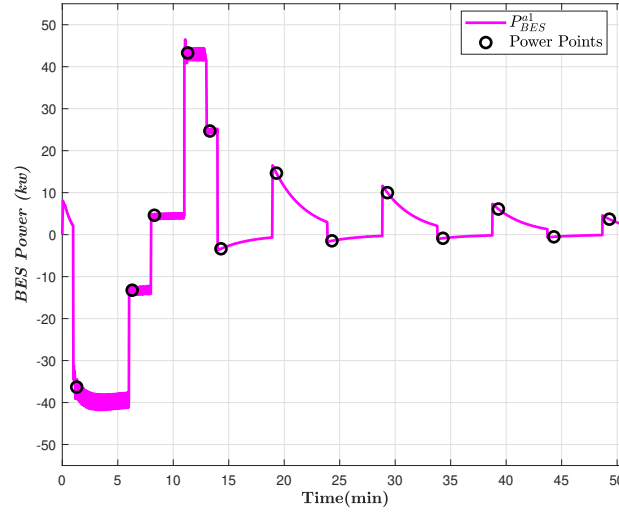


Figure 5.11: BES module-selected steady-state points used for feasible region analysis.

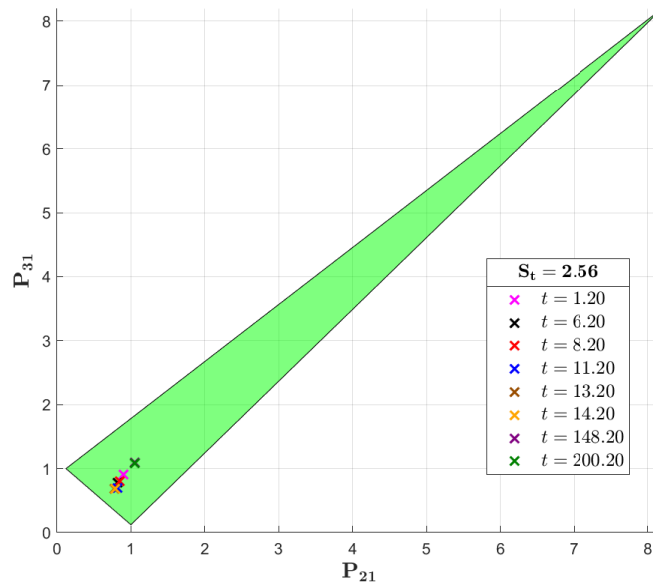


Figure 5.12: Evolution of CHB-AFE operating points obtained with the control strategy presented in [1]

grid interface.

It can be noticed from 5.13(a) that the DC-link voltages of all H-bridge cells are consistently maintained near their reference value. Notwithstanding the presence of intrinsic second-order ripple components, the voltages exhibit negligible variation and remain in equilibrium across all cells. This validates the efficacy of the proposed voltage-balancing technique in ensuring consistent energy distribution across the DC_link, even

under full-load conditions.

The output phase voltage of the CHB-AFE, depicted in Figure 5.13(b), displays a distinct multilevel stepped waveform, typical of cascaded H-bridge converters. This multilevel architecture significantly enhances the quality of the voltage waveform by diminishing harmonic content.

Figure 5.13(c) illustrates the associated grid-side phase current. The current is sinusoidal and precisely aligned with the grid voltage, exhibiting nearly negligible phase displacement. This indicates that the converter operates at unity power factor, ensuring efficient power transfer. Moreover, the smooth current waveform with minimal distortion indicates that the phase currents have minimal harmonics and maintains power quality during full-load operation.

These results demonstrate that the CHB-AFE with integrated BES module, attains precise DC-link voltage management, equitable power distribution among cells, and superior grid current injection, even under various load conditions.

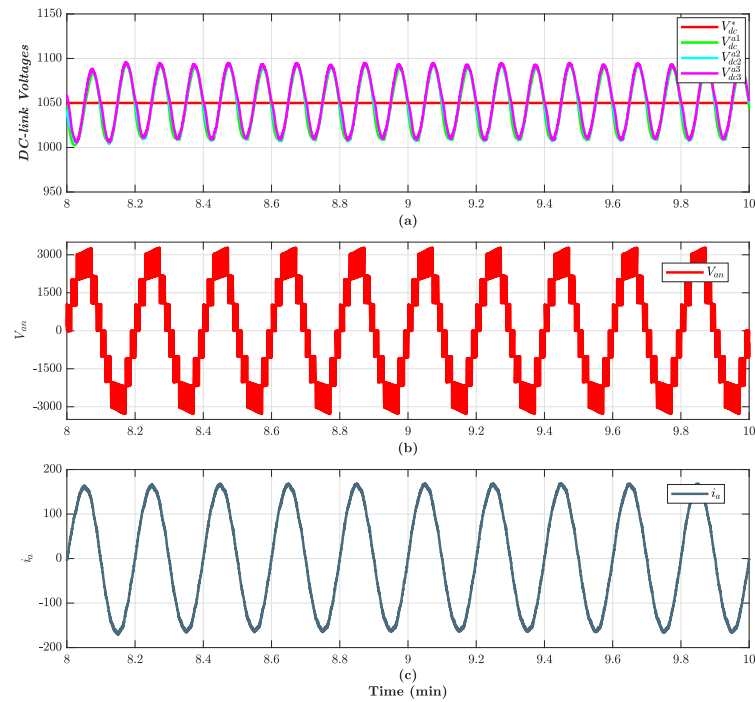


Figure 5.13: CHB-AFE behaviour under full load. a) DC-link voltage. b) Phase to neutral voltage. c) Grid current

5.3 Experimental Results

To further validate the effectiveness of the proposed control strategy under practical operating conditions, experimental tests are conducted on a laboratory-scale prototype of the cascaded H-bridge active front-end (CHB-AFE) converter. While the simulation results provide initial verification of the control performance, experimental validation is essential to account for non-idealities such as switching delays, measurement noise, and parameter uncertainties.

The experimental setup consists of a multilevel CHB-AFE system with integrated battery energy storage (BES) modules, controlled using a dSpace controller. The proposed voltage-balancing and optimal BES management strategies are implemented and tested under various operating conditions, including balanced and unbalanced loading scenarios and dynamic load variations representative of extreme fast charging (XFC) applications.

The objective of this section is to demonstrate the capability of the proposed control approach to maintain DC-link voltage balance, ensure stable operation within the feasible region, and achieve high power quality at the grid interface under realistic conditions. The key experimental results, including DC-link voltage behavior, grid voltage and current waveforms, and power distribution among H-bridge cells, are presented and discussed in the following subsections.

5.3.1 Experimental Setup

The proposed control strategy is experimentally proven through real-time implementation on a laboratory-scale single-phase 7-level cascaded H-bridge (CHB) prototype. Chapter 4 elucidates that the CHB-AFE system experiences two forms of power imbalance: per-cell power imbalance and per-phase power imbalance. The per-cell imbalance is rectified by the suggested DC-link voltage balancing method, while the per-phase imbalance can be alleviated through parallel connection of isolated converter modules across different phases.

The main objective of this research is to validate the effectiveness of the suggested per-cell control methodology and the optimal management of battery energy storage

(BES) modules, with the experimental investigation carried out on a single-phase system. This approach simplifies implementation while maintaining the critical dynamics of DC-link voltage balancing and power redistribution among H-bridge cells. Furthermore, under balanced operating conditions, the characteristics of a three-phase system can be determined from single-phase analysis.

The control algorithms are implemented in real time using the dSPACE MicroLabBox platform. The control strategies "The optimal control strategy developed for the BES module, as described in the previous chapter, is validated through MATLAB/Simulink simulations for a 7-level CHB-AFE system..." in this work are executed on the main processor via the dSPACE real-time interface (RTI), while time-critical tasks such as pulse-width modulation (PWM) signal generation, fast input/output handling, and protection mechanisms are supported through FPGA resources. This hierarchical distribution of tasks ensures deterministic real-time performance and reliable operation of the converter. The MicroLabBox provides multiple analog and digital input/output interfaces, enabling direct acquisition of voltage and current measurements, as well as the generation of gating signals for the power semiconductor devices. The dSPACE MicroLabBox and associated hardware components are shown in Figure 5.14.

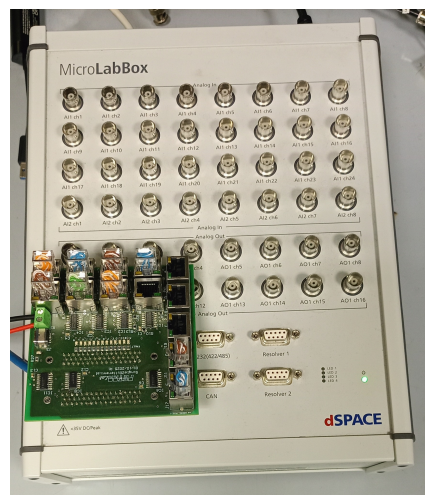


Figure 5.14: MicroLabBox dSpace

The 7-level CHB-AFE is realized by connecting three H-bridge modules in series, as depicted in figure 5.15. The converter is interfaced with a controllable AC grid through a coupling inductor, while a resistive load is connected on the DC side of each H-bridge cell.

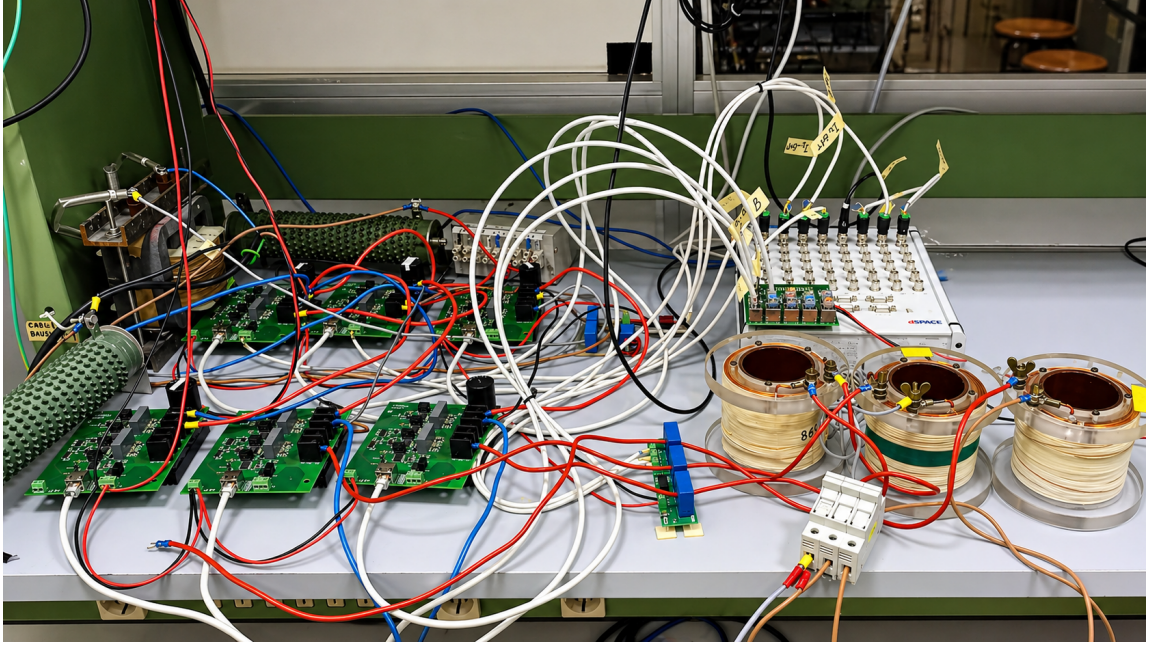


Figure 5.15: Experimental Setup of CHB-AFE converter with Integrated BES Module

In order to validate the proposed DC-link voltage balancing strategy and the analytically derived balancing limits, experimental tests are conducted under low-power conditions. However, the dynamic behavior of the system, including load variations and transient responses, is maintained consistent with the simulation scenarios to ensure a meaningful comparison. The overall schematic of the experimental setup is illustrated in figure 5.16, and the corresponding system parameters are summarized in Table 5.3 and table 5.4

Table 5.3: Multilevel CHB-AFE and BES Module Experimental Setup Parameters

Parameters		BES Parameters	
$V_{g,rms}$	105 V	L_f	0.864 mH
f	50 Hz	R_f	0.1 Ω
f_{sw}	10 kHz	f_{sw}	50 kHz
L_s	2 mH	C_b	2 Ah
R_s	0.1 Ω	V_b	50 V
C	1 mF	λ	100
V_{dc}^*	70 V	SoC*	50 %
n	3		
S_t	2.12		
λ_{sw}	0.01		

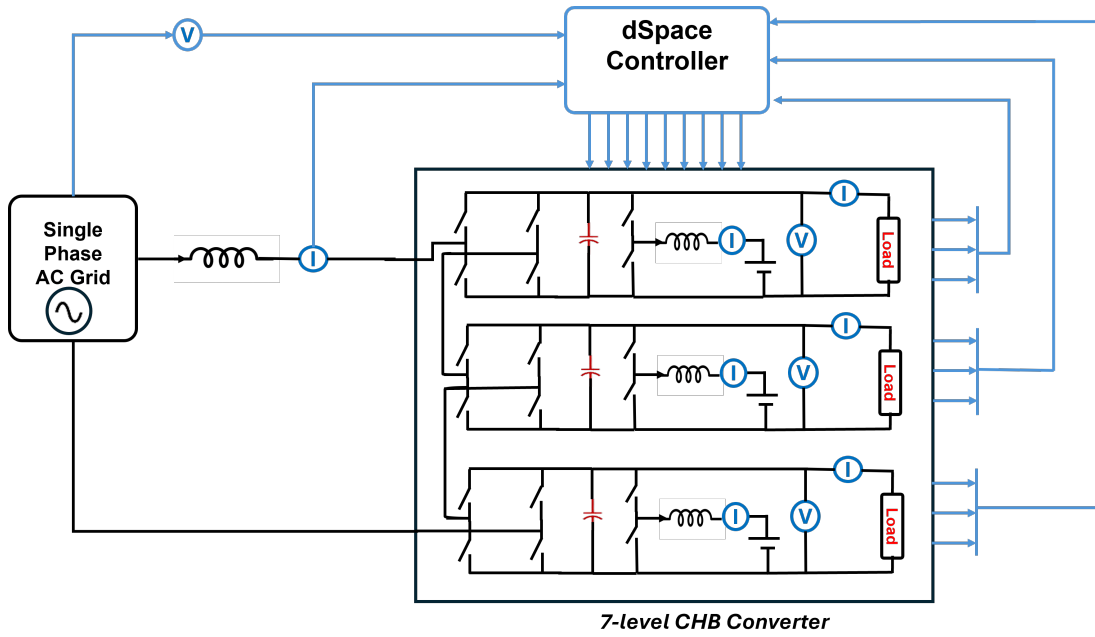


Figure 5.16: Block diagram of experimental setup of 7-level CHB-AFE with Integrated BES

Table 5.4: Experimental Control Parameters

Voltage PI		Current PI		BES (DC-DC) PI	
K_p	K_i	K_p	K_i	K_p	K_i
2	60	20	400	30	700

5.3.2 Grid Synchronization Using Single-Phase PLL

Accurate synchronization with the grid voltage is important for the successful operation of the grid-connected CHB-AFE rectifier system. This is accomplished by a phase-locked loop (PLL), which offers real-time estimation of the grid voltage phase angle, as depicted in figure 5.18. The estimated phase angle is employed in the control system to synchronize the reference current with the grid voltage, thus guaranteeing unity power factor operation and reliable power exchange with the grid.

In three-phase systems, synchronization can be immediately attained by Clarke and Park transformations. In a single-phase system, only one voltage signal exists, necessitating the artificial generation of an orthogonal component to facilitate transfer into the rotating dq reference frame. This study derives the orthogonal signal by employing two low-pass filters (LPFs) calibrated to the fundamental grid frequency, specifically

$\omega = 2\pi \cdot 50$ rad/s. This method facilitates the creation of a virtual two-phase system, permitting the implementation of Park transition [2].

The Park transformation applied to the resulting orthogonal signals v_α and v_β allows the voltage components in the rotating dq frame to be articulated as:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (5.1)$$

where $\hat{\theta}$ represents the estimated phase angle of the grid voltage. By expressing the input voltages as $V_\alpha = V_m \cos(\theta)$ and $V_\beta = V_m \sin(\theta)$, the transformed voltages can be written as:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m \cos(\theta - \hat{\theta}) \\ V_m \sin(\theta - \hat{\theta}) \end{bmatrix} \quad (5.2)$$

For small phase error $(\theta - \hat{\theta})$, the q -axis component can be approximated as:

$$V_q \approx V_m(\theta - \hat{\theta}) \quad (5.3)$$

Thus, V_q is proportional to the phase error between the actual and estimated grid angles. By regulating V_q to zero using a proportional-integral (PI) controller, the phase error is minimized, ensuring that the estimated angle $\hat{\theta}$ accurately tracks the grid phase θ . Figure 5.17 illustrates the small signal model of PLL.

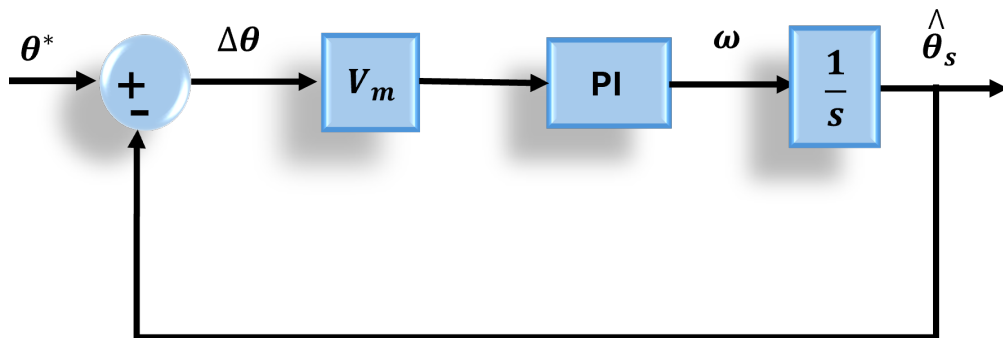


Figure 5.17: Small Signal closed loop model of PLL

The closed-loop dynamics of the PLL can be represented by a second-order system.

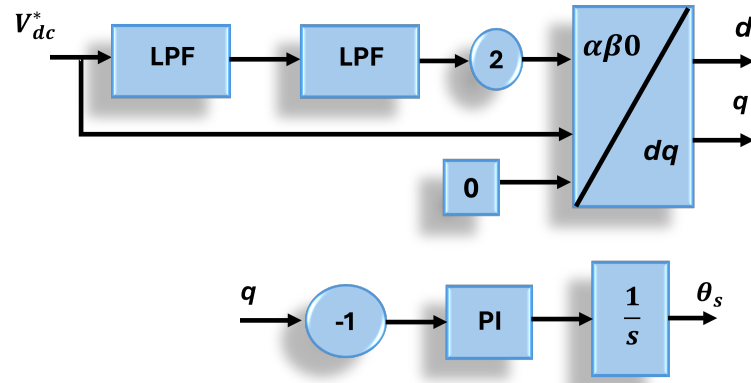


Figure 5.18: Block diagram of PLL for single-phase system

The small-signal transfer function of the PLL is given by:

$$\frac{\hat{\theta}(s)}{\theta(s)} = \frac{V_m k_p s + V_m k_i}{s^2 + V_m k_p s + V_m k_i} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (5.4)$$

where ω_n is the natural frequency and ζ is the damping ratio of the closed-loop system. These parameters are defined as:

$$\omega_n = \sqrt{V_m k_i}, \quad \zeta = \frac{k_p}{2} \sqrt{\frac{V_m}{k_i}} \quad (5.5)$$

The damping ratio is typically selected as $\zeta = 0.707$ to achieve a good trade-off between fast dynamic response and sufficient damping. The natural frequency ω_n determines the speed of the PLL response, where higher values result in faster tracking but reduced filtering capability.

In this work, the PLL parameters are selected based on the grid frequency of 50 Hz, resulting in $\omega_n = 2\pi \cdot 50 = 314$ rad/s. The corresponding PI controller gains are chosen to ensure stable and fast convergence of the phase angle under dynamic conditions.

The performance of the implemented PLL is validated experimentally, and the synchronization results are presented in figure 5.19. It can be observed that the estimated phase accurately tracks the grid voltage with negligible steady-state error, confirming the effectiveness of the proposed synchronization scheme.

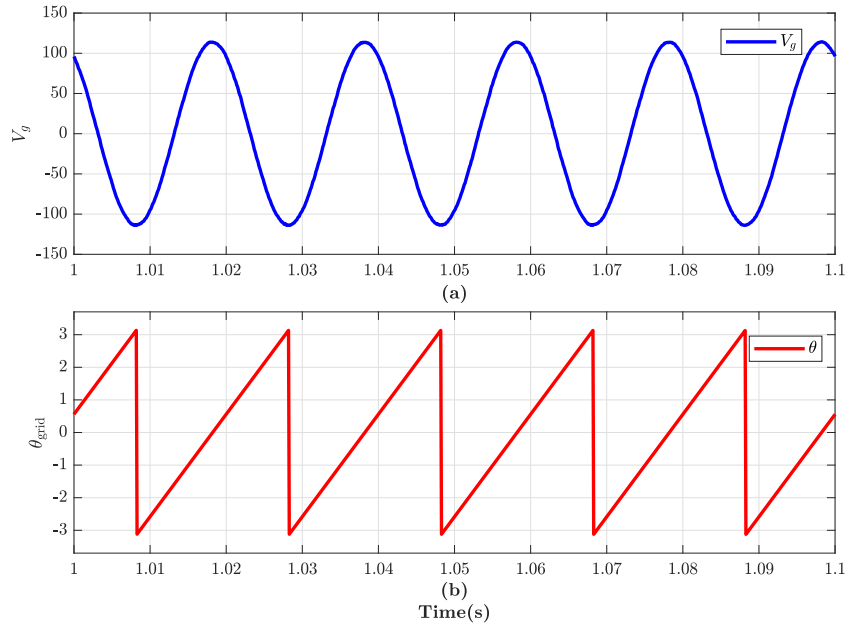


Figure 5.19: Experimental grid synchronization: (a) grid voltage v_g (b) estimated grid angle

5.3.3 Experimental Validation of DC-link Voltage Balancing Algorithm

Figure 5.20 illustrates the experimental validation of the proposed DC-link voltage balancing algorithm together with the analytically derived voltage balancing limits under different operating conditions. It should be noted that different time scales are used in figure 5.20(b) and figure 5.20(c). This is intentionally done to clearly illustrate the multilevel structure of the output voltage waveform and the corresponding grid current behavior. The zoomed-in time scale in 5.20(b) enables visualization of the stepped voltage waveform, while figure 5.20(c) highlights the sinusoidal nature of the grid current and its phase alignment with the voltage.

Initially, the CHB-AFE operates under balanced loading conditions, where identical loads are connected to all H-bridge modules. However, at $t = 2.5$ s, the CHB-AFE operation shifts to unbalanced loading, as highlighted by the black marker in figure 5.22. It can be observed that the DC-link voltages remain balanced at their predefined reference values under both conditions. Furthermore, the grid voltage and current are in phase, indicating unity power factor operation and proper synchronization with the grid.

To further validate the performance of the DC-link voltage balancing algorithm and the analytically derived feasibility limits under out-of-bound operating conditions, an

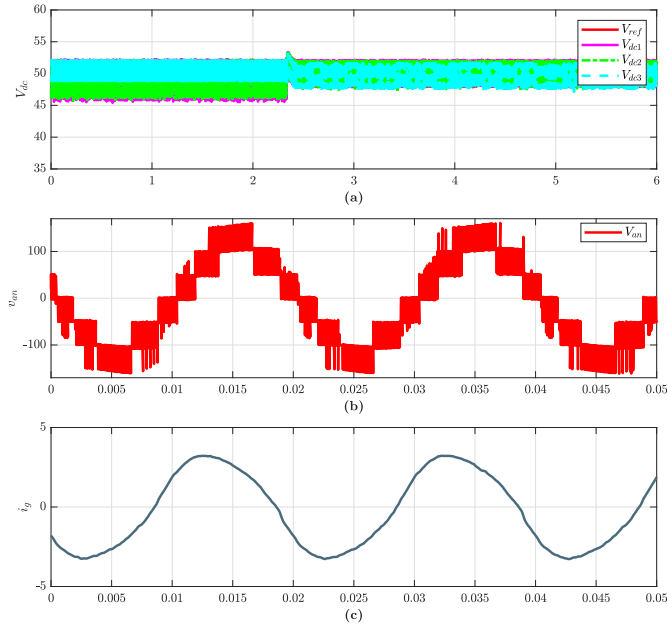


Figure 5.20: CHB-AFE behaviour in feasible region. a) DC-link voltage. b) Phase to neutral voltage. c) Grid current

additional test is conducted, as illustrated in Fig. 5.21. In this test, the CHB-AFE initially operates under balanced loading conditions, similar to the previous case. However, at $t = 1.9$ s, the operating point is intentionally shifted to an unbalanced loading condition, as indicated by the blue marker in Fig. 5.22.

It can be clearly observed that once the operating point moves outside the feasible voltage balancing region, the DC-link voltages can no longer be regulated at their reference values and begin to deviate. This behavior provides strong experimental validation of the analytically derived voltage balancing limits, confirming that stable voltage regulation is ensured only when the system operates within the feasible region.

Additionally, unity power factor operation is preserved within the feasible operating region, where the grid voltage and current remain synchronized. The corresponding multilevel output voltage waveform, presented in both figures 5.20 and figure 5.21, exhibits the expected stepped structure, confirming correct switching operation of the cascaded H-bridge converter.

Overall, these experimental results validate both the effectiveness of the proposed voltage balancing algorithm and the accuracy of the analytically derived feasibility boundaries.

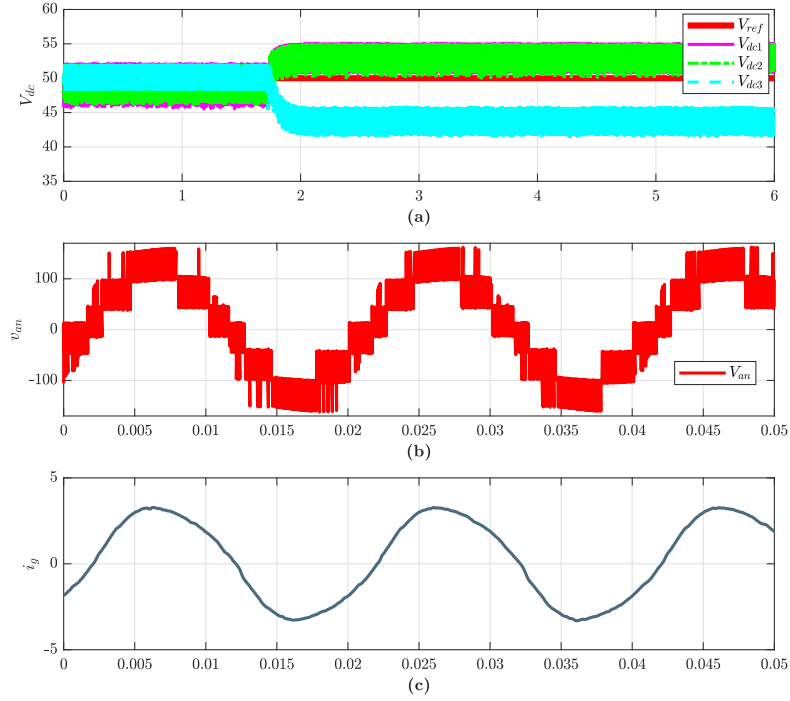


Figure 5.21: CHB-AFE behaviour in outside feasible region. a) DC-link voltage. b) Phase to neutral voltage. c) Grid current

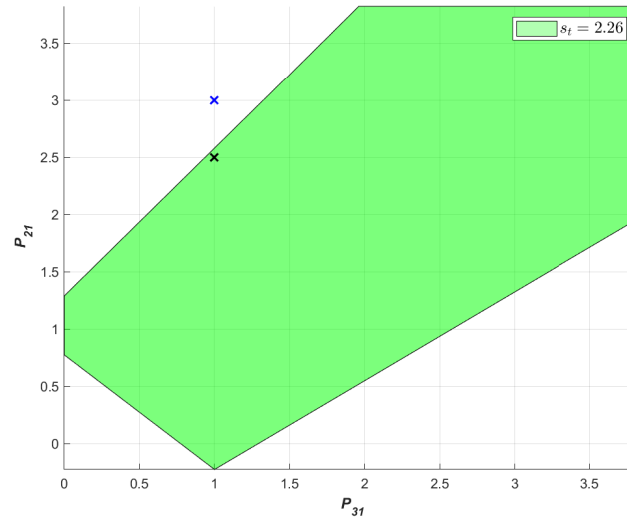


Figure 5.22: DC_Link voltage balancing limits for experimental validation

5.3.4 Experimental Validation Of Optimal Control of BES Module

In the experimental implementation of the proposed control strategy, one important modification is introduced in the experimental implementation of the average DC-link voltage control loop. In practice, the DC-link voltage exhibits relatively slow dynamics compared to the inner current control loop. However, the optimal power references gen-

erated by the QP-based controller are expected to be tracked with fast response. Due to this mismatch in dynamic bandwidth, the DC-link voltage controller alone is not able to immediately reflect rapid changes in the power reference within a single sampling interval.

To address this limitation, a feedforward term is incorporated into the outer DC-link voltage control loop. The purpose of this term is to provide an anticipatory current reference based on the instantaneous power demand, thereby improving the dynamic response of the system. The feedforward current is computed as

$$i_{ff} = 2 \cdot \frac{\sum_{i=1}^N (P_{EV,i} + P_{BES,i})}{v_{dc,avg}} \quad (5.6)$$

where $P_{EV,i}$ and $P_{BES,i}$ represent the power contributions of the EV loads and BES modules, respectively, and $v_{dc,avg}$ is the average DC-link voltage.

By incorporating this feedforward component, the outer voltage loop is effectively assisted in compensating for rapid power variations, while the feedback controller maintains steady-state regulation. This results in improved transient performance and ensures that the current control loop can promptly track the power references provided by the optimization layer.

To experimentally validate the proposed optimal management strategy for the BES modules, the operating principle outlined in section 5.2.1 is implemented on the hardware prototype under low-power conditions. The objective of this test is to assess the effectiveness of the proposed control strategy in real-time operation, taking into account practical limitations such as measurement noise, switching non-idealities, and hardware constraints.

To evaluate the system under dynamic EV charging conditions, a scenario similar to the simulation study is considered. EV arrivals and departures are assumed to be stochastic, with different charging requirements. Specifically, EVs arrive at charging ports 1, 2, and 3 at $t = 1.0$ min, $t = 6.11$ min, and $t = 9.10$ min, respectively, while their departures occur at $t = 12.0$ min, $t = 18.50$ min, and $t = 15.0$ min. It is worth noting that, in the experimental setup, charging port 3 becomes available earlier than port 2, reflecting the variability in charging duration.

Figure 5.23 presents the experimental results of the proposed control strategy under

dynamic EV charging conditions. When the first EV is connected with a power demand of approximately 0.5 kW, the corresponding BES module transitions to discharging mode to supply the required power, while the remaining BES modules operate in charging mode. This behavior is consistent with the simulation results and confirms that the proposed control strategy effectively ensures stable operation of the CHB-AFE rectifier.

As the system evolves, the influence of the state-of-charge (SoC) balancing term in the cost function becomes evident. In particular, when the SoC of individual BES modules approaches certain threshold values (e.g., around 43% and 52% in this experiment), further deviation from the reference is penalized. As a result, the control strategy limits additional charging or discharging actions in order to maintain the SoC close to its reference value. This leads to frequent switching between charging and discharging modes, resulting in chattering in the BES power profiles.

At $t = 6.11$ min, the second EV is connected with a power demand of approximately 0.3 kW. This reduces the overall imbalance in the system compared to the initial condition. Consequently, the power stress on the first BES module decreases, allowing its SoC to recover and gradually settle around 45%. In this operating region, the chattering observed in the BES power profiles is significantly reduced due to the improved balance between load demand and available power.

Subsequently, when the third EV is connected with a charging demand of approximately 210 W, the system approaches a near-symmetrical loading condition. Under this scenario, the grid supplies the majority of the load demand, while the BES modules transition predominantly to charging mode in order to restore and equalize their SoC levels. As a result, the BES modules operate with reduced dynamic stress, and the overall system behavior becomes smoother.

When the first EV departs at $t = 12.0$ min, the corresponding BES module transitions from discharging to charging mode, while the remaining modules continue to operate according to the load demand. This condition persists until the third EV departs at approximately $t = 15.10$ min. At this stage, the system once again experiences a relatively unbalanced loading condition, although with a lower overall power demand. Consequently, the SoC of the BES modules stabilizes around 45%, reflecting the reduced energy exchange required under this operating condition.

Finally, when the last EV departs at $t = 18.50$ min, the load demand is effectively removed, and the BES modules operate to restore their SoC levels toward the reference value. As a result, all modules gradually converge to the desired SoC, demonstrating the ability of the proposed control strategy to achieve SoC equalization under no-load conditions.

It is important to note that even under highly unbalanced loading conditions, the DC-link voltages of all H-bridge modules remain well regulated around their reference values, demonstrating the robustness of the proposed voltage balancing algorithm in the presence of significant power asymmetry. Furthermore, a dwell-time of 5 s is implemented for switching between QP_1 and QP_2 in the experimental setup, which is shorter than the 5 min used in simulation. Despite this difference, the control strategy maintains stable operation and effectively manages the trade-off between SoC balancing and power regulation.

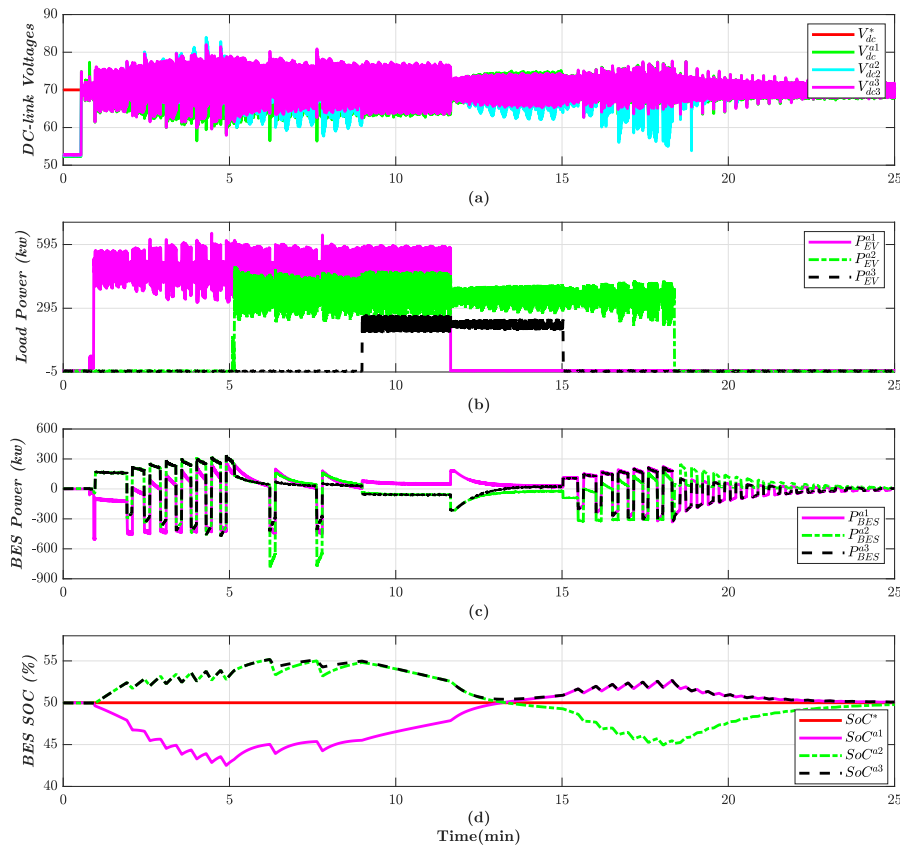


Figure 5.23: Experimental results under dynamic EV charging conditions: (a) DC-link voltages, (b) EV power demand, (c) BES module power, (d) BES state-of-charge (SoC).

To provide a clearer and more detailed insight into the dynamic behavior of the sys-

tem, the experimental results are divided into two time intervals: 1–10 min and 14–25 min and illustrated in 5.24 and 5.25. The intermediate interval between 10 and 14 min is relatively smooth and does not exhibit significant dynamic variations; therefore, it is omitted for clarity. This segmentation allows for a more focused analysis of the transient and highly dynamic regions of operation, where the interaction between BES modules, EV power demand, and SoC regulation is more pronounced. By zooming into these specific intervals, the key dynamic features—such as power oscillations, mode transitions, and SoC convergence can be observed more clearly without being affected by steady-state behavior.

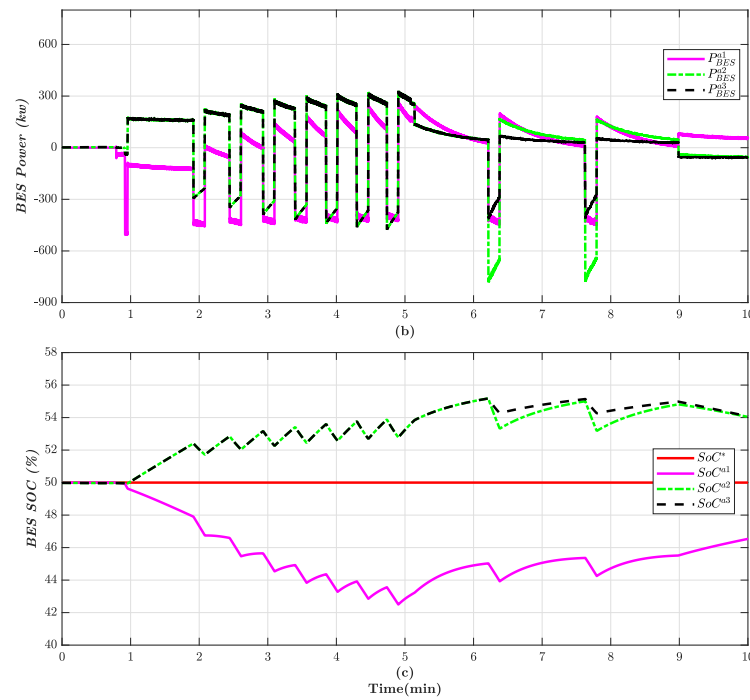


Figure 5.24: Experimental results in the interval 1–10 min: (b) BES module power P_{BES} and (c) BES state-of-charge (SoC).

To provide further insight into the operating behaviour of the CHB-AFE under different loading conditions, the feasible region plots are divided into two cases. The first plot represents the most critical scenario, where the EV charging station operates under highly unbalanced loading conditions. In this case, it can be observed that the system operating points remain within the feasible region at all times. This confirms that the proposed optimization-based control strategy successfully maintains the CHB-AFE within its admissible operating limits, even under severe imbalance. However, due to

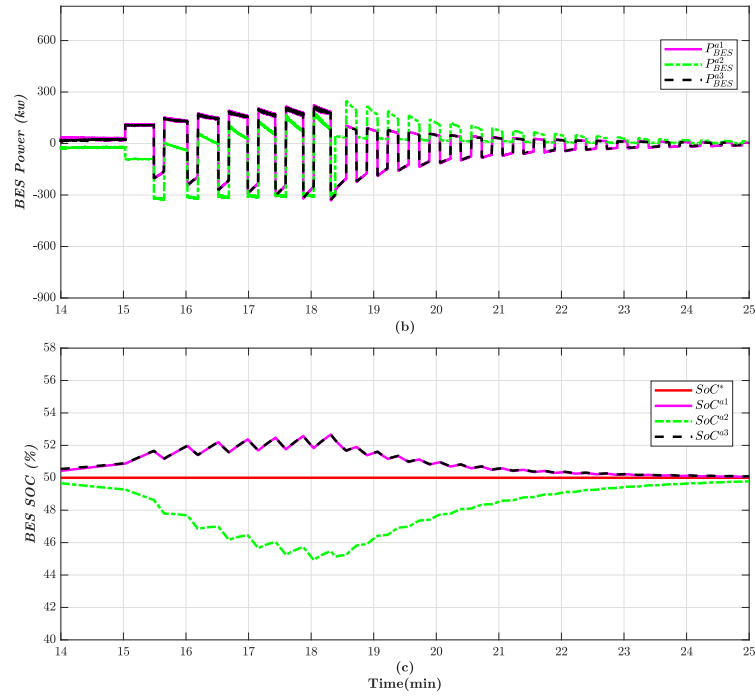
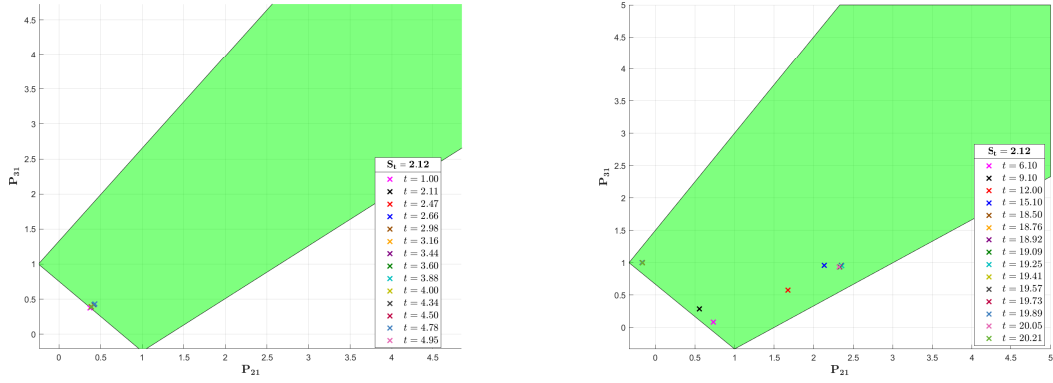


Figure 5.25: Experimental results in the interval 14–25 min: (b) BES module power P_{BES} and (c) BES state-of-charge (SoC).

the strong interaction between the SoC balancing objective and the system constraints, frequent switching between the QP formulations is observed in this region.

The second plot illustrates the system behaviour during EV arrival and departure events, where the loading condition gradually transitions toward a more balanced state and the BES state-of-charge converges toward its reference value. Compared to the first case, the operating points are more dispersed within the feasible region rather than concentrated near its boundary. This is primarily because the BES power values at the selected sampling instants are influenced by transient variations and measurement noise, resulting in slightly higher or lower extracted power values.

It is also worth noting that two separate feasible region plots are presented due to the wider range of power values observed during different operating intervals. This separation improves visualization clarity and allows a more accurate interpretation of system behaviour across both highly dynamic and relatively stable operating conditions.



(a) CHB-AFE operating limits under highly unbalanced loading conditions.

(b) CHB-AFE operating limits during EV arrivals, departures, and SoC convergence.

Figure 5.26: CHB-AFE operating limits in experimental test.

5.4 Summary

This chapter validates the proposed control strategy for BES modules integrated with CHB-AFE for XFC station application through MATLAB/Simulink simulations and experimental investigations. In simulation, the results confirm effective DC-link voltage balancing, adherence to the derived operating limits, and proper power distribution under dynamic EV charging scenarios. The optimal BES management strategy successfully maintains system operation within the feasible region while regulating SoC and reducing grid stress.

The experimental results further verify these findings under practical conditions, including measurement noise and hardware non-linearities. The CHB-AFE maintains stable DC-link voltages, unity power factor operation, and reliable performance during both balanced and unbalanced loading conditions. Overall, strong agreement between simulation and experimental results demonstrates the robustness and practical feasibility of the proposed control approach.

References 5

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Chapter 6:

Conclusion And Future Work

Conclusion

This dissertation investigates the modelling, control, and optimal power management of battery energy storage (BES) integrated with cascaded H-bridge (CHB)-based medium-voltage (MV) extreme fast-charging (XFC) stations, with the primary objective of improving battery utilization while reducing stress on both the grid and the distributed energy storage system. Although the CHB-based architecture offers inherent modularity, scalability, and direct medium-voltage interfacing, conventional control strategies generally employ predetermined or equal-power allocation among converter cells, which can lead to unbalanced battery utilization, unnecessary charge-discharge cycles, and accelerated battery degradation.

To overcome these limitations, an optimization-based BES power management strategy was developed by explicitly incorporating the CHB converter's intrinsic operating limits into the control framework. Analytical DC-link voltage-balancing constraints were derived and reformulated into practical power constraints in a quadratic programming (QP)-based optimization problem.

The proposed control strategy was validated through both simulation and experimental investigations under dynamic EV charging conditions and benchmarked against an existing control methodology. The results demonstrate that the proposed strategy maintains all operating points within the feasible operating region, preserves DC-link voltage balance, achieves effective SoC equalization, and provides more balanced utilization of the BES modules. Compared with the benchmark control strategy, the proposed method reduces unnecessary battery cycling, mitigates excessive discharge of individual BES modules, and improves overall battery utilization without compromising the dynamic performance or operational stability of the CHB-AFE rectifier.

Future Development

A natural extension of this research is the application of the proposed framework to larger CHB systems with an increased number of cells, the incorporation of battery-degradation-aware models, and real-time implementation on embedded platforms. Further work may also investigate integrating renewable energy sources in place of or alongside the energy storage system. In addition, the development of cost-effective strategies for state-of-charge (SoC) balancing of BES modules represents an important direction for improving system efficiency and scalability. These developments would facilitate the transition from laboratory-scale validation to a scalable, practically deployable XFC station controller.