

# **Electro-Thermal Modeling and Surge Reliability of High-Power Semiconductor Devices with Machine Learning Based Parameter Prediction**



**Università  
di Genova**

**Fawad Ahmad**

Supervisor: Luis Ramon Vaccaro

Department of Electrical, Electronic, Telecommunications Engineering and  
Naval Architecture (DITEN)  
University of Genoa

This dissertation is submitted for the degree of  
*Doctor of Philosophy*

July 2026

I would like to dedicate this thesis to everyone who supported me throughout this journey . . .

# Acknowledgement

First and foremost, I would like to thank Allah Almighty for granting me the opportunity, strength, and perseverance to pursue and successfully complete my doctoral studies. His guidance remained a constant source of motivation throughout this journey.

I would like to express my sincere gratitude to my supervisor, Prof. Dr. Luis Ramon Vaccaro, for his vision, guidance, continuous support, and encouragement throughout the course of this research. His strong theoretical background, extensive research experience, and innovative thinking significantly enhanced the scientific value of this work. Working under his supervision has been a great privilege for me and will remain one of the most memorable experiences of my academic life.

I gratefully acknowledge Poseico Power Electronics S.p.A. for the valuable collaboration with the University of Genoa and for providing access to essential experimental platforms and industrial expertise. I would like to particularly thank my industrial supervisor, Marco Portesine, and my colleague Federico Portesine for their continuous technical support during the experimental and testing phases of this research. I am especially thankful to Marco Portesine for his availability, guidance, and support during a challenging period of professional and personal adjustment. He generously shared his extensive industrial experience, linked practical insights directly to my research work, and continuously exchanged ideas with me, which significantly improved the quality and impact of this research. His critical perspective, not only in research but also in broader aspects of problem solving, has greatly shaped my ability to think analytically and approach challenges with greater depth and maturity.

A special acknowledgment is extended to the Italian Ministry of Education, University, and Research for the financial support provided through the University of Genoa under the Programma Regionale Fondo Sociale Europeo Plus (FSE+) 2021–2027, Priorità 2—Istruzione e Formazione—ESO 4.6 (OS-f), Operazione “Scienze e tecnologie per l’ingegneria elettrica e i sistemi complessi per la mobilità”. This support made it possible to pursue and successfully complete this enriching doctoral program. Furthermore, the opportunity to study and conduct research at a prestigious institution in Italy significantly broadened my academic perspective and will undoubtedly contribute to my future professional career.

I would like to express my sincere gratitude to all my teachers, especially Prof. Mario Marchesoni of the Department of Electrical Engineering, University of Genoa (UniGe), Genoa, Italy, for their invaluable contributions to building my theoretical foundation and conceptual understanding. I am also grateful to all the staff at Poseico Power Electronics S.p.A., particularly Emilio Sacchi, for their support and technical insights, which significantly enriched my research experience.

I would like to thank my colleagues in the PETRA research group for fostering a collaborative, supportive, and intellectually stimulating research environment. Their cooperation and camaraderie made the research process both productive and enjoyable.

Finally, I would like to express my deepest gratitude to my parents, brothers, and sisters for their unwavering encouragement, motivation, prayers, and continuous support throughout my Ph.D. studies. I am forever indebted to my parents, whose sacrifices and unconditional support were fundamental to the successful completion of this degree.



# Abstract

High-power semiconductor devices are considered key components of modern power electronic systems operating in high-voltage and high-current applications such as high-voltage direct current transmission, railway traction, industrial power conversion, and electric vehicle fast-charging infrastructure. As power density continues to increase, the reliable operation of these devices is increasingly constrained by thermal stress and transient overload conditions, particularly during surge current events. Therefore, it is a critical challenge to accurately estimate junction temperature and assess the reliability of device robustness. The rapid increase in junction temperature influences the reliability of the device, both at the device design and system levels, leading to performance degradation and device failure.

This thesis proposes electro-thermal and data-driven modeling methodologies to address these challenges, with a primary focus on diodes and thyristors. First, the transient thermal impedance of high-power press-pack diodes is characterized by the development of an electro-thermal modeling framework. Thermal resistance and capacitance parameters are analytically derived from device geometry and material properties, enabling the construction of Cauer thermal networks that are subsequently transformed into equivalent Foster thermal models. Moreover, curve-fitting techniques are performed in MATLAB<sup>®</sup> to extract thermal parameters from transient thermal impedance responses. The proposed models are validated through experimental measurements.

Building upon this foundation, a model is proposed to estimate the forward voltage drop for high-power diodes under high surge current levels. Moreover, simulations were also performed to estimate the junction temperature. By integrating rated electrical parameters with thermal simulation data, the proposed methodology captures dynamic slope resistance and transient voltage behavior to counter the limitations of conventional static current–voltage-based temperature estimation methods. Moreover, the results of the proposed model are compared with experimental results.

In addition, a comparative study of two different packaging assemblies is conducted to investigate and analyze the thermal performance and surge capability. An insulated module diode and a press-pack diode with pressure contact technology (PCT), both with

identical specifications and power ratings, are utilized to evaluate the influence of packaging assembly on device performance. For this purpose, a dedicated experimental setup is developed, generating a 10 ms half sine wave, and a series of tests of the forward voltage drop across varying surge levels were conducted. Moreover, electro-thermal simulations are also performed to analyze and compare junction temperature and analyze failure behavior.

In addition to physics-based modeling, this thesis introduces machine learning (ML) frameworks for classifying and predicting key design and performance parameters, including chip diameter and average current of high-power semiconductor devices. A comprehensive survey of high-power thyristors is conducted, analyzing the influence of chip diameter and thickness on both electrical and thermal performance. Moreover, a dedicated dataset is developed by extracting electrical parameters from the leading semiconductor manufacturer's datasheet of multiple models. Moreover, multiple ML models, including gaussian process regression (GPR), support vector machine (SVM), artificial neural network (ANN), and ensemble methods, are also implemented. Furthermore, data augmentation, shapley additive explanation (SHAP) and feature optimization are also performed.

Overall, this research establishes a unified framework, combining electro-thermal modeling, simulation, experimental validation, and data-driven techniques to improve the reliability assessment and design of high-power semiconductor devices. The proposed methodologies provide practical tools for manufacturers and system designers, contributing to the development of robust and reliable devices and systems.

**Keywords:** *Press Pack Diodes; Cauer Model to Foster Model Transformation; Thermal Networks; Cauer Model; Foster Model; Surge Current Analysis; Semiconductor Devices; Thermal Characterization; Junction Temperature Prediction; Electro-thermal Simulation; Forward-voltage Modeling; Surge Current Capability; Failure Behavior; Electro-thermal Modelling; Pressure Contact Technology; High-power Semiconductor Devices; Machine Learning in Semiconductors; Chip Diameter Prediction; High-power Semiconductors; Electrical Parameters Analysis; Data-driven Semiconductor Design; Average Current Prediction; Classification in Semiconductor Devices, Electrical Characterization, Machine Learning in Semiconductors*

# Sommario

I dispositivi a semiconduttore di alta potenza sono considerati componenti chiave dei moderni sistemi di elettronica di potenza operanti in applicazioni ad alta tensione e alta corrente, quali la trasmissione in corrente continua ad alta tensione (HVDC), la trazione ferroviaria, la conversione di potenza industriale e le infrastrutture di ricarica rapida per veicoli elettrici. Con il continuo aumento della densità di potenza, il funzionamento affidabile di tali dispositivi è sempre più limitato da sollecitazioni termiche e condizioni di sovraccarico transitorio, in particolare durante eventi di corrente di spunto. Pertanto, la stima accurata della temperatura di giunzione e la valutazione dell'affidabilità e della robustezza del dispositivo rappresentano una sfida cruciale. Il rapido incremento della temperatura di giunzione influisce in modo significativo sull'affidabilità del dispositivo, sia a livello di progettazione del componente sia a livello di sistema, portando a un degrado delle prestazioni e, in casi estremi, al guasto del dispositivo.

Questa tesi propone metodologie di modellazione elettro-termica basate sui dati per affrontare tali criticità, con particolare attenzione a diodi e tiristori. In primo luogo, l'impedenza termica transitoria di diodi press-pack di alta potenza viene caratterizzata attraverso lo sviluppo di un framework di modellazione elettro-termica. I parametri di resistenza e capacità termica vengono derivati analiticamente a partire dalla geometria del dispositivo e dalle proprietà dei materiali, consentendo la costruzione di reti termiche di tipo Cauer successivamente trasformate in modelli termici equivalenti di tipo Foster. Inoltre, vengono applicate tecniche di curve fitting in ambiente MATLAB® per l'estrazione dei parametri termici a partire dalle risposte di impedenza termica transitoria. I modelli proposti sono validati mediante misure sperimentali.

Sulla base di questo approccio, viene proposto un modello per la stima della caduta di tensione diretta in diodi di alta potenza sottoposti a elevati livelli di corrente di spunto. Sono inoltre eseguite simulazioni per la stima della temperatura di giunzione. Integrando i parametri elettrici nominali con i dati provenienti dalle simulazioni termiche, la metodologia proposta consente di descrivere la resistenza dinamica di pendenza e il comportamento transitorio della tensione, superando i limiti dei metodi convenzionali di stima della temperatura

basati su caratteristiche corrente–tensione statiche. I risultati del modello proposto vengono infine confrontati con dati sperimentali.

Viene inoltre condotto uno studio comparativo di due diverse soluzioni di packaging al fine di analizzarne le prestazioni termiche e la capacità di sopportare correnti di spunto. A tal fine, vengono utilizzati un diodo in modulo isolato e un diodo press-pack con tecnologia a contatto di pressione (Pressure Contact Technology, PCT), aventi specifiche e potenze nominali identiche, per valutare l’influenza dell’assemblaggio del package sulle prestazioni del dispositivo. A questo scopo è stato sviluppato un banco di prova dedicato in grado di generare una semionda sinusoidale di 10 ms, e sono state condotte prove della caduta di tensione diretta a diversi livelli di corrente di spunto. Sono inoltre eseguite simulazioni elettro-termiche per stimare e confrontare la temperatura di giunzione e analizzare i meccanismi di guasto.

Oltre alla modellazione basata sulla fisica, la tesi introduce un framework di machine learning per la classificazione e la previsione di parametri chiave di progetto e prestazioni, quali il diametro del chip e la corrente media nei dispositivi a semiconduttore di alta potenza. Viene condotta un’analisi approfondita dei tiristori di alta potenza, valutando l’influenza del diametro e dello spessore del chip sulle prestazioni elettriche e termiche. Inoltre, viene sviluppato un dataset dedicato mediante l’estrazione di parametri elettrici dai datasheet di diversi modelli forniti dai principali produttori di semiconduttori. Sono quindi implementati diversi modelli di machine learning, tra cui la regressione con processi gaussiani, le macchine a vettori di supporto, le reti neurali artificiali e metodi ensemble. Vengono inoltre applicate tecniche di data augmentation, analisi shapley additive explanations (SHAP) e ottimizzazione delle feature.

Nel complesso, questa ricerca definisce un framework unificato che combina modellazione elettro-termica, simulazione, validazione sperimentale e tecniche data-driven al fine di migliorare la valutazione dell’affidabilità e la progettazione di dispositivi a semiconduttore di alta potenza. Le metodologie proposte forniscono strumenti pratici per produttori e progettisti di sistemi, contribuendo allo sviluppo di dispositivi e sistemi più robusti e affidabili.

# Table of contents

|                                                                                    |          |
|------------------------------------------------------------------------------------|----------|
| Acknowledgement                                                                    | iii      |
| Abstract                                                                           | v        |
| Sommario                                                                           | vii      |
| List of Figures                                                                    | xiv      |
| List of Tables                                                                     | xix      |
| List of Publications                                                               | xxi      |
| List of Symbols                                                                    | xxiv     |
| List of Abbreviations                                                              | xxvii    |
| <b>1 Introduction</b>                                                              | <b>2</b> |
| 1.1 Overview and Research Motivation                                               | 2        |
| 1.1.1 Role of High Power Devices in Power Electronics                              | 3        |
| 1.1.2 Reliability of High Power Devices                                            | 4        |
| 1.1.3 Need for Electro-Thermal Modeling                                            | 5        |
| 1.1.4 Role of Electrothermal Modeling in Device Analysis                           | 6        |
| 1.1.5 Failure Mechanisms and Reliability Challenges in Power Semiconductor Devices | 7        |
| 1.2 Machine Learning in Power Electronics                                          | 9        |
| 1.3 Challenges in Device modeling and Analysis                                     | 10       |
| 1.4 Research Objectives                                                            | 11       |
| 1.5 Organization of the Thesis                                                     | 12       |

|          |                                                                             |           |
|----------|-----------------------------------------------------------------------------|-----------|
| <b>2</b> | <b>Fundamentals and Literature Review</b>                                   | <b>16</b> |
| 2.1      | Overview                                                                    | 16        |
| 2.2      | Market Analysis of Power Devices                                            | 18        |
| 2.3      | Introduction to Semiconductors                                              | 22        |
| 2.3.1    | Semiconductors and Doping                                                   | 22        |
| 2.3.2    | Operating Principles of High-Power Diodes                                   | 23        |
| 2.3.3    | Ideal and Practical Diode Characteristics                                   | 24        |
| 2.4      | Packaging Technologies and Device Configurations                            | 24        |
| 2.5      | Thermal Modeling and Junction Temperature Estimation Techniques             | 26        |
| 2.5.1    | Measurements-based Studies                                                  | 27        |
| 2.5.1.1  | Direct Measurements                                                         | 28        |
| 2.5.1.2  | Indirect Measurement Methods                                                | 30        |
| 2.5.1.3  | Limitations of Measurement-Based Approaches                                 | 33        |
| 2.5.2    | Simulation-based Studies                                                    | 33        |
| 2.5.2.1  | RC Thermal Networks                                                         | 33        |
| 2.5.2.2  | Electro-Thermal Coupled Models                                              | 37        |
| 2.5.2.3  | Numerical Methods                                                           | 39        |
| 2.6      | Machine Learning Applications in Power Electronics                          | 41        |
| 2.7      | Gap Analysis                                                                | 42        |
| 2.8      | Problem Formulation                                                         | 43        |
| 2.9      | Scientific Contributions                                                    | 44        |
| <b>3</b> | <b>Transient Thermal Impedance Modeling of High-Power Press-Pack Diodes</b> | <b>47</b> |
| 3.1      | Overview and Research Motivation                                            | 47        |
| 3.2      | Physical Structure and Material Characterization of Press-Pack Diodes       | 49        |
| 3.3      | Analytical Calculation of Thermal Resistance and Capacitance                | 50        |
| 3.4      | Electro-Thermal Modeling Framework                                          | 50        |
| 3.4.1    | Development of the Cauer Thermal Network                                    | 50        |
| 3.4.2    | Thermal Parameter Extraction for the Foster Thermal Network                 | 52        |
| 3.4.3    | Transformation and Interpretation Using Foster Thermal Networks             | 53        |
| 3.5      | Experimental Setup                                                          | 54        |
| 3.5.1    | Experimental Validation and Discussion                                      | 59        |
| 3.6      | Limitations                                                                 | 59        |
| 3.7      | Conclusion                                                                  | 60        |

|          |                                                                                                                   |            |
|----------|-------------------------------------------------------------------------------------------------------------------|------------|
| <b>4</b> | <b>Surge Current Electro-Thermal Modeling and Junction Temperature Estimation</b>                                 | <b>62</b>  |
| 4.1      | Overview and Research Motivation . . . . .                                                                        | 62         |
| 4.2      | Surge Wave Generator . . . . .                                                                                    | 64         |
| 4.3      | Proposed Model . . . . .                                                                                          | 64         |
| 4.4      | Experimental Setup, Validation and Analysis . . . . .                                                             | 68         |
| 4.4.1    | Experimental Setup . . . . .                                                                                      | 68         |
| 4.5      | Results and Validation . . . . .                                                                                  | 70         |
| 4.6      | Analysis . . . . .                                                                                                | 71         |
| 4.7      | Modeling and Simulations . . . . .                                                                                | 73         |
| 4.7.1    | Resistance Capacitance Equivalent Method . . . . .                                                                | 73         |
| 4.7.2    | Finite Element Method . . . . .                                                                                   | 73         |
| 4.8      | Simulation Results and Discussion . . . . .                                                                       | 75         |
| 4.9      | Limitations . . . . .                                                                                             | 80         |
| 4.10     | Conclusion . . . . .                                                                                              | 80         |
| <b>5</b> | <b>Comparative Analysis of Surge Reliability and Failure Mechanisms in Press-Pack and Insulated Module Diodes</b> | <b>83</b>  |
| 5.1      | Overview and Research Motivation . . . . .                                                                        | 83         |
| 5.2      | Press-Pack and Insulated Module Diodes . . . . .                                                                  | 86         |
| 5.3      | Experimental Test . . . . .                                                                                       | 87         |
| 5.4      | Experimental Results . . . . .                                                                                    | 88         |
| 5.5      | Numerical Acquisition and Processing . . . . .                                                                    | 89         |
| 5.6      | Simulation Setup . . . . .                                                                                        | 91         |
| 5.7      | Simulation Results and Junction Temperature Comparison . . . . .                                                  | 91         |
| 5.8      | Failure Mechanisms and Reliability Assessment . . . . .                                                           | 93         |
| 5.9      | Limitations . . . . .                                                                                             | 97         |
| 5.10     | Conclusion . . . . .                                                                                              | 98         |
| <b>6</b> | <b>Machine Learning-Based Classification and Prediction of Chip Diameter in High-Power Devices</b>                | <b>100</b> |
| 6.1      | Overview and Research Motivation . . . . .                                                                        | 100        |
| 6.2      | Influence of Chip Diameter and Thickness on Electrical and Thermal Performance . . . . .                          | 103        |
| 6.2.1    | Effect of Change in Material Thickness on Device Performance . . . . .                                            | 103        |
| 6.2.2    | Impact of Change in Material Diameter on Device Performance . . . . .                                             | 104        |
| 6.2.3    | Performance Evaluation of Geometric Variations . . . . .                                                          | 106        |
| 6.3      | Methodology . . . . .                                                                                             | 107        |

|          |                                                                                     |            |
|----------|-------------------------------------------------------------------------------------|------------|
| 6.3.1    | Data Acquisition . . . . .                                                          | 107        |
| 6.3.2    | Data Augmentation . . . . .                                                         | 108        |
| 6.3.3    | Feature Optimization . . . . .                                                      | 110        |
| 6.4      | Implementation of Machine Learning Models . . . . .                                 | 110        |
| 6.4.1    | Support Vector Machine . . . . .                                                    | 111        |
| 6.4.2    | Artificial Neural Network . . . . .                                                 | 112        |
| 6.4.3    | Ensemble Methods . . . . .                                                          | 113        |
| 6.5      | Results and Discussion . . . . .                                                    | 113        |
| 6.5.1    | Comparison of Classification Accuracies . . . . .                                   | 113        |
| 6.5.2    | Confusion Matrix Analysis . . . . .                                                 | 114        |
| 6.5.2.1  | Confusion Matrix of Optimized Features . . . . .                                    | 116        |
| 6.5.3    | Prediction of Chip Diameter . . . . .                                               | 119        |
| 6.6      | Limitations . . . . .                                                               | 121        |
| 6.7      | Conclusion . . . . .                                                                | 121        |
| <b>7</b> | <b>Machine Learning Framework for Average Current Classification and Prediction</b> | <b>124</b> |
| 7.1      | Overview and Research Motivation . . . . .                                          | 124        |
| 7.2      | Methodology . . . . .                                                               | 127        |
| 7.2.1    | Dataset . . . . .                                                                   | 128        |
| 7.3      | Feature Extraction and Selection . . . . .                                          | 129        |
| 7.4      | Implementation of Machine Learning Models . . . . .                                 | 129        |
| 7.4.1    | Artificial Neural Network . . . . .                                                 | 130        |
| 7.4.2    | Ensemble Methods . . . . .                                                          | 131        |
| 7.4.3    | Support Vector Machine . . . . .                                                    | 132        |
| 7.4.4    | Gaussian Process Regression . . . . .                                               | 133        |
| 7.5      | Results and Discussion . . . . .                                                    | 133        |
| 7.5.1    | SHAP-Based Feature Importance and Interpretability . . . . .                        | 133        |
| 7.5.2    | Classification Performance Evaluation . . . . .                                     | 134        |
| 7.5.2.1  | Confusion Matrix and Metrics . . . . .                                              | 135        |
| 7.5.3    | Average Current Prediction Results . . . . .                                        | 138        |
| 7.5.3.1  | Performance of the Artificial Neural Network . . . . .                              | 138        |
| 7.5.3.2  | Performance of the Optimized Ensemble Model . . . . .                               | 140        |
| 7.5.3.3  | Gaussian Process Regression . . . . .                                               | 142        |
| 7.6      | Conclusion . . . . .                                                                | 145        |



|          |                                                                  |            |
|----------|------------------------------------------------------------------|------------|
| <b>8</b> | <b>Conclusions and Future Research Directions</b>                | <b>147</b> |
| 8.1      | Overview . . . . .                                               | 147        |
| 8.2      | Summary of Findings and Main Contributions . . . . .             | 147        |
| 8.2.1    | Electro-Thermal Modeling of High-Power Devices . . . . .         | 147        |
| 8.2.2    | Surge Current Analysis . . . . .                                 | 148        |
| 8.2.3    | Packaging Technology Comparison . . . . .                        | 148        |
| 8.2.4    | Data-Driven Design Using Machine Learning . . . . .              | 148        |
| 8.3      | Possible Improvements and Future Direction . . . . .             | 149        |
| 8.3.1    | Extension to Wide-Bandgap and Multi-Chip Architectures . . . . . | 149        |
| 8.3.2    | Statistical Surge Reliability Assessment . . . . .               | 149        |
| 8.3.3    | Interface Effects and Aging Considerations . . . . .             | 149        |
| 8.3.4    | Extensions of Machine Learning Frameworks . . . . .              | 150        |
| 8.4      | Final Remarks . . . . .                                          | 150        |
|          | <b>References</b>                                                | <b>151</b> |

# List of Figures

|      |                                                                                                                            |    |
|------|----------------------------------------------------------------------------------------------------------------------------|----|
| 1.1  | Some notable factors impacting device reliability and leading to device degradation and failure. . . . .                   | 5  |
| 2.1  | Number of scientific publications on thermal modeling of electronic devices (source: Web of Science). . . . .              | 17 |
| 2.2  | Global market share 2023: Power semiconductors. . . . .                                                                    | 18 |
| 2.3  | Estimated market share of high power devices by application (2025). . . .                                                  | 19 |
| 2.4  | Impact of diameter on electrical characteristics average current and $V_{RRM}$ . .                                         | 20 |
| 2.5  | Formation of depletion region. . . . .                                                                                     | 23 |
| 2.6  | V-I characteristics of ideal and practical diode. . . . .                                                                  | 24 |
| 2.7  | Structure and heat-transfer mechanism of a conventional brazed and welded contact module. . . . .                          | 25 |
| 2.8  | Schematic of the structure and heat-transfer mechanisms of the PCT-insulated module. . . . .                               | 26 |
| 2.9  | Schematic illustration of the structure and heat-transfer mechanisms in the PCT press pack diode. . . . .                  | 26 |
| 2.10 | Some notable techniques for temperature evaluation of high-power semiconductor devices. . . . .                            | 27 |
| 2.11 | Cauer type thermal network corresponding to the device structure. . . . .                                                  | 34 |
| 2.12 | Equivalent circuit schematic of a Foster thermal network. . . . .                                                          | 35 |
| 3.1  | Structural schematic of high power press pack diode. . . . .                                                               | 49 |
| 3.2  | Equivalent Cauer thermal network of the high-power press-pack diode structure in PSIM as described in Section 3.2. . . . . | 51 |
| 3.3  | Thermal impedance versus time curve obtained through cauer thermal model.                                                  | 53 |
| 3.4  | Curve fitting in MATLAB®. . . . .                                                                                          | 54 |
| 3.5  | Foster network circuit diagram. . . . .                                                                                    | 55 |
| 3.6  | Thermal impedance versus time curve obtained through foster thermal model.                                                 | 55 |

|      |                                                                                                                                                                                                                                                                                                    |    |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 3.7  | Experimental setup for thermal resistance measurement. . . . .                                                                                                                                                                                                                                     | 56 |
| 3.8  | Test equipment scheme. . . . .                                                                                                                                                                                                                                                                     | 58 |
| 3.9  | Comparison of the cauer, foster and analytical model. . . . .                                                                                                                                                                                                                                      | 59 |
| 4.1  | Schematic representation of the surge wave generator setup. . . . .                                                                                                                                                                                                                                | 65 |
| 4.2  | System model of the proposed forward voltage prediction model. . . . .                                                                                                                                                                                                                             | 66 |
| 4.3  | Simulated results under varying peak surge current conditions: (a) instantaneous power dissipation profiles; (b) corresponding transient temperature responses. . . . .                                                                                                                            | 67 |
| 4.4  | Schematic representation of the experimental surge current test setup, including the surge generator and the DUT. . . . .                                                                                                                                                                          | 68 |
| 4.5  | Experimental equipment setup used for pre- and post-surge electrical characterization:<br>(a) forward conduction test setup. (b) $V_{RRM}$ and $I_{RRM}$ test setup. . . . .                                                                                                                       | 69 |
| 4.6  | Experimental setup used for measuring the forward voltage of the DUT across various surge current levels. . . . .                                                                                                                                                                                  | 70 |
| 4.7  | Surge current conditions and corresponding forward voltages: (a) 6400 A, $V_F = 3.6$ V<br>(b) 10,800 A, $V_F = 5.4$ V (c) 14,400 A, $V_F = 6.2$ V (d) 20,400 A, $V_F = 7.8$ V. In each subplot, the yellow trace denotes the surge current and the teal trace denotes the forward voltage. . . . . | 71 |
| 4.8  | Comparison of static, experimental, and proposed models for diode forward voltage characteristics. . . . .                                                                                                                                                                                         | 72 |
| 4.9  | Geometry of the diode and corresponding finite element mesh developed in ANSYS for evaluating electro-thermal behavior under high-surge-current conditions. . . . .                                                                                                                                | 74 |
| 4.10 | Thermal characterization of the DUT: (a) thermal impedance versus time curve; (b) voltage, current, and peak temperature dynamics under the surge current. . . . .                                                                                                                                 | 75 |
| 4.11 | Average temperature of the DUT obtained from simulation across multiple surge currents. . . . .                                                                                                                                                                                                    | 76 |
| 4.12 | (a) Impact of temperature on forward voltage under fixed surge current. (b) Characteristics of time evolution of voltage ( $V_F(t)$ ), current ( $I(t)$ ), and maximum junction temperature $T_{j_{max}}(t)$ . . . . .                                                                             | 77 |
| 4.13 | (a) Minimum, average, and maximum temperatures estimated by the proposed model for a surge current. (b) Average temperature comparison: proposed model vs. experimental data and static I–V model. . . . .                                                                                         | 77 |

|      |                                                                                                                                                                                                     |     |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 4.14 | Temperature distribution in the silicon chip under the surge current at different time instances: (a) 1 ms, (b) 4 ms, (c) 7 ms, and (d) 9 ms. . . . .                                               | 78  |
| 4.15 | Temperature distribution across the entire device under the surge current. . .                                                                                                                      | 79  |
| 4.16 | Heat distribution in the silicon chip under the surge current at different time instants: (a) 1 ms, (b) 4 ms, (c) 7 ms, and (d) 9 ms. . . . .                                                       | 79  |
| 4.17 | Comparison between the junction temperature estimated using the RC equivalent circuit in PSIM and the FEM-based simulation in ANSYS. . . . .                                                        | 80  |
| 5.1  | Device structure (a) PCT insulated module diode (b) PCT press pack diode. . .                                                                                                                       | 86  |
| 5.2  | Surge current waveforms for the performed experimental surge tests. . . . .                                                                                                                         | 87  |
| 5.3  | Measured voltages for PCT press pack diode. . . . .                                                                                                                                                 | 88  |
| 5.4  | Measured voltages for diode module for corresponding surge currents. . . . .                                                                                                                        | 89  |
| 5.5  | Current and voltage waveforms recorded during the experiment using an oscilloscope. The yellow traces represent the surge current, while the teal traces correspond to the forward voltage. . . . . | 90  |
| 5.6  | Parameter waveforms during surge operation: (a) Measured current and voltage waveforms, (b) Acquired time-dependent power based on corresponding electrical parameters. . . . .                     | 91  |
| 5.7  | Temperature under different surge peak (a) Press pack diode (b) Diode module. . .                                                                                                                   | 92  |
| 5.8  | (a) Surge trajectory, I-V curve (b) V-T, I-T and $T_{max}$ . . . . .                                                                                                                                | 93  |
| 5.9  | Surge trajectory and I-V curve, V-T, I-T and $T_{max}$ (a) Press pack PCT (b) PCT module. . . . .                                                                                                   | 94  |
| 5.10 | Impact of evaporation of metal on silicon chip (a) Press pack diode (b) Module diode. . . . .                                                                                                       | 94  |
| 5.11 | Impact of surge on molybdenum (a) Press pack diode (b) Module diode. . . . .                                                                                                                        | 95  |
| 5.12 | Failure of silicon chip (a) Press pack diode (b) Module diode. . . . .                                                                                                                              | 96  |
| 5.13 | Optical microscope images showing failure of silicon chip after surge test (a) With no crack at sides. (b) With crack at center. . . . .                                                            | 96  |
| 5.14 | Comparison of thermal impedance between PCT press pack diode and PCT module diode. . . . .                                                                                                          | 97  |
| 6.1  | Impact of change in thickness on thermal resistance in different materials (a) Copper. (b) Molybdenum. (c) Silicon. (d) Silicon at 5 ms. . . . .                                                    | 104 |
| 6.2  | Behavior of device performance due to change in thickness at 5 ms. . . . .                                                                                                                          | 105 |
| 6.3  | Impact of change in diameter on device thermal impedance. . . . .                                                                                                                                   | 105 |
| 6.4  | Impact of change in material geometry on device average current in copper. . .                                                                                                                      | 106 |
| 6.5  | Validation of original data and augmented data. . . . .                                                                                                                                             | 109 |

|      |                                                                                                             |     |
|------|-------------------------------------------------------------------------------------------------------------|-----|
| 6.6  | Contribution of feature on output for diameter classification. . . . .                                      | 110 |
| 6.7  | Methodology for diameter classification and prediction. . . . .                                             | 111 |
| 6.8  | Confusion matrix of test accuracy for classification of diameter by ANN. . . . .                            | 115 |
| 6.9  | Confusion matrix of test accuracy for the diameter classification for SVM. . . . .                          | 116 |
| 6.10 | Confusion matrix of test accuracy for ensemble. . . . .                                                     | 117 |
| 6.11 | Confusion matrix of test accuracy for the diameter classification with feature optimized ANN. . . . .       | 118 |
| 6.12 | Confusion matrix of test accuracy for the diameter classification with optimized features ensemble. . . . . | 118 |
| 6.13 | Confusion matrix of test accuracy for the diameter classification with optimized features SVM. . . . .      | 119 |
| 6.14 | Prediction accuracy of chip diameter using the ensemble model. . . . .                                      | 120 |
| 6.15 | Prediction accuracy of chip diameter using the Support Vector Machine (SVM) model. . . . .                  | 120 |
| 6.16 | Prediction accuracy of chip diameter using the Artificial Neural Network (ANN) model. . . . .               | 121 |
| 7.1  | Various techniques to estimate average current. . . . .                                                     | 126 |
| 7.2  | Methodology for classification and prediction of average current. . . . .                                   | 128 |
| 7.3  | MRMR-based feature ranking showing relevance scores of input features. . . . .                              | 130 |
| 7.4  | Contribution of feature on output for average current prediction. . . . .                                   | 134 |
| 7.5  | Impact of input features on average current for each class. . . . .                                         | 135 |
| 7.6  | Confusion matrix of average current classification on the test dataset using the ensemble model. . . . .    | 137 |
| 7.7  | Confusion matrix of average current classification on the test dataset using the SVM model. . . . .         | 137 |
| 7.8  | Confusion matrix of average current classification on the test dataset using the ANN model. . . . .         | 138 |
| 7.9  | Response plot of ANN (a) Full featured (b) Reduced featured. . . . .                                        | 139 |
| 7.10 | Actual vs predicted of ANN (a) Full featured (b) Reduced featured. . . . .                                  | 139 |
| 7.11 | Residual ANN (a) Full featured (b) Reduced featured. . . . .                                                | 140 |
| 7.12 | Response plot of ensembles (a) Full featured (b) Reduced featured. . . . .                                  | 141 |
| 7.13 | Residual of ensemble (a) Full featured (b) Reduced featured. . . . .                                        | 141 |
| 7.14 | Actual vs predicted of ensemble (a) Full featured (b) reduced featured. . . . .                             | 142 |
| 7.15 | Response plot of GPR (a) Full featured (b) Reduced featured. . . . .                                        | 143 |
| 7.16 | Actual vs predicted of GPR (a) Full featured (b) reduced featured. . . . .                                  | 144 |
| 7.17 | Residual of GPR (a) Full featured (b) Reduced featured. . . . .                                             | 144 |

|                                                                                                  |     |
|--------------------------------------------------------------------------------------------------|-----|
| 7.18 Predicted responses with associated 95% confidence intervals from the GPR<br>model. . . . . | 145 |
|--------------------------------------------------------------------------------------------------|-----|

# List of Tables

|     |                                                                                         |     |
|-----|-----------------------------------------------------------------------------------------|-----|
| 1.1 | Failure mechanism in PCT devices both press-pack and PCT insulated modules.             | 8   |
| 2.1 | Comparative summary of high current thyristor devices available in market.              | 21  |
| 3.1 | Electrical and thermal analogy.                                                         | 51  |
| 3.2 | Extracted thermal parameters.                                                           | 53  |
| 3.3 | Temperature measured at each thermocouple.                                              | 57  |
| 4.1 | Measured surge current and corresponding forward voltage.                               | 70  |
| 4.2 | Extracted parameters under different surge current conditions.                          | 73  |
| 5.1 | Technology aspects of high power semiconductor devices.                                 | 84  |
| 5.2 | Comparison of electrical and thermal characteristics: Press pack vs module.             | 92  |
| 6.1 | Change in silicon current.                                                              | 107 |
| 6.2 | Molybdenum current variation.                                                           | 107 |
| 6.3 | Diameter classes and corresponding included diameters.                                  | 107 |
| 6.4 | Sample of dataset features used in the proposed model.                                  | 108 |
| 6.5 | Architecture of machine learning models.                                                | 112 |
| 6.6 | Model performance on validation and test datasets.                                      | 114 |
| 6.7 | Computational performance metrics for classification and regression-based prediction.   | 115 |
| 6.8 | Model performance on validation and test datasets with optimized parameters.            | 117 |
| 6.9 | Comparative performance of optimized regression models for average current forecasting. | 119 |
| 7.1 | Dataset features used in the proposed model, including average current details.         | 129 |
| 7.2 | Architecture of machine learning models for classification models.                      | 131 |
| 7.3 | Architecture of machine learning models for regression models.                          | 132 |
| 7.4 | Model performance on validation and test datasets.                                      | 136 |

|     |                                                                                                                              |     |
|-----|------------------------------------------------------------------------------------------------------------------------------|-----|
| 7.5 | Computational performance metrics for classification. . . . .                                                                | 136 |
| 7.6 | Comparison of testing and validation performance of regression models. . .                                                   | 140 |
| 7.7 | Comparative testing and validation performance of reduced-feature regression models for average current forecasting. . . . . | 142 |
| 7.8 | Computational performance metrics for prediction: Full featured and reduced featured. . . . .                                | 144 |



# List of Publications

## Journal Articles

1. **F. Ahmad**, L. Vaccaro, A. A. Nkembi, M. Marchesoni, and F. Portesine, "*Classification and Prediction of Average Current in High-Power Semiconductor Devices: A Machine Learning Framework*," *Electronics*, vol. 15, no. 6, p. 1149, Mar. 2026.  
DOI: <https://doi.org/10.3390/electronics15061149>
2. **F. Ahmad**, L. Vaccaro, A. A. Nkembi, M. Marchesoni, F. Portesine, and G. Anyanwu, "*Junction Temperature and Failure Behavior of High-Power Press Pack vs. Module Diodes Under High Anomalous Surge Currents*," *Electronics*, vol. 15, no. 1, p. 121, Dec. 2025.  
DOI: <https://doi.org/10.3390/electronics15010121>
3. **F. Ahmad**, L. Vaccaro, A. A. Nkembi, M. Marchesoni, and F. Portesine, "*Surge Current Analysis of High-Power Press Pack Diodes: Junction Temperature and Forward-Voltage Modelling*," *Electronics*, vol. 14, no. 24, p. 4899, Dec. 2025.  
DOI: <https://doi.org/10.3390/electronics14244899>
4. **F. Ahmad**, L. Vaccaro, A. A. Nkembi, and F. Portesine, "*Classification and Prediction of Chip Diameter in High-Power Semiconductor Devices Through Electrical Parameters Using Machine Learning*," *Technologies*, vol. 13, no. 12, p. 567, Dec. 2025.  
DOI: <https://doi.org/10.3390/technologies13120567>
5. A. A. Nkembi, D. Santoro, **F. Ahmad**, I. Kortabarria, P. Cova, E. Sacchi, and N. Delmonte, "*Novel Droop-Based Techniques for Dynamic Performance Improvement in a Linear Active Disturbance Rejection Controlled Dual Active Bridge for Fast Battery Charging of Electric Vehicles*," *Energies*, vol. 17, no. 20, p. 5171, Oct. 2024.  
DOI: <https://doi.org/10.3390/en17205171>
6. A. A. Nkembi, D. Santoro, **F. Ahmad**, I. Kortabarria, P. Cova, E. Sacchi, and N. Delmonte, "*A Novel Feedforward Scheme for Enhancing Dynamic Performance of*

*Vector-Controlled Dual Active Bridge Converter with Dual Phase Shift Modulation for Fast Battery Charging Systems,"* **Electronics**, vol. 13, no. 19, p. 3791, Sep. 2024.  
DOI: <https://doi.org/10.3390/electronics13193791>

## Conference Proceedings

1. **F. Ahmad**, F. Portesine, M. Ashero, and L. Vaccaro, "*Transient Thermal Impedance Characterization of New High-Power Press Pack Diodes,*" in **Proceedings of the 2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)**, Jun. 2024.  
DOI: <https://doi.org/10.1109/SPEEDAM61530.2024.10608828>
2. Armel Asongu Nkembu, **Fawad Ahmad**, Iñigo Kortabarria, Paolo Cova, Nicola Delmonte, and Danilo Santoro, "*Performance Comparison of Different Modular Dual Active Bridge Converter Topologies for Fast Battery Charging Applications,*" in **Proceedings of the 2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)**, Jun. 2024.  
DOI: <https://doi.org/10.1109/SPEEDAM61530.2024.10609166>



# List of Symbols

| Symbol            | Description                              | Unit                                 |
|-------------------|------------------------------------------|--------------------------------------|
| $A$               | Surface Area                             | $\text{m}^2$                         |
| $A(z)$            | Effective Area at Thickness $z$          | $\text{m}^2$                         |
| $c_T$             | Specific Heat Capacity                   | $\text{J}/(\text{kg}\cdot\text{K})$  |
| $d$               | Layer Thickness                          | $\text{m}$                           |
| $h$               | Convective Heat Transfer Coefficient     | $\text{W}/(\text{m}^2\cdot\text{K})$ |
| $I_{AV}$          | Average Current                          | $\text{A}$                           |
| $I_C$             | Collector Current                        | $\text{A}$                           |
| $I_{\text{Peak}}$ | Peak Current                             | $\text{A}$                           |
| $I_{RRM}$         | Peak Reverse Current                     | $\text{A}$                           |
| $K_T$             | Thermal Conductivity                     | $\text{W}/(\text{m}\cdot\text{K})$   |
| $P_0$             | Peak Power Amplitude                     | $\text{W}$                           |
| $Q$               | Heat Flow                                | $\text{W}$                           |
| $Q_w$             | Heat Dissipation Paths                   | $\text{W}$                           |
| $R^2$             | Coefficient of Determination             | –                                    |
| $R_{th}$          | Thermal Resistance                       | $\text{K}/\text{W}$                  |
| $R_{th(j-h)}$     | Junction to Heat Sink Thermal Resistance | $\text{K}/\text{W}$                  |
| $r_T$             | Slope Resistance                         | $\Omega$                             |
| $r_{T0}$          | Reference Slope Resistance               | $\Omega$                             |
| $t$               | Time                                     | $\text{s}$                           |
| $t_0$             | Time Shift of Gaussian Dip               | $\text{s}$                           |
| $T$               | Pulse Duration                           | $\text{s}$                           |
| $T_a$             | Ambient Temperature                      | $^{\circ}\text{C}$                   |
| $T_c$             | Case Temperature                         | $^{\circ}\text{C}$                   |
| $T_j$             | Junction Temperature                     | $^{\circ}\text{C}$                   |
| $V_{CE}$          | Collector Emitter Voltage                | $\text{V}$                           |
| $V_F$             | Forward Voltage Drop                     | $\text{V}$                           |
| $V_{TH}$          | Threshold Voltage                        | $\text{V}$                           |
| $V_{T0}$          | Reference Threshold Voltage              | $\text{V}$                           |
| $Z_{th}$          | Thermal Impedance                        | $\text{K}/\text{W}$                  |
| $Z_{th(j-c)}$     | Junction to Case Thermal Impedance       | $\text{K}/\text{W}$                  |
| $\alpha$          | Temperature Coefficient of Resistivity   | $1/\text{K}$                         |

| Symbol        | Description             | Unit              |
|---------------|-------------------------|-------------------|
| $\beta$       | Attenuation Coefficient | —                 |
| $\varepsilon$ | Gaussian Noise Vector   | —                 |
| $\rho$        | Material Density        | kg/m <sup>3</sup> |
| $\sigma$      | Standard Deviation      | —                 |
| $\sigma^2$    | Variance                | —                 |
| $\tau_i$      | Time Constant           | s                 |



# List of Abbreviations

| Abbreviation | Description                                        |
|--------------|----------------------------------------------------|
| AI           | Artificial intelligence                            |
| AlN          | Aluminum nitride                                   |
| ANNs         | Artificial neural networks                         |
| CNN          | Convolutional neural network                       |
| CTE          | Coefficient of thermal expansion                   |
| DT           | Decision tree                                      |
| DUT          | Device under test                                  |
| FEA          | Finite element analysis                            |
| FEM          | Finite element method                              |
| FDM          | Finite Difference Method                           |
| FVM          | Finite Volume Method                               |
| GaN          | Gallium Nitride                                    |
| GD           | Gaussian distribution                              |
| GPR          | Gaussian process regression                        |
| HVDC         | High-voltage direct current                        |
| IEC          | International Electrotechnical Commission          |
| IGBTs        | Insulated-gate bipolar transistors                 |
| IR           | Infrared thermography                              |
| JEDEC        | Joint Electron Device Engineering Council          |
| LTI          | Linear time-invariant                              |
| MAE          | Mean absolute error                                |
| MAPE         | Mean absolute percentage error                     |
| ML           | Machine learning                                   |
| MOSFETs      | Metal–oxide–semiconductor field-effect transistors |
| MRMR         | Minimum redundancy maximum relevance               |
| MSE          | Mean square error                                  |
| PCA          | Principal component analysis                       |
| PCT          | Pressure contact technology                        |
| PLECS        | Piecewise linear electrical circuit simulation     |
| POD          | Proper orthogonal decomposition                    |

**Abbreviation Description**

---

|       |                                                     |
|-------|-----------------------------------------------------|
| RC    | Resistor–capacitor                                  |
| RMS   | Root mean square                                    |
| RMSE  | Root mean square error                              |
| SHAP  | Shapley Additive Explanations                       |
| SiC   | Silicon Carbide                                     |
| SOA   | Safe operating area                                 |
| SPICE | Simulation program with integrated circuit emphasis |
| SRC   | Semiconductor Research Corporation                  |
| SVMs  | Support vector machines                             |
| TSEPs | Temperature-sensitive electrical parameters         |
| TSOPs | Temperature-sensitive optical parameters            |
| VRRM  | Peak reverse repetitive voltage                     |





# Chapter 1

## Introduction

This chapter presents the importance of electro-thermal modeling of high-power semiconductor devices, with particular focus on diodes, considering the growing demand for improved device reliability and operational efficiency. It highlights the major challenges arising from elevated junction temperature during transient and surge operating conditions, which contribute to performance deterioration and potential device failure. In addition, the chapter defines the research gap and states the study objectives, highlighting the importance of electro-thermal modeling techniques, consideration of packaging and assembly effects, and the incorporation of data-driven methodologies. Finally, it presents an overview of the thesis structure, explaining how each chapter is designed to address and fulfill the proposed research objectives.

### 1.1 Overview and Research Motivation

High-power semiconductor devices, particularly high-power press pack diodes and thyristors, are fundamental components in modern power electronics and industrial applications such as high voltage direct current (HVDC) transmission [1, 2], electric vehicle fast charging [3, 4], hydrogen electrolysis, traction power supplies [5], voltage regulation, and multilevel converters [6–8]. Initially, these devices, mostly based on silicon, were designed for low-power applications where operations required a limited range of power density, resulting in limited thermal performance concerns [9]. However, with advancements in semiconductor technology, the demand for robust power conversion systems has increased, resulting in a growing need for the development of better high-power semiconductor devices [10]. The increasing demand for high power densities in these applications has motivated manufacturers to develop advanced power semiconductor devices with improved designs and new packaging techniques to optimize power dissipation in order to meet the required power

ratings [11]. Thermal behavior, especially junction temperature, remains a critical factor that may compromise the device safety [12, 13]. Regardless these advances, an excessive rise in temperature due to power dissipation may result in performance degradation, premature aging, and catastrophic device failure [13, 14]. Therefore, accurate estimation of junction temperature is critical for optimizing power dissipation, enhancing reliability, and maintaining safe operation within specific thermal limits.

### 1.1.1 Role of High Power Devices in Power Electronics

Over the past few decades, the growing demand for efficient energy conversion and control has been a key factor in the advancement of power electronics [15, 16]. Early systems were mostly based on semiconductor devices with limited voltage and current handling capabilities. The devices were also used for operations with low switching frequencies [17]. Over the time, the demands for higher power density, efficiency, compactness, and reliability increased [18]. This expanded power electronics into more demanding application domains such as HVDC, renewable energy integration, industrial motor drives, and electrified transportation systems [19–21]. High-power semiconductor devices, especially high power diodes and thyristors, are considered as critical elements to perform operation of these systems by enabling efficient switching, rectification, and control of higher voltages and currents [22–25]. However, during fault conditions, switching transients, and surge events, these devices are often exposed to severe transient over-currents [26–28]. Under such conditions, the device is subjected to extensive electro-thermal stress, leading to instantaneous power dissipation. The sudden increase in power dissipation results in rapid and highly non-uniform temperature rises [29, 30]. Therefore, it is very important to analyze the electrical and thermal behavior in order to predict device performance, ensure safe operation, and improve reliability. The importance of high-power devices has grown considerably alongside the electrification of modern energy systems. The transition from conventional gasoline and diesel vehicles to electric, hybrid, and fuel-cell vehicles has been strongly supported by significant improvements in the performance, efficiency, size, and cost of power semiconductor devices [31–33]. In electric and hybrid vehicles, power semiconductor devices regulate energy flow between batteries, traction motors, and charging systems [34–36]. In grid-connected converters and industrial drives, they must withstand demanding operational conditions including transient overloads and fault-induced current surges [37–39]. In all these applications, device failure under surge conditions represents a critical reliability concern, making the accurate characterization of device behavior under such events a topic of significant practical importance.

With the development of next-generation semiconductor materials has further improved the performance of high power devices in modern power electronics applications [15]. At present, silicon-based devices are widely used in most applications due to the already well established equipment and industry; however, wide bandgap materials, such as SiC and GaN, offer higher switching speeds, improved thermal performance, and lower power losses [40–42]. These characteristics result in more compact and efficient power converters for various applications, including renewable energy systems, electric transportation, and industrial drives. As modern energy systems increasingly move toward electrification and higher power density, improving the performance and reliability of high-power semiconductor devices has become a key research focus in power electronics.

### 1.1.2 Reliability of High Power Devices

The existing limitations, as discussed above, become critical, particularly under transient and abnormal operating conditions, such as fault and surge current events, where devices are subjected to extremely high current levels over very short time durations [43]. Under these conditions, the electrical stress leads to intense power dissipation, which in turn causes a rapid and spatially non-uniform junction temperature rise governed primarily by transient thermal impedance [44]. These abrupt changes in temperature exceed those observed during steady-state operation, defining increasing temperature as a dominant factor governing device performance, lifetime, and failure risk [45]. Unlike steady-state operation, transient regimes are dominated by thermal capacitance and short-term heat diffusion effects, resulting in steep temperature gradients within the device structure. As power densities continue to increase in modern power electronic applications, the ability of semiconductor devices to safely withstand such transient thermal loads has become a decisive design and qualification criterion. Consequently, accurate evaluation of thermal behavior is essential under abnormal conditions in order to ensure reliable operation and device safety. This motivates the development of advanced electro-thermal modeling and analysis methodologies that are capable to capture transient temperature evolution and internal thermal gradients. Failure behavior in semiconductor devices mainly occurs due to elevated junction temperatures [46], which arise from the combined interaction of electrical loading, thermal impedance, and material properties, as illustrated in Figure 1.1. These failures typically indicate material degradation, interconnect fatigue, solder fatigue and delamination, or cracking of critical device regions, particularly the semiconductor chip. Importantly, the non-uniform temperature distribution generated during transient surge events concentrates thermo-mechanical stress at packaging interfaces, causing failures to originate at locations such as the die attach, bond wires, substrates, and molding compounds [47].

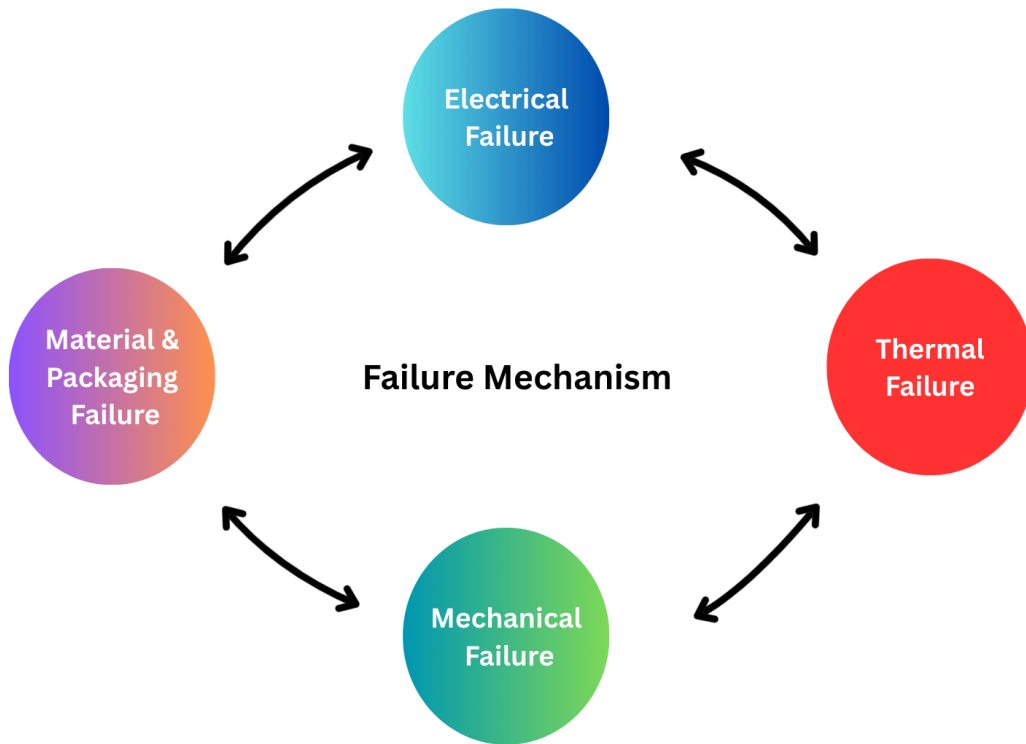


Fig. 1.1 Some notable factors impacting device reliability and leading to device degradation and failure.

Mismatches in the coefficient of thermal expansion (CTE) between dissimilar materials actuate thermo-mechanical stresses during thermal or power cycling, leading to interfacial cracking, delamination, or bond-wire lift-off [48]. The degradation mechanisms associated with packaging are significantly increased during high surge current conditions, where rapid thermal gradients elevate local stress levels well beyond those encountered during prolonged steady operation. Consequently, packaging-dependent failure mechanisms emerge as a significant reliability issue under surge conditions, which underscores the requirement for modeling techniques that explicitly incorporate transient electro-thermal behavior and realistic packaging effects.

### 1.1.3 Need for Electro-Thermal Modeling

Electro-thermal modeling is considered an important tool for the accurate analysis, design, and reliability assessment of high-power semiconductor devices [49, 50]. These models allow the coupled evaluation of electrical operation and heat generation under realistic operating conditions [51]. Electrical conduction and switching processes inherently generate heat, while the resulting temperature rise directly alters key electrical parameters such as

on-state resistance, carrier mobility, leakage current, and efficiency, establishing a dynamic feedback mechanism between the electrical and thermal domains. This process becomes more critical in high-power-density applications and transient operating conditions such as fault and surge current conditions [52, 53]. The rapid increase in power dissipation results in steeper junction temperature excursions, which is governed by transient heat diffusion and thermal inertia [28]. Therefore, accurate electro-thermal modeling is required, which is capable of estimating accurate thermal behavior, including precise junction temperature, internal temperature gradients, and hot-spot formation, which directly influence device performance, reliability, and safe operating limits [54–57]. From a reliability perspective, temperature is the dominant factor accelerating degradation mechanisms, including thermo-mechanical stress, interfacial delamination, interconnect fatigue, and material degradation, all of which are intensified under transient electrical stress [58–60]. By incorporating temperature-dependent electrical characteristics and realistic heat transfer, electro-thermal models provide critical insight into failure susceptibility and reliability margins that cannot be obtained through electrical analysis only. In addition, electro-thermal modeling enables the optimization of performance and design of device geometry, packaging architecture, and thermal management strategies, which reduce dependence on extensive experimental tests. When applied to realistic mission profiles and transient loading conditions, these models also enable quantitative assessment of long-term degradation and lifetime [61, 62], making electro-thermal modeling an indispensable tool for the reliable design and qualification of high-power semiconductor devices operating under extreme electrical and thermal stress conditions.

#### **1.1.4 Role of Electrothermal Modeling in Device Analysis**

The significant advances in the development of electro-thermal models and their effectiveness in addressing several issues have improved the reliability of power semiconductor devices; however, their performance and robustness still remain highly susceptible to high surge current levels [63]. In abnormal scenarios, such as short circuits across devices, the current can increase instantaneously within milliseconds, resulting in a fast and significant rise in temperature [64, 65]. Such abrupt thermal changes can instantaneously affect the structural integrity and long-term reliability of semiconductor devices [66]. Importantly, such surge events are inherent to practical power electronic converter operation and cannot be entirely avoided through control or protection strategies alone. Therefore, it is critical to assess both thermal and electrical characteristics of devices in order to define safe surge current limits, ensuring reliable operation under fault conditions. To encounter this challenge, manufacturers usually provide surge current ratings in device datasheets. These ratings are mostly based

on extensive experimental tests and electro-thermal simulations conducted according to standardized procedures defined by various organizations such as the Joint Electron Device Engineering Council (JEDEC) and the International Electrotechnical Commission (IEC) [67, 68]. These standardized methodologies provide a benchmark for device qualification under transient surge conditions, reflecting the crucial role of junction temperature in device degradation, chip failure, and deterioration of key electrical parameters such as on-state resistance, which directly affects the voltage drop during conduction. These standardized surge ratings give a useful reference; moreover, these models are typically derived under realistic device structure and operating conditions and fully account for device-specific transient thermal behavior, packaging-dependent thermal paths, or dynamic variations in electrical parameters. Consequently, such ratings are also validated with experimental tests to reflect the actual surge capability or failure limits of devices under realistic operating conditions. However, performing large numbers of simulations or experimental tests for different operating conditions can be time-consuming.

### **1.1.5 Failure Mechanisms and Reliability Challenges in Power Semiconductor Devices**

Failure behavior in semiconductor devices primarily occurs due to elevated junction temperatures, which arise from multiple interacting factors. These failure mechanisms have been detailed discussed in [69–71]. They typically result as material degradation, interconnect fatigue, solder fatigue, delamination, or cracking of critical device regions, especially the chip. Failures that arise due to packaging and material stresses usually originate at interfaces such as the die attach, bond wires, substrate, and molding compounds. Mismatches in the CTE between two dissimilar materials induce thermo-mechanical stresses due to thermal or power cycling, which can lead to interfacial cracking, delamination, or bond-wire lift-off. Furthermore, voids or delamination in solder and die attach layers also increase thermal resistance, resulting in localized hot spots and accelerated degradation [72–74]. Failures that are initiated due to mechanical stresses are usually driven by external perturbations such as vibration, shock, or handling stress [75, 76]. Encapsulation-induced stress can also contribute significantly, where uneven stress distribution in molding compounds causes die cracking or initiates delamination at weak interfaces [77]. Failures that occur due to thermal stresses are primarily associated with rise in temperature, gradients, as well as thermal cycling [78]. Repeated thermal cycling induces fatigue in solder joints and bond wires, while localized hot spots cause differential expansion and accelerate crack propagation. At elevated temperatures, creep in solder and die attach layers further compromises structural and thermal integrity.

In extreme cases, a positive feedback between temperature rise and leakage current may initiate thermal runaway, culminating in catastrophic device failure. Failures that occur due to electrical overstress, are usually triggered by conditions such as increase in blocking voltage, higher surge current levels, and over voltage transients [79, 80]. Apart from this, other mechanisms include thermal fatigue during fast commutation, avalanche breakdown, and gate-oxide degradation. Mostly these failures occurs abruptly, leading to immediate device destruction. While robust protection circuits can reduce the risk, they may not prevent irreversible damage. Electrical overstress can result in increase leakage current and forward voltage drop which may lead in short-circuit conditions, metallization melting, or even chip fracture[72]. Moreover, PCT devices also eliminate traditional bond-wire and solder-related degradation by relying on direct contact between the die and electrodes. However, failures in these devices still arise due to interface degradation associated instabilities, as detailed in Table 1.1.

Table 1.1 Failure mechanism in PCT devices both press-pack and PCT insulated modules.

| Failure Mechanism            | Blocking Voltage                            | Over Voltage               | High Current (Surge)                                                      | Thermal Fatigue                                    | Failure During Commutation                                                |
|------------------------------|---------------------------------------------|----------------------------|---------------------------------------------------------------------------|----------------------------------------------------|---------------------------------------------------------------------------|
| Origin                       | Internal to devices (manufacturing origin)  | External circuit           | External circuit or consequence of internal short circuit                 | High Temperature variation (High Thermal cycling)  | Peak of voltage or current during commutation                             |
| Preliminary effects          | Increase and instability of leakage current | -                          | Increase of VF (forward voltage during conduction)                        | Increase of VF (forward voltage during conduction) | Peak or voltage and current during commutation detectable by oscilloscope |
| Final effect                 | Short Circuit of devices                    | Short Circuit of devices   | Short Circuit of devices                                                  | Short Circuit of devices                           | Short Circuit of devices                                                  |
| Chip failure localization    | No easy to detect on the chip               | Fusion on the edge of chip | Degradation of aluminum metallization and fusion of large area of silicon | Degradation surface contact by thermal fatigue     | Small fusion at the center of cathode region                              |
| Role of junction temperature | Medium                                      | No relevant                | High                                                                      | High                                               | High                                                                      |

The primary failure mechanisms include fretting damage, micro-eroding, gate-oxide damage, spring fatigue and stress relaxation [81, 82]. In welding and brazed diodes, the failure mechanism of bond wire lift-off can lead to an open circuit condition, which may generate an arc. The resulting electric shock can trigger an explosion outside the device, posing hazards to the external environment. In contrast, PCT diodes contain no bond wires; therefore, under high current and voltage conditions, failure manifests as a short circuit, leading to elevated temperatures and eventual chip fracture rather than arc formation. All failure phenomenon are monitored using prognostics and health management techniques



through various health indicators such as on-state voltage  $V_{CE,sat}$  [83, 84], threshold voltage  $V_{th}$  [85], switching waveforms [86], case temperature  $T_c$  [87], and thermal impedance  $Z_{th}$  [88]. Notably,  $T_c$  and  $Z_{th}$  can distinguish between bond-wire lift-off and solder layer degradation, enabling detailed failure mechanism analysis. Bond-wire lift-off is monitored by measuring the relative health indicator at a fixed junction temperature, although this requires precise  $T_j$  and power loss measurements [89–91].  $T_c$  is also proposed as an indicator for solder layer degradation; however, sensor placement between the case and heatsink can impact heat dissipation efficiency [87]. Alternative approaches use on-state voltage and bond-wire voltage drop as damage indicators. on-state voltage for temperature estimation, predicting solder joint failures that increase thermal resistance, and bond-wire voltage drop to detect bond-wire degradation [92]. In this context, data-driven approaches have recently emerged as a promising complementary tool for device modeling and analysis.

## 1.2 Machine Learning in Power Electronics

Machine learning (ML) techniques have recently become effective tool to address complex modeling and design challenges across a wide range of domains [93–95]. Particularly, in power electronics applications, several ML models have been developed for semiconductor device characterization, fault diagnostics, and condition monitoring, thereby complementing conventional analytical and numerical approaches [96–102]. Conventional physics-based models are usually based on complex physical equations that represent carrier transport, thermal effects, and device behavior. These models results in optimal physical interpretability, however, their implementation often requires detailed knowledge of device physics, leading to intensive computation. In contrast, ML-based models are capable to predict outputs on the underlying relationships between input parameters and device responses learned directly from data [103]. Consequently, ML approaches can analyze complex electrical, thermal, and structural interactions without solving the governing physical equations. ML models can be integrated with finite element analysis (FEA) to estimate the equivalent resistivity and thermal conductivity, chip-level thermal mapping and the prediction of temperature change rates of semiconductor chips under various operating conditions with improved accuracy [104, 105]. Apart from this, the efficiency of computation of trained ML models is also high which provide an advantage over traditional physics-based simulations. Once the model is trained, ML models can produce predictions multiple times faster than full numerical simulations. This enable rapid exploration of large parameter spaces and feasibility to train complex models on extensive datasets. This capability is valuable for both system level and device-level design tasks, where evaluating numerous device configurations using physics-

based electro-thermal simulations would be computationally complex [106].

ML models can be generally divided into supervised, unsupervised, and reinforcement learning categories. Supervised models are further divided into classification and regression approaches: classification assigns data to predefined groups or classes, whereas regression predicts exact numerical values based on patterns learned from previous data. Unsupervised learning methods are more appropriate for pattern discovery and clustering in unlabeled datasets, whereas reinforcement learning is primarily employed for control and optimization problems. Within the supervised learning approach, several algorithms have been applied to power electronics and semiconductor device modeling, including artificial neural networks (ANNs), support vector machines (SVMs), ensemble methods such as random forests and gradient boosting, and deep learning architectures [107–111]. These models have shown particular effectiveness in capturing the complex nonlinear relationships inherent in electro-thermal device behavior, due to their flexible architectures and strong function approximation capabilities. This demonstrates the significant potential of applying ML in modeling, manufacturing, and predictive analysis for semiconductor applications [112].

### 1.3 Challenges in Device modeling and Analysis

The electro-thermal modeling and analysis of high-power semiconductor devices are explored extensively in literature, resulting in advanced and improved models; however, several key challenges still require further studies, such as transient and high surge current conditions. These factors may influence the performance of the device and lead to lower accuracy, compromised reliability, and complex industrial applicability of existing modeling and analysis methodologies. The key challenges are highlighted as follows:

**Surge Analysis at Very High Anomalous Current Levels:** Semiconductor devices may be subjected to extreme surge current levels in various high-power applications, that can exceed far beyond their nominal operating range. Many studies were conducted to investigate surge behavior at current levels ranging from tens to several hundred amperes [113–117], however, real-world applications, such as HVDC systems and traction converters, can expose devices to surge currents in the kiloampere range. Therefore, the lack of systematic analysis at such higher current levels limits the relevance of existing surge capability assessments for high-power applications.

**Limited Representation of Dynamic Electrical Behavior:** Conventional surge current analysis mostly rely on static or linearized current–voltage characteristics or depend on experimental measurement tests [114, 118]. Such assumptions are not sufficient to capture the temperature dependence of key electrical parameters, including forward voltage drop

and slope resistance in high-current transients. Consequently, these models fail to effectively characterize the associated electro-thermal feedback mechanisms that influence device behavior under surge conditions.

**Challenges in Experimental Validation at High Surge Currents:** Experimental validation of device performance at extreme surge current levels is very challenging due to safety issues, performance degradation, and the risk for catastrophic failure to the device. As a result, numerous studies are only based on simulations, lacking experimental validation or depend on simplified or restrained testing conditions that fail to represent actual surge scenarios. This limitation lowers the validation of model predictions and limits its applicability to practical reliability evaluation.

**Insufficient Consideration of Packaging-Dependent Thermal Behavior:** The influence of packaging technology on transient thermal behavior and surge robustness is often treated implicitly or neglected in the literature. Factors such as thermal contact resistance, mechanical compliance, and heat flow paths play a critical role in determining junction temperature evolution during surge events. The absence of systematic, packaging-aware analysis limits understanding of how different device assemblies influence surge capability and failure behavior.

**Lack of Data-Driven Tools for Device-Level Design Parameters:** The use of ML models is increasing day by day in power electronics applications; however, most existing studies only focus on system-level control, fault detection, or converter optimization. Data-driven tools specifically targeting device-level design parameters, such as chip diameter and average current capability, are not explored, although these are very crucial for device selection, design optimization, and reliability assessment.

**Limited Interpretability of Machine Learning Models:** Numerous ML models results in higher prediction accuracy but they are unable to provide sufficient physical interpretability. The lack of insight into feature importance and model decision processes are useful for semiconductor device designers, giving transparent and physically meaningful guidance to support engineering decisions.

## 1.4 Research Objectives

In high-power semiconductor devices, power dissipation increases with the increasing current, allowing junction temperature to rise, which may lead to performance degradation and device failure. This research focuses on the investigation of the electro-thermal behavior and reliability of high-power semiconductor devices operating under high surge current conditions. In particular, this work emphasizes the accurate thermal characterization of

transient thermal impedance. Moreover, the key objective of this work is the development of a methodology to accurately predict forward voltage behavior and estimate junction temperature under high surge current conditions, where direct temperature measurement is not feasible and conventional static electrical models are insufficient. The proposed methodology is intended to improve the accuracy of junction temperature estimation during transient operation.

In addition, this dissertation seeks to investigate the influence of packaging technologies, both experimentally and numerically, on surge current capability and failure behavior. For this purpose, a key objective is to conduct a comparative analysis of press-pack and insulated module semiconductor devices under identical electrical and thermal stress conditions. Moreover, recognizing the increasing diversity of high-power semiconductor devices and the growing application of ML in power electronics, this research aims to introduce data-driven ML frameworks. Hence, the main objective is to develop methodologies that have the capability to predict key device design parameters, such as chip diameter and average current capability, based on electrical and thermal characteristics. These frameworks are intended to complement physics-based modeling approaches by capturing nonlinear relationships that are difficult to represent analytically.

## 1.5 Organization of the Thesis

The thesis is structured to provide a comprehensive and systematic study and analysis of electro-thermal behavior, surge current reliability, packaging-dependent performance, and data-driven characterization of high-power semiconductor devices. The organization progresses from fundamental operating principles and state-of-the-art analysis to advanced modeling methodologies, experimental validation, and predictive frameworks. The structure of the thesis is outlined as follows:

- **Chapter 1: Introduction**

This chapter presents the background and motivation of the research, emphasizing the importance of electro-thermal reliability in high-power semiconductor devices operating under transient and surge conditions. It outlines the key challenges, identifies the research gaps, formulates the problem statement, defines the research objectives, and summarizes the scientific contributions of the thesis. The chapter concludes with an overview of the thesis organization.

- **Chapter 2: Operating Principles of High-Power Semiconductor Devices**

This chapter reviews the fundamental operating principles of high-power diodes and

thyristors, with particular emphasis on press-pack and insulated module configurations. It discusses packaging technologies, heat generation mechanisms, heat flow paths, and junction temperature formation. The chapter further reviews thermal resistance, thermal capacitance, and transient thermal impedance concepts, followed by a comprehensive literature survey of measurement-based and simulation-based thermal modeling techniques. In addition, recent applications of ML in power electronics and semiconductor device analysis are reviewed to establish the context for data-driven modeling approaches.

- **Chapter 3: Transient Thermal Impedance Characterization of High-Power Devices**

This chapter focuses on the development and validation of an electro-thermal modeling framework for accurate characterization of transient thermal impedance in high-power press-pack semiconductor devices. Thermal parameters are extracted, and equivalent Cauer and Foster thermal networks are derived. Experimental validation is presented, demonstrating accurate junction temperature estimation under transient operating conditions.

- **Chapter 4: Surge Current Analysis and Electro-Thermal Modeling**

This chapter presents a detailed electro-thermal analysis of high-power semiconductor devices subjected to high surge current conditions. A forward-voltage-based methodology is developed to estimate junction temperature under surge events. A dedicated experimental setup generating a 10 ms half-sine surge current waveform is introduced, and experimental measurements are combined with numerical simulations to validate the proposed modeling approach and analyze transient thermal behavior.

- **Chapter 5: Impact of Packaging Technologies and Failure Behavior**

This chapter investigates the influence of packaging technology on surge current capability and failure behavior through a comparative analysis of press-pack and insulated module diode assemblies with identical chip dimensions and electrical ratings. Electro-thermal simulations supported by experimental data are used to estimate junction temperature evolution, identify thermal limitations, and analyze packaging-dependent failure mechanisms under high-stress surge conditions.

- **Chapter 6: Machine Learning-Based Classification and Prediction of Chip Diameter in High Power Devices**

This chapter introduces data-driven modeling frameworks for predicting and classifying key device-level design parameters. ML models are developed to predict chip

diameter using electrical and thermal features extracted from manufacturer datasheets. Moreover, the performance of different ML algorithms is systematically evaluated.

- **Chapter 7: Machine Learning Framework for Average Current Classification and Prediction**

This chapter introduces data-driven modeling frameworks to predict average current capability using electrical and thermal features extracted from manufacturer datasheets. Feature importance and interpretability are analyzed using SHAP methods, and the performance of different ML algorithms is systematically evaluated.

- **Chapter 8: Conclusions and Future Work**

This chapter summarizes the key findings and scientific contributions of the thesis. It discusses the implications of the proposed electro-thermal and data-driven methodologies for device reliability assessment and design optimization. Finally, potential directions for future research are outlined, including extensions to wide-bandgap devices, advanced packaging architectures, and large-scale data-driven reliability analysis.



# Chapter 2

## Fundamentals and Literature Review

This chapter discusses the fundamental concept of high-power semiconductor devices and critically reviews the existing literature, with a keen focus on electro-thermal behavior, surge current, packaging technologies, and data-driven modeling approaches. In section 2.3, the operating principles and fundamental characteristics of high-power semiconductor devices are discussed that establish the physical basis for subsequent analysis. Moreover, different available packaging technologies and device configurations are discussed in section 2.4. Section 2.2 presents data of commercially available high-power diodes and thyristors from leading manufacturers, highlighting ongoing trends in device electrical parameters in industry, including power ratings and chip dimensions. In addition, thermal modeling and junction temperature estimation techniques reported in the existing literature are critically reviewed in section 2.5, including measurement-based and simulation-based approaches. Finally, section 2.6 discusses the application of ML techniques in power electronics and semiconductor device analysis.

### 2.1 Overview

The applications of power electronics, as discussed earlier, operating at high power densities, require accurate thermal characterization to ensure efficiency and reliability [119]. These models can be developed by utilizing various physical and mathematical methods and are capable of estimating the maximum junction temperature in semiconductor devices [120]. These models improve the performance of devices by offering enhanced thermal management [121], resulting in reduced power losses and a prolonged life cycle [122, 123]. The rapid advancements in thermal modeling based on analysis of various parameters such as materials, geometry, operating temperatures, cooling systems, and material interfaces offer a diverse range of thermal management solutions for semiconductor devices [54, 124–126].



These developments create substantial opportunities and establish a robust framework for thermal modeling in power electronics. Many research organizations and standardization bodies have collaborated to establish frameworks for characterization of different parameters in semiconductor devices regarding their applications, acknowledging the critical role of thermal modeling. The IEC, for instance, periodically releases standards such as IEC 60747 that address the specifications and characteristics of semiconductor devices; subsequently, IEC 60146 defines the performance requirements for semiconductor power converters and switches [68], ensuring consistency and reliability across various applications. In addition, the JESD51 (JEDEC) series provides comprehensive standards for thermal characterization of semiconductor packages [67]. By enabling precise temperature prediction and enhancing system competitiveness through design optimization, analysis of material degradation, and advanced packaging techniques, thermal modeling plays a pivotal role in improving system performance and reliability [126–128]. This perspective provides a valuable framework for advancing research on power semiconductor devices, particularly in addressing complex and high-demand applications.

These challenges and the importance of thermal modeling for semiconductors have gained

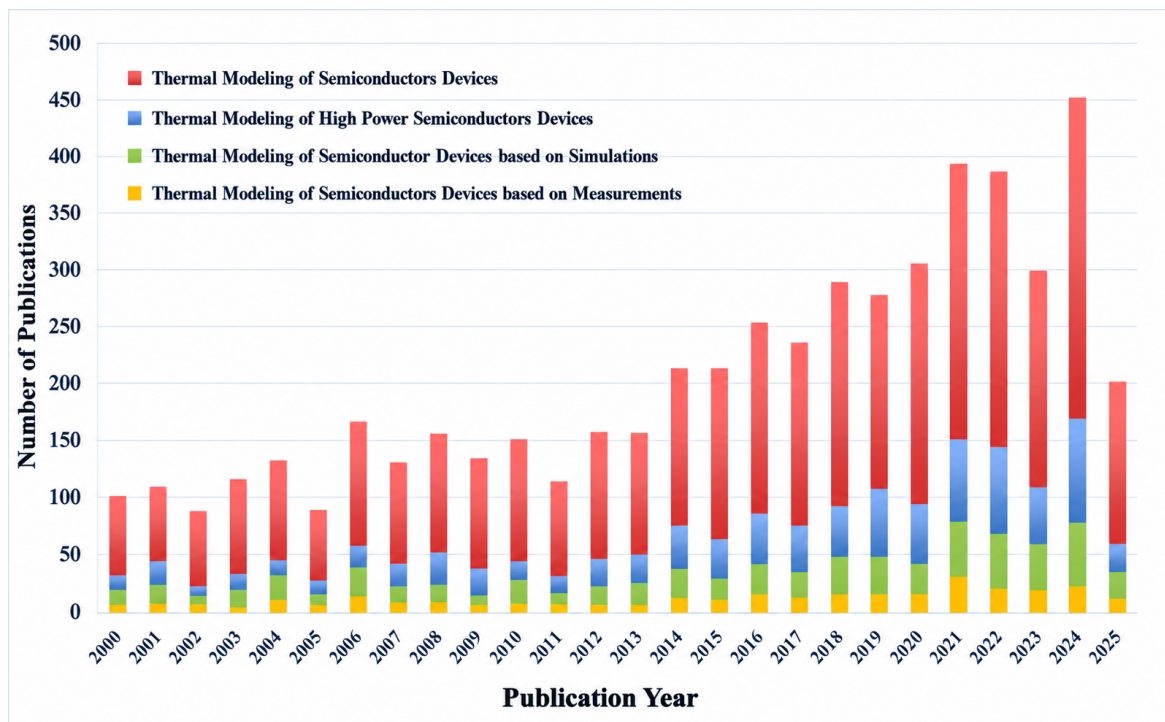


Fig. 2.1 Number of scientific publications on thermal modeling of electronic devices (source: Web of Science).

significant attention from both academia and industry. According to the Web of Science

database, between 2000 and 2025, over 3,546 articles were published on "Thermal Modeling of Semiconductor Devices," with 884 focusing on "Thermal Modeling of High-Power Semiconductor Devices," with more than 70 % appearing in journal articles as shown in Figure 2.1, reflecting substantial innovation and scholarly contribution to this field. A notable portion of this research is funded by national institutes or ministries, primarily focusing on commercially available devices. Recently, the U.S. Department of Commerce, in collaboration with the Semiconductor Research Corporation (SRC), announced the establishment of the SMART USA Institute (Semiconductor Manufacturing and Advanced Research with Twins USA) with \$1 billion in funding [129]. This initiative aims to advance semiconductor technology by leveraging digital twins for optimizing manufacturing, advanced packaging, assembly, and testing processes.

## 2.2 Market Analysis of Power Devices

The manufacturing of high-power semiconductor devices represents an advanced and evolving field, driving innovation across multiple industries by enabling efficient solutions for a wide range of applications. Key device types include diodes, transistors (such as MOSFETs and IGBTs), and thyristors. Diodes are two-terminal devices that permit current flow in only one direction, offering simple and robust functionality. In contrast, transistors and thyristors, featuring three or more terminals, enable signal amplification and switching capabilities, making them suitable for more complex power management tasks. Each of these devices operates based on distinct physical mechanisms, offering specific advantages and trade-offs. However, their primary objective is to maximize energy efficiency in high-power electronic systems. The demand for efficient conversion and growing industrialization has driven the dominance

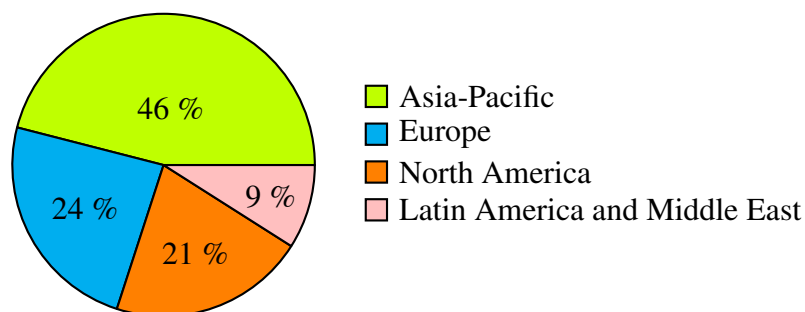


Fig. 2.2 Global market share 2023: Power semiconductors.

of power semiconductors, according to Market.us, the global power semiconductor market is expected to increase to USD 90.5 billion by 2033, up from USD 54.0 billion in 2023 [130],

with Asia-Pacific countries holding the largest share, as depicted in Figure 2.2. Another report projects a 9.1% increase during 2025 and 2034 and highlights that the impact of AI has contributed to the semiconductor market growth, reaching USD 321.1 billion by 2034 [131]. The largest share of total power devices use belongs to applications such as industrial (drives, converters, renewable)[132], automotive (including EV traction applications) [133], IT, telecom & consumer electronics [134], and others (military, aerospace, other) as shown in Figure 2.3

Recent advancements in power semiconductor device design have seen several manufac-

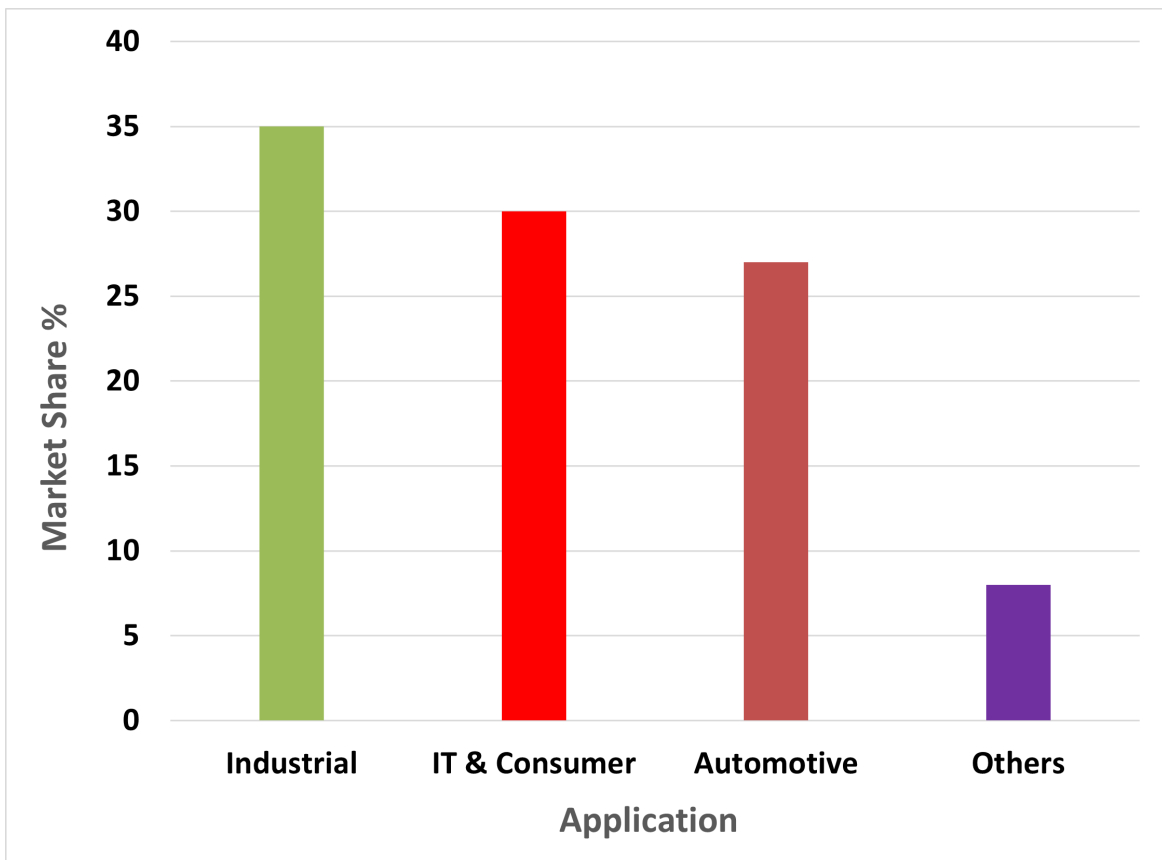


Fig. 2.3 Estimated market share of high power devices by application (2025).

turers develop devices capable of supporting significantly higher current ratings as evident from Table 2.1. For instance, ABB has achieved an average current rating of up to 7612 A, Infineon up to 6110 A, Dynex up to 8750 A, and Poseico Power Electronics S.p.A. up to 8100 A. While these increases in current handling are notable, it is important to highlight that manufacturers have also optimized key parameters, particularly  $V_{RRM}$  (peak reverse repetitive voltage) and chip diameter to facilitate these improvements. The diameter of the chip exhibits a directly proportional relationship with current capacity. In contrast, increasing

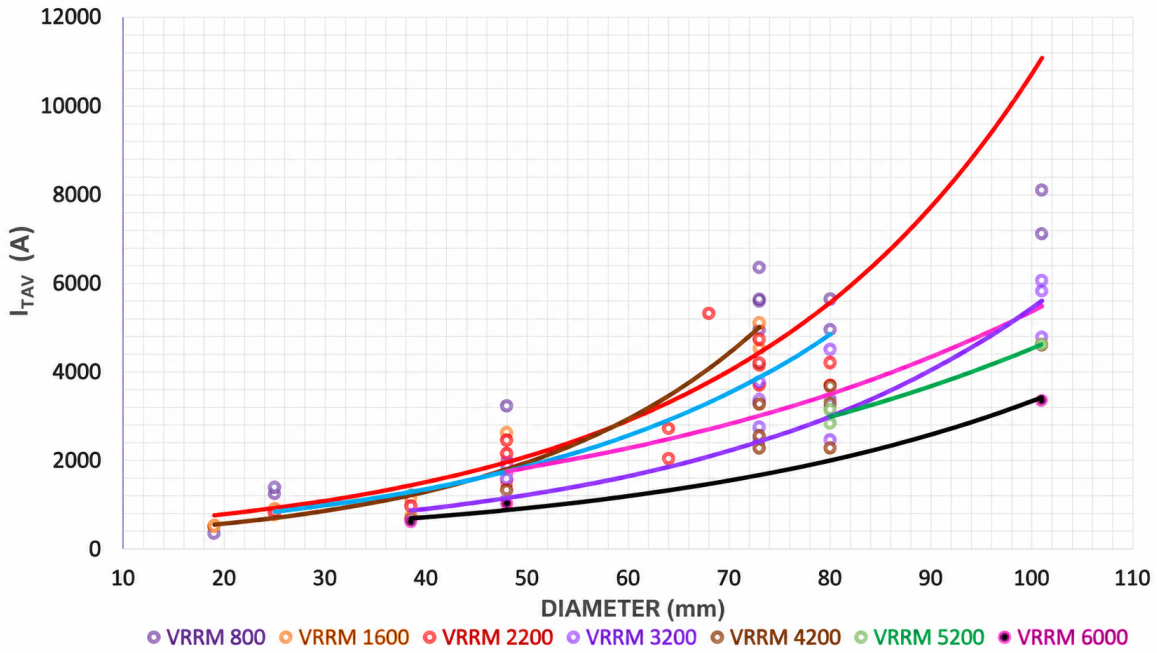


Fig. 2.4 Impact of diameter on electrical characteristics average current and  $V_{RRM}$ .

$V_{RRM}$  tends to reduce current capability, as observed in Figure 2.4. The exponential curves in Figure 2.4 further confirm the linear dependence of current on chip diameter, while also highlighting the decreasing trend of  $V_{RRM}$  with increasing average current. For example, ABB offers devices with current ratings ranging from 5000 A to 6880 A over a  $V_{RRM}$  span of 1800 V to 8500 V. The device 5STP 42L1800, featuring a 78 mm chip diameter and  $V_{RRM}$  of 1800 V, achieves a current rating of 5356 A. Comparatively, multiple ABB devices with a larger 100 mm chip diameter but different  $V_{RRM}$  values (1800 V, 2800 V, and 4200 V) demonstrate a clear trend: the 5STP 50Q1800 ( $V_{RRM} = 1800$  V) attains the highest current of 7612 A. ABB has further increased chip diameters to 110 mm and 143 mm. Devices with a 110 mm diameter use  $V_{RRM}$  values of 5200 V and 6500 V, while those with 143 mm chips use 7200 V and 8500 V. Despite the increase in chip size, devices with lower  $V_{RRM}$  values consistently achieve higher current ratings, such as those with 5200 V and 7200 V for 110 mm and 143 mm diameters, respectively. Furthermore, devices with 143 mm diameters demonstrate lower thermal resistance, contributing to improved current-handling performance. Infineon Technologies has introduced devices with chip diameters ranging from 86 mm to 115 mm. The highest current rating of 6110 A is attained by the device T4771N22TOF PR, featuring a 100 mm chip diameter and  $V_{RRM}$  of 2200 V. In contrast, a device with a larger 115 mm diameter and a higher  $V_{RRM}$  of 5200 V (T4021N52TOH) achieves a lower average current rating of 5460 A. Several other Infineon devices with 100

Table 2.1 Comparative summary of high current thyristor devices available in market.

| Manufacturer | Device Code    | Diameter (mm) | Current (A) | $V_{RRM}$ (V) |
|--------------|----------------|---------------|-------------|---------------|
| ABB          | 5STP 50Q1800   | 100           | 7612        | 1800          |
|              | 5STP 45Q2800   | 100           | 6879        | 2800          |
|              | 5STP 38Q4200   | 100           | 5326        | 4200          |
|              | 5STP 52U5200   | 110           | 6232        | 5200          |
|              | 5STP 48Y7200   | 143           | 6220        | 7200          |
|              | 5STP 45Y8500   | 143           | 5494        | 8500          |
|              | 5STP 42L1800   | 78            | 5356        | 1800          |
| Dynex        | DCR7610H28     | 100           | 8743        | 2800          |
|              | DCR6140H42     | 115           | 6485        | 4200          |
|              | DCR5240H52     | 115           | 5685        | 5200          |
|              | DCR4420H65     | 115           | 4774        | 6500          |
|              | DCR4940V18     | 73            | 5572        | 1800          |
|              | DCR4060V22     | 73            | 4562        | 2200          |
| Infineon     | T4771N22TOF PR | 100           | 6110        | 2200          |
|              | T4021N52TOH    | 115           | 5460        | 5200          |
|              | T3441N52TOH    | 100           | 4410        | 5200          |
|              | T3801N36TOF VT | 100           | 5370        | 3600          |
|              | T3160N18TOF VT | 75            | 4620        | 1800          |
|              | T2810N22TOF VT | 75            | 4070        | 2200          |
| Poseico      | AT908          | 101           | 8099        | 800           |
|              | AT906          | 101           | 7114        | 800           |
|              | AT960          | 101           | 6057        | 3200          |
|              | AT975          | 101           | 4624        | 5200          |
|              | AT706          | 80            | 4947        | 800           |
|              | AT970          | 101           | 4780        | 3400          |

mm chips and  $V_{RRM}$  of 5200 V also demonstrate reduced current capabilities, reinforcing the inverse correlation between  $V_{RRM}$  and current. Dynex Semiconductors has developed the DCR5240H52, which features a 115 mm chip and 5200 V  $V_{RRM}$ , achieving 5685 A. Notably, Dynex has also used 115 mm diameters with varied  $V_{RRM}$  values of 4200 V and 6500 V for the DCR6140H42 and DCR4420H65, yielding current ratings of 6485 A and 4774 A, respectively. The highest current capability among Dynex devices is 8750 A, attained by the DCR7610H28, which uses a 110 mm chip and a relatively moderate  $V_{RRM}$  of 2800 V. This again emphasizes the importance of balancing  $V_{RRM}$  and chip size for maximizing the current. Similarly, Poseico Power Electronics S.p.A. has developed several devices with a consistent chip diameter of approximately 101 mm, paired with varying  $V_{RRM}$  levels: 800 V, 2900 V, 3200 V, 3400 V, and 5200 V. The device AT908, with the lowest  $V_{RRM}$  of 800 V, achieves the highest current of 8100, while the AT975, with a  $V_{RRM}$  of 5200 V, records

the lowest current value of 4624 A among the group. Across all manufacturers, maximum current ratings are predominantly achieved with chip diameters around 100 mm and relatively lower  $V_{RRM}$  values. While increasing chip size generally enhances current capacity, higher  $V_{RRM}$  levels introduce trade-offs due to increased electric field stresses and associated thermal limitations. As silicon-based technologies approach their physical and thermal performance limits, particularly in terms of power density, manufacturers are increasingly investigating alternative materials. Among these, wide-bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) are gaining significant attention. These materials offer superior electrical properties, including higher breakdown voltage, faster switching speed, and improved thermal conductivity, making them ideal candidates for next-generation high-power applications.

## 2.3 Introduction to Semiconductors

This section gives a brief introduction to semiconductors and their fundamental properties. The concepts of doping, the operating principles of high-power diodes, and the characteristics of ideal and practical diodes are also discussed as follows.

### 2.3.1 Semiconductors and Doping

Semiconductors are considered a critical material in defining the foundation and development of modern power electronic systems and devices. These materials offer flexibility to control their electrical properties to optimize device performance and reliability. Intrinsic semiconductors such as silicon (Si) and germanium (Ge), having four valence electrons, result in limited electrical conductivity under normal conditions [135]. However, the addition of a calculated amount of impurities increases their conductivity. The process of adding impurities is known as doping, which produces extrinsic semiconductors. Usually, pentavalent (e.g., phosphorus or arsenic) and trivalent atoms (e.g., boron or gallium) are added to create n-type and p-type semiconductors [136]. N-type materials introduce an extra number of electrons, whereas p-type materials introduce holes, acting as majority carriers, respectively. When these two materials are combined, a P-N junction is created, which allows the flow of current in one direction. After the formation of a p–n junction, layers of positive and negative charges are created near the junction. This occurs when free electrons from the n-type region diffuse across the junction and recombine with holes in the p-type region. These two layers of positive and negative charges form the depletion region as shown in Figure 2.5. The



concentration and distribution of these dopants strongly influence the electrical behavior, breakdown capability, and thermal performance of power semiconductor devices.

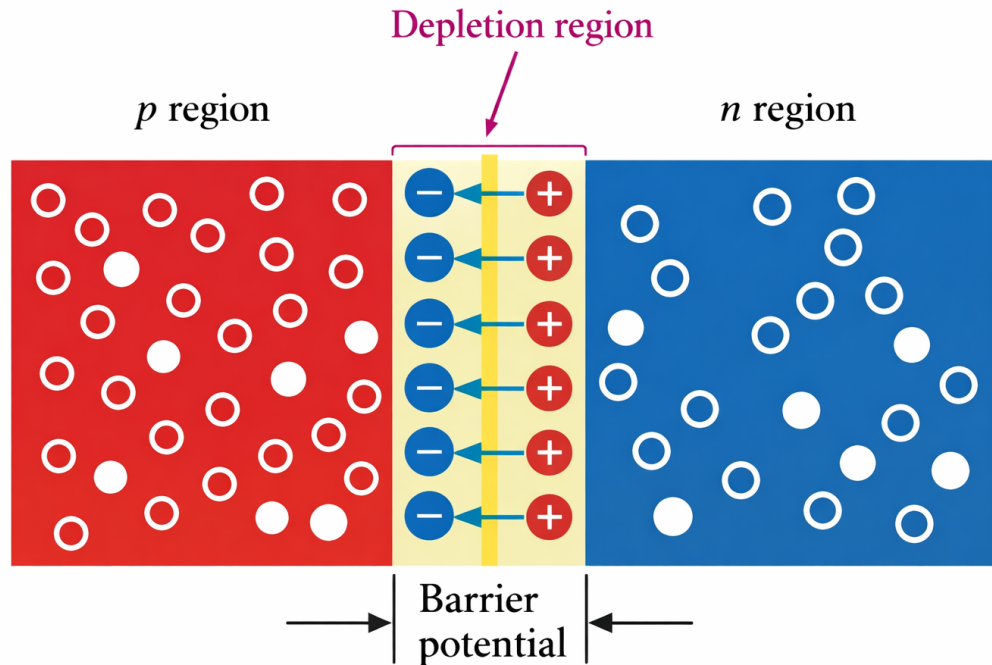


Fig. 2.5 Formation of depletion region.

### 2.3.2 Operating Principles of High-Power Diodes

High-power diodes typically operate under either forward-bias or reverse-bias conditions [137, 138]. A diode is forward biased when the anode is connected to the positive terminal and the cathode is connected to the negative terminal of the voltage source. In forward bias condition, the applied external voltage reduces the width of the depletion region, which enables charge carriers to cross the junction and begin current conduction [138]. The increase in forward current increases conduction losses and junction temperature, which makes thermal management a critical design consideration [139]. The depletion region becomes wider in the reverse bias condition, and the diode blocks the flow of current. High power diodes are specifically designed with thick drift regions and capable to carry larger reverse voltages without breakdown. However, excessive reverse voltage can cause avalanche breakdown, which may result in performance degradation and irreversible device damage.

### 2.3.3 Ideal and Practical Diode Characteristics

An ideal diode starts current conduction with zero voltage drop when forward-biased and completely blocks current conduction under reverse bias conditions as shown in Figure 2.6. However, practical diodes do not exhibit ideal behavior and real high-power diodes require to exceed a forward voltage threshold to overcome the depletion region. The threshold voltage is typically around 0.7–1.2 V for silicon devices subjected to current density and temperature [140]. Under reverse bias, a small leakage current flows due to minority carriers. The leakage current increases with an increase in temperature. When the applied reverse voltage exceeds the breakdown voltage, an avalanche effect may occur, resulting in a sharp increase in reverse current [141]. The interaction between electrical conduction and thermal behavior makes electro-thermal modeling essential for accurate prediction of diode performance and reliability under high-current and surge conditions.

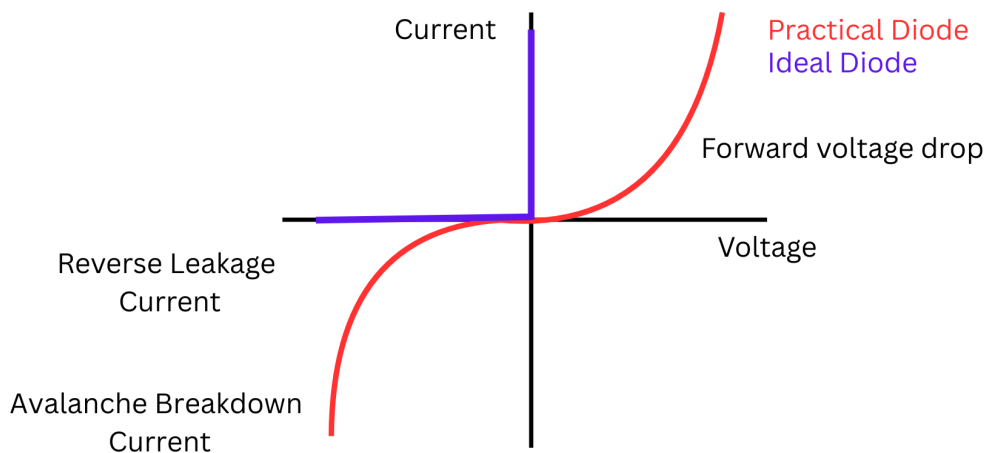


Fig. 2.6 V-I characteristics of ideal and practical diode.

## 2.4 Packaging Technologies and Device Configurations

High-power semiconductor devices have traditionally been implemented using insulated module-based architectures, as illustrated in Figure 2.7, using brazing and welding contact technology, where a semiconductor chip and multiple layers of various materials (Si, AlN, AlSiC, Copper) are connected together and to external electrodes via soldering and welding



wires. However, this packaging approach supports only low- to medium-current operation because heat ( $Q$ ) flows through a single conduction path from the chip to the heat sink before being dissipated to the ambient  $Q_w$ . This limited thermal pathway reduces reliability, and long-term operation is often compromised due to degradation mechanisms such as bonding wire lift-off and solder joint cracking, which lead to performance degradation and eventual device failure [142, 143]. With advancements in the packaging technology, PCT

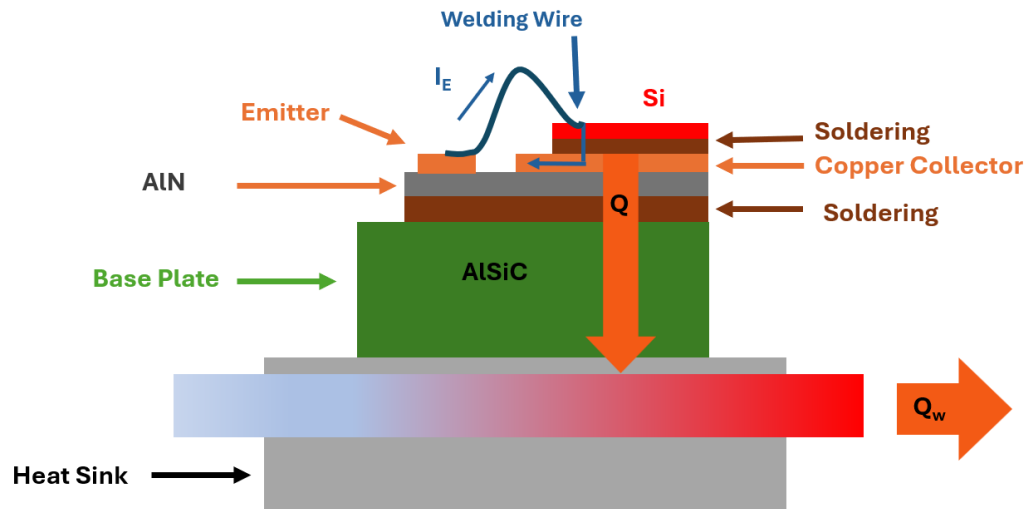


Fig. 2.7 Structure and heat-transfer mechanism of a conventional brazed and welded contact module.

has been reestablished and extended to various configurations, including insulated modules and press-pack ceramic housing assemblies as shown in Figure 2.8 and 2.9, respectively. In these devices, multiple layers are stacked together by clamping force, ensuring direct electrical and thermal contact without the need for wire bonds or solder joints. Moreover, in switching devices, such as thyristors, IGBTs, etc., the gate connections to the terminals are replaced by gate springs. The gate springs make them more reliable and robust to performance degradation and failure. The insulated module assemblies commonly employ monolithic, silicon, round-shaped diodes, and thyristors. This configuration enhances the device reliability and support medium to high current ratings while reducing the risk of failure by eliminating soldered interconnections. For applications with very high currents, the use of PCT in the press-pack ceramic housing designs further improves the reliability and thermal performance. This configuration enables two-sided cooling, supported by heat sink A and heat sink B, with corresponding heat dissipation paths as depicted in Figure 2.9. However, increased current levels  $I_T$  from anode (A) to cathode (K) beyond the limits can make all these packaging configurations susceptible to failures such as fretting damage, micro-eroding,

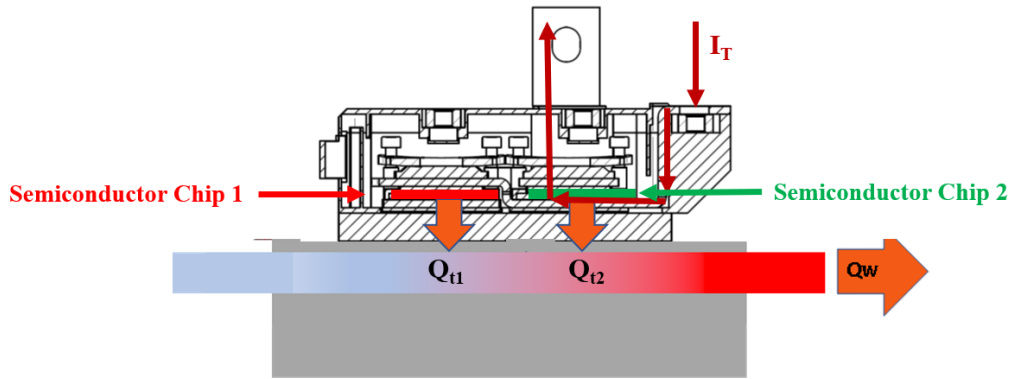


Fig. 2.8 Schematic of the structure and heat-transfer mechanisms of the PCT-insulated module.

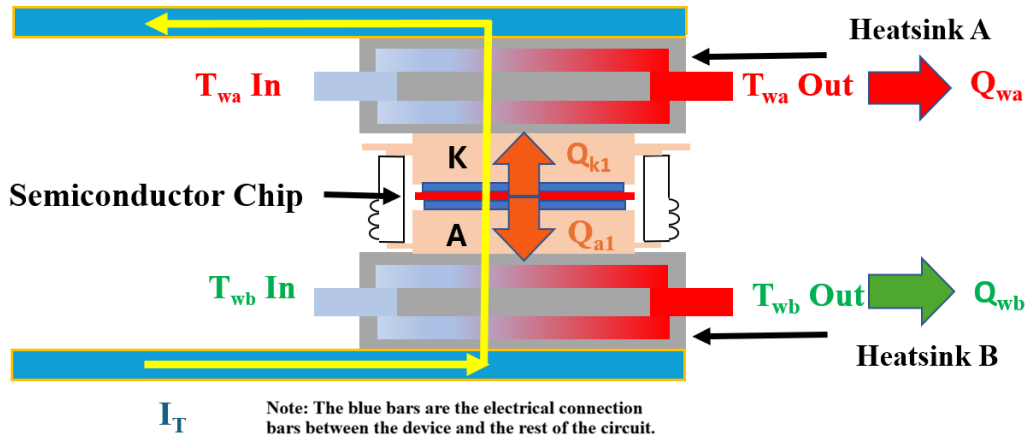


Fig. 2.9 Schematic illustration of the structure and heat-transfer mechanisms in the PCT press pack diode.

and spring fatigue. Additionally, press-pack devices lack encapsulation, decreasing the risk of chip rupture and explosion under fault conditions. The failures are primarily driven by excessive junction temperatures caused by surge currents and thermal cycling, inducing thermo-mechanical stresses that ultimately compromise device reliability [144].

## 2.5 Thermal Modeling and Junction Temperature Estimation Techniques

Power dissipation and thermal management are considered critical challenges in the design and operation of high-power semiconductor devices [145]. Consequently, significant attention

has been given to develop techniques that manage the device temperature and operate it in an acceptable operating range. However, to ensure efficient thermal management and improve performance and reliability of the device, precise evaluation of the device's junction temperature is required [146]. Since direct measurement of the junction temperature is difficult and requires complex equipment or becomes impractical in some scenarios, various approaches have been developed to estimate it under different operating conditions. These approaches are typically divided into two major categories: measurement-based methods and simulation-based methods. These methods are further divided into subcategories as illustrated in Figure 2.10 and detailed in subsequent sections.

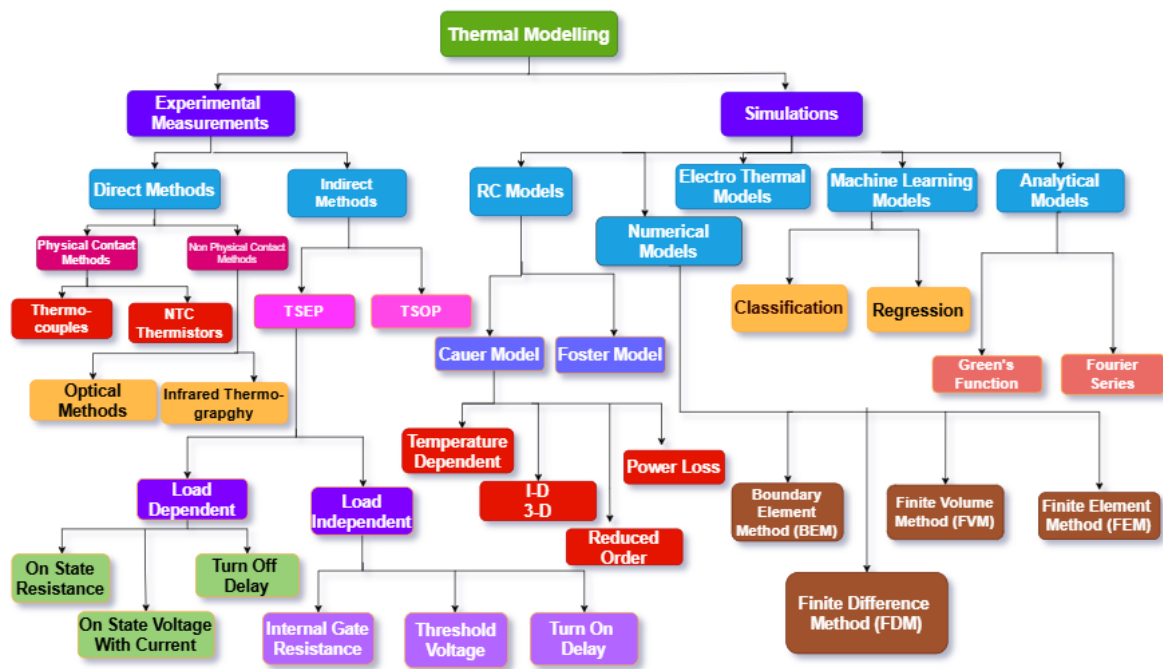


Fig. 2.10 Some notable techniques for temperature evaluation of high-power semiconductor devices.

### 2.5.1 Measurements-based Studies

The actual heat transfer and thermal behavior of a power semiconductor device can be accurately measured and characterized through performing experimental measurements. A wide range of measurement methods have been developed to measure the temperature of devices under various operating conditions and power levels. Early temperature measurement approaches were predominantly based on the thermal expansion properties of materials [147, 148]; however, with advances in technology, these techniques have been improved

and complemented by more sophisticated methods that offer improved accuracy, spatial resolution, and temporal response.

Based on measurement principles, experimental temperature measurement techniques are broadly classified into direct and indirect methods. Direct methods aim to measure temperature through physical contact or optical interaction with the device, whereas indirect methods measure junction temperature from temperature-dependent electrical or optical parameters. This classification forms the foundation of modern experimental thermal characterization and provides guidelines for the selection of appropriate techniques for both offline characterization and online monitoring applications. [85, 149].

### 2.5.1.1 Direct Measurements

Direct temperature measurement methods emerged after the invention of liquid-in-glass thermometers with the development of thermocouples, which enable precise thermal assessment through direct contact between the semiconductor die and the sensing element [150], reducing measurement errors [151], including environmental factors. A wide variety of physical-contact and non-physical-contact direct measurement techniques have been implemented in semiconductor materials, leading to the development of more technical and advanced devices acting as thermometers or temperature transducers to enable precise temperature monitoring and estimation.

**2.5.1.1.1 Physical Contact Methods** Physical contact methods measure the temperature of a device by placing a sensor in close proximity to the semiconductor die or package surface. Generally, thermocouples and resistive temperature sensors [150] are used for measurements. These methods can provide high accuracy under controlled conditions; however, they usually require opening the package or modifying the module, which can introduce safety concerns and mechanical risk [152].

**A Thermocouples** The working principle of thermocouples is based on the Seebeck effect, which deals with electromagnetic effects in the circuit of metal conductors when two different metals are connected. A difference in temperature between the two contacts can form a thermal potential in the closed circuit [153], which can be measured to estimate the temperature. The temperature measured by thermocouple is determined by contact location. The measured temperature becomes uncertain because of the temperature distribution with a gradient on the module surface. However, the sensing point of the thermocouple is often not sufficiently thermally insulated against the heatsink. The thermocouple may be cooled from the wire and heatsink, thus reducing the case temperature. Moreover, the clamping pressure

applied to press the module against the heatsink varies during the test, which may change the contact between the thermocouple and the case, thus changing the sensing temperature. Finally, there is no electrical insulation between the thermocouple and the heatsink.

Conventional thermocouples are constructed from two dissimilar metallic wires (e.g., Type K [154, 155], N, S, or R) and have long served as reliable sensors due to their simplicity, durability, and broad temperature ranging from  $-200\text{ }^{\circ}\text{C}$  to  $2000\text{ }^{\circ}\text{C}$  [156]. Among traditional thermocouples, Type J (Iron–Constantan) was employed in semiconductor thermal testing due to its moderate sensitivity. These devices operate across a wide range of temperature ranging from  $0\text{ }^{\circ}\text{C}$  to  $750\text{ }^{\circ}\text{C}$ . However, the iron component is prone to oxidation, which compromise long term accuracy in humid or high-temperature conditions. In contrast, Type K (Chromel–Alumel) has emerged as the predominant choice in power semiconductor thermal monitoring by offering a higher temperature range ( $-200\text{ }^{\circ}\text{C}$  to  $+1250\text{ }^{\circ}\text{C}$ ), fast dynamic response, and cost-effectiveness. It is typically implemented using fine-gauge wire (e.g., 36 AWG) with bare bead or welded junctions directly affixed to device cases or heat spreaders. However, the performance of the thermocouple along the time may be degraded, hence calibration are required to maintain the quality [157]. In this case, Type N are more stable at high temperatures for longer periods [158].

**B Negative Temperature Coefficient Thermistors(NTC)** Negative Temperature Coefficient (NTC) thermistors are based on the principle that their electrical resistivity decreases with increasing temperature [159, 160]. The concept traces back to Faraday’s discovery in 1833, where the resistivity of  $\text{Ag}_2\text{S}$  was observed to decrease with temperature [159]. Which later evolved into early implementations by including materials like  $\text{Cu}_2\text{O}$ ,  $\text{Cu}_2\text{S}$ , and  $\text{UO}_2$ , which were positioned on heat sinks or module casings to approximate case temperatures ( $T_c$ ) in power modules. While useful, they only offer delayed and spatially averaged estimates of the actual junction temperature, thus making it unsuitable for the fast-switching, high-density packaging demands of modern SiC and GaN devices. To address these limitations, high-temperature ceramic-based NTC thermistors have been directly integrated into power modules. The inclusion of these devices enhance the development of diverse structural categories, including spinel-type, perovskite-type, pyrochlore, and ceramic-polymer composites. Among these devices, spinel ( $\text{AB}_2\text{O}_4$ ) and perovskite ( $\text{ABO}_3$ ) structured ceramics are used in applications, where high temperature measurements are required. However, physical contact sensors suffer from limited temporal resolution and spatial averaging effects, particularly in high-power density devices, where strong temperature gradients exist. Heat conduction along sensor wires and contact pressure variability also distort the measured temperature,

making these techniques unsuitable for accurate junction temperature estimation in practical power modules [161].

**2.5.1.1.2 Non-Physical Contact Methods** Non-contact techniques measure temperature without mechanical interaction with the device, primarily using optical or electromagnetic principles. Infrared (IR) thermography is the most widely adopted non-contact approach and has been extensively applied for surface temperature mapping in power devices [162].

**A Infrared Thermography** Infrared thermography is a non-contact temperature measurement technique that employs an infrared camera to capture the thermal radiation emitted by the DUT and subsequently extract the junction temperature. This method introduces minimal electrical interference with the DUT and therefore has limited impact on circuit operation [163]. However, the accuracy of infrared thermography is strongly dependent on the surface emissivity of the DUT and on the appropriate selection of the camera integration time, both of which must be carefully calibrated within the relevant temperature range [164, 165]. Similar to other direct physical measurement techniques, IR thermography typically requires modification of the device packaging. The modifications include partial package removal and the elimination of dielectric gel layers, in order to gain optical access to the semiconductor surface [166, 167]. To further improve measurement accuracy, the exposed surface of DUT is often coated with a high-emissivity material in order to reduce emissivity-related uncertainty. This approach enables high spatial resolution and detailed thermal mapping, however, the relatively low frame rate of most infrared cameras limits temporal resolution, resulting in slow response times and reduced suitability for fast transient measurements. Consequently, despite its advantage in spatial characterization, IR thermography is generally employed as an offline diagnostic or validation tool rather than for real-time junction temperature monitoring. It is most commonly used to validate junction temperature extraction techniques and thermal models rather than as a primary method for online temperature estimation. However, non-contact methods remain limited by surface emissivity uncertainty, encapsulation attenuation, and lack of direct access to the active junction region. Consequently, their applicability is restricted to offline diagnostics and model validation rather than embedded or real-time temperature monitoring [168].

### 2.5.1.2 Indirect Measurement Methods

Indirect junction temperature estimation methods measure the device junction temperature from electrical or optical parameters that exhibit a predictable dependence on temperature. These parameters, commonly referred to as temperature-sensitive electrical parameters

(TSEPs) or temperature-sensitive optical parameters (TSOPs), form the basis of most practical junction temperature monitoring techniques due to their non-intrusive nature and compatibility with online operation. In power electronic systems where direct temperature sensing is impractical, TSEP-based approaches offer an optimal alternative between accuracy [169], implementation complexity, and real-time capability.

TSEP-based methods estimate junction temperature by correlating variations in selected electrical parameters with temperature through prior calibration. Typical TSEPs include on-state voltage, on-state resistance, threshold voltage, saturation current, switching delay times, and internal gate resistance. Despite their frequent use, all TSEP-based techniques shared a fundamental challenge of maintaining stability between the relationship of parameter and temperature. The ambiguity in this relationship may be introduced by various factors, including packaging parasitics, variations in operating conditions, and progressive device aging, highlighting the need for precise calibration and compensation mechanisms to maintain accuracy over the device lifetime. Among the available TSEPs, the on-state voltage drop is one of the most extensively used owing to its approximately linear dependence on junction temperature [170–173]. High-current injection methods extract the voltage drop during normal conduction [174, 175], but self-heating and switching interference complicate accurate temperature estimation under realistic operating conditions [176]. Low-current injection techniques minimize these effects by reducing power dissipation during measurement and improving stability of calibration in application of diodes and IGBTs [177, 85]. However, despite their relative simplicity, on-state voltage-based methods remain sensitive to performance degradation. Moreover, changes that occur in contact resistance and metallization due to device aging also alter the voltage–temperature relationship, which results in estimation errors if not explicitly accommodated [86].

On-state resistance is another important TSEP technique, exhibiting a monotonic increase with temperature and finding widespread application in MOSFETs and IGBTs [178, 179]. Although its temperature dependence is well defined, precise and synchronized voltage and current measurements for accurate extraction are required [180]. In transient or higher surge currents, substantial errors can occur due to measurement noise, limited bandwidth, and timing mismatches between sensing channels. To minimize the error, several studies have proposed noise-robust estimation techniques and time-skew compensation strategies to improve accuracy [181, 182]. Moreover, inherent coupling between thermal effects and aging-induced resistance increase, which complicates the separation of temperature variation from long-term degradation, also limits the reliability of resistance-based methods [183]. Threshold voltage represents another popular TSEP due to its good linearity and sensitivity [184–186] and ability to not be affected by the device operating conditions. It



can be employed as integrated monitoring, which makes it suitable for embedded power electronics [187, 188]. However, the relatively low temperature sensitivity, complexity in online measurement, and threshold voltage drift problem in some applications limit applicability [187, 189]. Moreover, it is susceptible to switching noise and parasitic coupling in fast-switching devices [188]. Furthermore, bias stress and aging mechanisms induce permanent threshold voltage shifts, which require adaptive calibration strategies or the fusion of multiple parameters to preserve estimation accuracy in long-term operation.

Saturation current-based temperature estimation is another popular TSEP technique that utilizes the temperature dependence of carrier mobility. This technique results in fast temporal response and has minimal circuit intrusion, but high-resolution current sensing and careful mitigation of parasitic capacitance effects is required. Several studies are conducted that incorporate neural-network-assisted calibration frameworks to address sensitivity to operating point variation and aging. Nevertheless, these models rely on device-specific training data, and vulnerability to measurement noise remains a key challenge. Dynamic TSEPs are a widely used technique that is derived from switching behavior, such as turn-on and turn-off delay times [190, 191], and provide additional temperature-dependent indicators. Turn-on delay generally exhibits weak temperature sensitivity and strong dependence on current and gate-drive conditions, limiting its practical usefulness [192, 193]. In contrast, turn-off delay has preferred in most applications due to its higher temperature sensitivity [194]. However, the sensitivity is reduced in wide-bandgap devices, highlighting the need for high-resolution timing circuitry or sensitivity enhancement techniques. Moreover, the increasing gate resistance can also improve temperature sensitivity, but it degrades switching performance, which motivates the development of circuit-level solutions that enhance sensitivity without compromising dynamic behavior.

Recently, internal gate resistance has become known as a promising TSEP due to its prominent temperature dependence and practical suitability for online monitoring [195]. Measurement methodologies utilizing gate current analysis [196, 197], signal injection, and off-state sensing have exhibited significant accuracy without the need for any additional sensors to measure temperature. Regardless of these advantages, the extraction of internal gate resistance is highly sensitive to electromagnetic interference, parasitic inductance, and blocking voltage effects, especially in rapid-switching SiC and GaN devices. Recent studies have focused to propose calibration techniques and ML models to overcome these limitations, resulting in high accuracy and robustness. These advancements highlight the importance of data-driven methodologies to encounter challenges in traditional TSEP-based junction temperature estimation techniques.



### 2.5.1.3 Limitations of Measurement-Based Approaches

Despite significant research in this area, measurement-based estimation of junction temperature encounters basic limitations. The non-uniform temperature distribution throughout the semiconductor die results in spatial ambiguity, while aging affects the temperature sensitivity of electrical parameters over time [14]. Moreover, the implementation complexity is also increased by the varying characteristics between devices, which require individual calibration. Measuring junction temperature during ultra-fast switching transients is also challenging due to various factors including, limited sensor bandwidth and significant electromagnetic interference. These challenges demand a combination of measurement methodologies with adaptive thermal modeling frameworks and ML models, as discussed in the following sections.

## 2.5.2 Simulation-based Studies

### 2.5.2.1 RC Thermal Networks

RC thermal networks are mostly utilized to predict junction temperatures or the temperature of critical locations in the power modules for electrothermal design, thermal management, reliability, and lifetime prediction [198–201]. The models were constructed using either Cauer thermal models or Foster thermal models. Moreover, mathematical models have also been proposed that can transform these networks into to each other. [202, 203].

**2.5.2.1.1 Cauer Thermal Modeling** Thermal modeling of power semiconductor devices has evolved from simple RC lumped networks to multilayered electrothermal networks. Among these, the Cauer-type thermal network as shown in Figure 2.11 is prominent due to its direct correspondence with device structure, where each RC pair represents a physical material layer, enabling physically interpretable and accurate heat-flow modeling [202, 204–206]. Traditional one-dimensional (1-D) Cauer models, though computationally efficient, assume constant thermal parameters and fail to capture multidimensional heat spreading under high power densities. In these models, the case temperature of a power module is often used as the reference for calculating junction temperature. To improve accuracy, 2-D [207, 208] and 3-D Cauer networks have been developed to model inter-chip and inter-module coupling effects, but at the expense of increased model order and computational complexity [209–212]. In order to reduce the model order and minimize the computational burden, including both time and resources, research has focused on order reduction [213–216], thermal parameter extraction optimization [217–220], and simplifying power loss calculation [221–223]. Among them, the authors in [213] proposed a junction temperature simulation model based on a reduced-order decoupling method for multi chip power module. In this model, only the steady-state

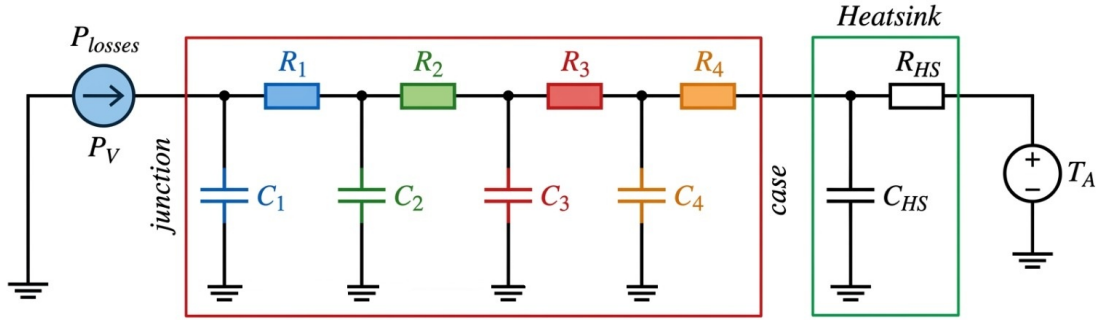


Fig. 2.11 Cauer type thermal network corresponding to the device structure.

information of few RC parameters was required, and thus, the parameter extraction efficiency was enhanced. Following that, a reduced-order thermal observer of power module was presented in [214], which allows to provide a real-time accurate estimation of junction temperature even under complex transient conditions. Additionally, in [217], a novel 3-D physical RC network model was proposed for IGBT modules in which the effects of junction temperature variations were fully considered. An enhancement of this thermal network model (TNM) is the use of the novel RC parameters extraction method, which is able to simplify the modeling process because the temperature responses are not required. In [220], an RC parameter extraction method based on the equivalent heat flow paths was reported, which avoids the extraction of thermal transient curves and the thermal impedance matrix, leading to a low computational cost. Meanwhile, one interesting method simplifying the complexity of the TNM via artificial neural network (ANN) for power modules was presented in [223]. Parameter extraction methods include analytical, time-constant, structure-function. Additionally, empirical curve fitting [204–206] offer simplicity but limited physical relevance. in order to improve the physical accuracy finite element method (FEM) assisted techniques became a prior choice, providing geometry based RC parameters [209, 218, 221, 224]. Moreover, recent works also integrate optimization algorithms (e.g., level-based learning swarm optimization and sequential quadratic programming (LLSO–SQP) [212] within FEM frameworks to achieve accurate, high-dimensional parameter identification. Novel 3-D physical RC models for IGBT modules [217] further include junction-temperature effects and eliminate the need for thermal response measurements. Despite significant progress, most existing thermal network models still assume constant boundary conditions and material properties, limiting their predictive accuracy under dynamic operating environments.

**2.5.2.1.2 Foster Thermal Modeling** Foster thermal networks have been employed for compact thermal modeling of power semiconductor devices due to their mathematical simplicity, empirical accuracy, and straightforward integration with circuit-level simulators such as SPICE and PLECS. In contrast to Cauer networks, Foster models represent thermal behavior through a series of lumped RC elements obtained by curve fitting of the device's transient thermal impedance. Thermal impedance is typically derived from datasheets or experimental step-response measurements. Early Foster models were widely adopted because of their

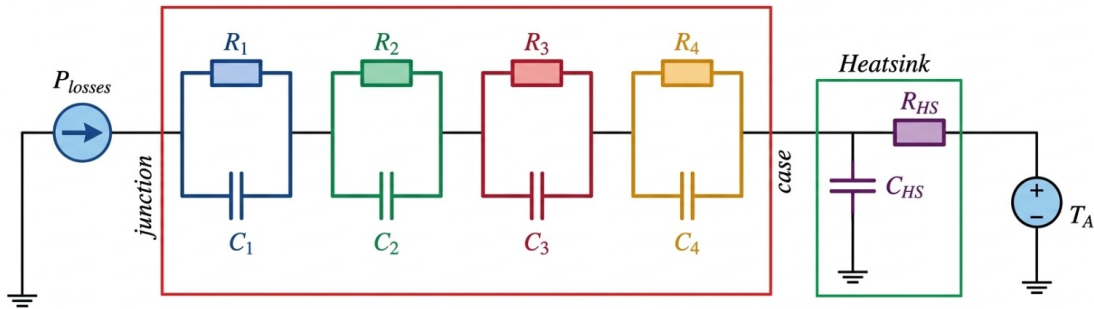


Fig. 2.12 Equivalent circuit schematic of a Foster thermal network.

low computational cost and ease of parameter identification. For example, datasheet-based fitting methods have been used to establish low-order Foster networks for Si and SiC devices. This enables rapid junction temperature estimation in circuit simulations [225]. However, a fundamental limitation of the Foster representation is the lack of direct physical meaning and strong dependence on the reference boundary conditions. Consequently, junction temperature predictions in traditional Foster models vary synchronously with changes in the reference temperature. This introduces substantial errors when cooling conditions or ambient environments deviate from those assumed during parameter extraction [226–228]. This limitation becomes critical under transient and surge operating conditions where thermal paths and boundary conditions vary dynamically. To improve physical interpretability, several studies have proposed mathematical transformations from Foster to Cauer networks [202, 203]. These approaches aim to map empirically fitted RC elements onto physically meaningful layers. However, such transformations partially address the lack of physical correspondence, result in high-order networks, and do not adequately capture outward heat flow or nonlinear boundary effects. FEM-assisted parameter extraction has further improved Foster modeling fidelity by enabling multi-node impedance identification across device layers [229, 230]. These approaches incorporate self- and cross-heating effects and achieve improved estimation results that closely agree with TSEP measurements. Nevertheless, their

accuracy remains sensitive to thermal interface conditions, power distribution, and chip spacing, which limit their robustness under varying operating conditions. Recent research has revisited Foster modeling from a frequency-domain perspective to overcome inherent time-domain limitations. In [231], the thermal impedance was analyzed using Bode plots, revealing that conventional Foster networks fail to capture long-term thermal dynamics associated with heat sinks and interface materials. By introducing a frequency-domain thermal transfer function, this approach enables improved modeling of thermal delay and energy storage along the heat-flow path, addressing a key weakness of datasheet-based Foster models. Further advancements have focused on modular and boundary-aware Foster formulations. Case-referenced Foster models partition the thermal path into junction-to-case, case-to-heatsink, and heatsink-to-ambient components, allowing the internal device model to be reused across different cooling configurations [227]. This modularization significantly improves scalability in system-level electro-thermal simulations. In parallel, nonlinear Foster models have been developed in which thermal resistance and capacitance are expressed as functions of temperature or heat-transfer coefficients, enabling adaptation to varying cooling intensities and boundary conditions [232, 233]. More recent studies have also explored incorporating aging and degradation effects into Foster networks. Parameter drift associated with solder fatigue, thermal grease degradation, and substrate delamination has been linked to changes in thermal impedance over time [234, 126]. While these models improve life-time estimation, they typically rely on pre-defined degradation scenarios and fixed network structures, limiting their predictive capability for early-stage failure detection.

Overall, modern Foster-based thermal modeling has evolved beyond its original empirical formulation through frequency-domain analysis, FEM-informed parameter extraction, modularization, and nonlinear boundary adaptation. Despite these improvements, Foster networks remain inherently behavior-oriented rather than structure-oriented, making them less suitable for detailed device-level thermal analysis under extreme transient conditions. As a result, Foster models are best suited for fast system-level simulations and preliminary thermal assessment, while physically interpretable Cauer-based and hybrid electro-thermal models are increasingly favored for surge analysis, packaging evaluation, and reliability-oriented design.

**2.5.2.1.3 Comparative Analysis of Cauer and Foster Thermal Networks** A comparative analysis of Foster and Cauer thermal network models reflects their critical roles in electrothermal modeling. The Foster network offers a mathematically compact and behavior-oriented modeling, which is ideal for system-level simulations as well as fast transient fitting. In contrast, the Cauer network offers a physically interpretable and structure-oriented

formulation, where each RC element corresponds to a material or interface, enabling accurate device-level heat-flow representation. Moreover, Foster models primarily depends on curve fitting and multi-node parameter, however, Cauer thermal models focus to extract parameter from device dimensions and material and preserve geometric accuracy. Recent improvements have made Foster models suitable for aging and online estimation, whereas Cauer frameworks stands out for real-time RC adaptation and temperature-dependent analysis. Foster networks also used neural network-based fitting, whereas Cauer models prefer physics-informed AI coupling that retains physical consistency. Collectively, Foster models emphasize computational efficiency, while Cauer models prioritize physical accuracy and adaptability.

### 2.5.2.2 Electro-Thermal Coupled Models

Electro-thermal coupled models integrate both electrical and thermal models together through bidirectional interaction between temperature and power dissipation. In these models, electrical operation generates power losses, acting as thermal sources, while the resulting temperature rise feeds back to modify TSEP. Such coupling allows device behavior to be simulated within circuit-based environments, including Saber, PSpice, PLECS, and Simulink. This makes electro-thermal modeling a widely adopted approach to analyze power semiconductor devices under realistic operating conditions [235, 236]. Electrical sub-models, typically derived from semiconductor physics, are capable of resolving fast switching phenomena at microsecond or nanosecond time scales, whereas thermal behavior is commonly represented using compact RC networks based on the thermoelectric analogy [237, 238]. This formulation enables efficient co-simulation of electrical performance and temperature evolution in system-level tools.

Finite-element-based electro-thermal models extend this concept by resolving spatial temperature distributions and nonlinear material behavior with high fidelity. In such approaches, FEM-derived thermal behavior is often reduced to equivalent Foster or Cauer thermal networks for integration with electrical solvers [239, 240]. These models have been extensively applied to investigate reliability-relevant phenomena such as short-circuit events, solder fatigue, and bond-wire degradation. However, most FEM-assisted electro-thermal models rely on averaged power-loss inputs obtained from circuit simulators, which limits their ability to capture localized temperature gradients arising from non-uniform current density, metallization geometry, or packaging defects. However, most FEM-assisted electro-thermal models rely on averaged power-loss inputs obtained from circuit simulators. This limits their ability to capture localized temperature gradients arising from non-uniform current density, metallization, or packaging defects. Moreover, spatially resolved conduction loss modeling

has been reported in the literature, but local modeling of both conduction and switching losses remains limited, particularly under high transient surge current conditions. To overcome this limitation, [241] proposed a fully coupled three-dimensional electro-thermal FEM model of an IGBT, incorporating nonlinear forward characteristics and spatially resolved current-density-based loss calculations. The model significantly improves the prediction of hot-spot temperatures by distinguishing averaged and local loss formulations. This approach was further extended in [242] to chip-level analysis, accounting for uneven current distribution and intra-chip thermal coupling. Similarly, unified electro-thermal formulations based on compensation theory have been implemented in circuit simulators [243], though many of these approaches still assume uniform temperature distributions or rely on empirically calibrated parameters, limiting their applicability for strongly localized heating and multi-chip interaction effects. The nonlinear dependence of electrical and thermal parameters on junction temperature has been investigated in several studies [244, 245], while experimental validation under varying switching frequencies, load currents, and ambient conditions has confirmed the capability of electro-thermal models to reproduce dynamic device behavior [246]. Die-level thermal coupling has been explicitly quantified using influence-coefficient matrix approaches for liquid-cooled modules [247]. However, these models often require re-identification when cooling conditions change. To overcome this limitation, case-referenced formulations have been proposed that decouple internal module thermal impedance from external cooling conditions, enabling greater model reuse across operating environments [227]. Although RC-based electro-thermal models offer computational efficiency and ease of implementation, their spatial resolution is inherently limited by the number of thermal nodes, resulting in discontinuous temperature fields. Consequently, they are well suited for junction or regional temperature estimation but are insufficient for detailed stress analysis or deformation studies that require coupling with mechanical fields [224]. This limitation has motivated the development of fully coupled electro-thermal-mechanical FEM models. These models resolve three-dimensional heat flow, thermo-mechanical stress, and material degradation mechanisms within power modules [248]. These models provide valuable insight for packaging design and failure analysis; however, they often replace detailed electrical behavior with simplified power-loss models, preventing accurate prediction of voltage-current characteristics during transient operation.

Recently, a number of studies are conducted that focused on improving physical accuracy and computational efficiency through multi-time-scale and reduced-order electro thermal models. These studies results in reducing simulation time without compromising accuracy by exploiting the separation between fast electrical dynamics and delayed thermal responses. For example, in [249] a multi-time-scale electro-thermal model is proposed that combines FEM-



based thermal analysis with Proper Orthogonal Decomposition (POD). The model predicts accurate junction temperature estimation under varying operating conditions. Similarly, reduced-order and Linear Time-Invariant (LTI) identification techniques are also employed to reduce computational costs while maintaining temperature prediction accuracy of more than 95% [250]. Although, these approaches achieved higher efficiencies, however, they require precise calibration and manufacturer datasets. Building on these developments, hybrid and AI-enhanced electro-thermal models have been developed, combining physics-based formulations with data-driven learning. ANNs have been trained on high-fidelity FEM data to rapidly estimate electro-thermal stresses and transient junction temperatures with high accuracy [251, 252]. These hybrid models results good performance over purely physics-based solvers, though their generalization capability remains limited by training data and device specificity. As a result, there is growing interest in physics-informed neural networks that embed physical constraints into learning architectures to improve robustness and interpretability. The scope of electro-thermal modeling has also expanded to encompass reliability and aging analysis through fully coupled electro-thermo-mechanical frameworks. The impact of bond-wire lift-off, solder fatigue, and contact degradation on thermal and stress distributions are also investigated in the literature [253, 254]. While these approaches provide deep physical insight, their high computational cost currently restricts their applicability to offline analysis rather than real-time monitoring or control.

In general, electro-thermal coupled modeling has transformed from simple circuit-based models to highly accurate multiphysics and hybrid models. Despite significant progress has been recorded, there are still some substantial issues to be addressed. In particular, validation procedures are not standardized appropriately, degradation effects are not captured adequately in compact models, as well as need of flexible models that can handle high transient surge currents. To address these challenges, it's essential to develop physics-informed, reduced-order electro-thermal models that maintain accuracy, can adapt to changing boundary conditions, and are still fast enough for system-level and reliability-focused applications.

### 2.5.2.3 Numerical Methods

Numerical modeling has been widely used to analyze various characteristics of high power semiconductor devices such as electrical, thermal, and mechanical by solving the governing partial differential equations of heat conduction. Generally, FEM, Finite Difference Method (FDM), and Finite Volume Method (FVM) techniques are employed, which are capable to predict temperature distributions with high accuracy, particularly in scenarios with complex geometries and thermally coupled multi-chip devices [96, 255]. These models are used to perform multiphysics analysis, evaluate heat transfer, thermo-mechanical stress, and material

level interactions to improve heat dissipation and reliability in high-power devices [256]. Among these techniques, FEM has emerged as the dominant numerical approach due to its flexibility in handling nonlinear material properties, complex packaging structures, and coupled electrical–thermal–mechanical fields. Commercial FEM solvers such as COMSOL Multiphysics [257], ANSYS, and TCAD are mostly employed in the development of device as well as package models, allowing precise evaluation of thermal behavior and mechanical deformation under various operating conditions. Moreover, FEM-based simulations also provide high spatial resolution and detailed internal temperature information [258], which is critical for analyzing failure and degradation mechanisms [142]. For instance, [259] employed FEM to evaluate chip temperature and variations across solder layers considering different levels of degradation. Moreover, in [260] changes in temperature and stress concentrations at bond-wire contact regions are investigated. Apart from this, numerical methods are also applied in the thermal and packaging design of IGBT modules to reduce experimental tests, faster development cycles, and lower design costs [261, 262].

In order to enhance computational efficiency, FEM has been combined with compact thermal-resistance networks, enabling rapid evaluation of nodal temperatures while retaining the accuracy of spatially resolved simulations. These hybrid approaches enable FEM to extract thermal parameters, which are then embedded into circuit-equivalent thermal networks to efficiently capture cross-thermal coupling effects in multi-chip devices [211, 263]. This strategy results in simulation time reduction without disturbing the accuracy of electro-thermal analysis. Moreover, a number of studies have employed numerical methods to construct thermal impedance matrices for power devices, accommodating self-heating and thermal coupling effects in IGBT modules [264]. Subsequent, later studies refined these models by correcting thermal diffusion angles and modifying impedance matrices to reflect solder-layer aging and evolving coupling behavior [265]. Furthermore, compensation strategies have also been proposed to account for aging-induced, increase in casing thermal resistance, due to degradation of thermal interface materials such as thermal grease [266]. Other studies investigate thermal coupling behavior under aged thermal grease conditions. However, many of these studies assume ambient or heat-sink temperature as a fixed reference node. This assumption simplify the analysis and restricts applicability when external boundary conditions vary significantly [227]. Moreover, the authors in [267] proposed a FEM-based model to investigate the influence of thermal grease aging on thermal coupling in IGBT modules. In this work the relationship between grease degradation, heat conduction area, and effective heat transfer area are analyzed. Despite these advances, two fundamental limitations persist in numerical thermal coupling analysis of power devices. First, external cooling systems are typically represented by effective heat transfer coefficients,



which are difficult to accurately determine under varying cooling conditions and are not well suited for modeling progressive cooling degradation, such as thermal grease aging. Second, computationally FEM simulations are intensive to analyze transient thermal behavior over long mission profiles, which are not suitable for long-duration simulations [268]. Overall, numerical methods, especially FEM provide unmatched accuracy and physical insight for analyzing temperature distribution, thermal coupling, and degradation mechanisms in high-power semiconductor devices. However, their high computational cost and sensitivity to boundary-condition assumptions limit their applicability for real-time analysis, long-term mission profile simulation, and iterative design optimization. These limitations encourage the use of numerical methods with reduced-order models and data-driven techniques in order to achieve a balance between accuracy and computational efficiency.

## 2.6 Machine Learning Applications in Power Electronics

ML techniques primarily rely on data-driven models trained on specific scenarios, eliminating the need to manually formulate complex analytical expressions and compute design parameters. These models possess self-learning capabilities, achieving high accuracy even with larger datasets while maintaining computational efficiency. ML can be broadly categorized into supervised and unsupervised learning. Supervised learning is used to develop models in which predictions are made based on both input and output data, enabling accurate forecasting. It can be further divided into classification and regression; classification assigns data to predefined categories, while regression predicts numerical values based on previous data patterns. These models are widely employed in power electronics and semiconductor applications, transforming processes from design and manufacturing to testing and optimization [269, 270]. Recent studies have demonstrated the effectiveness of ML techniques in modeling [271], prediction [270], and fault diagnosis of IGBTs and power electronic devices [272]. In [273], junction temperature and device degradation were estimated by predicting the on-state voltage using k-nearest neighbor (kNN), support vector machines (SVM), and decision tree (DT) models. ML approaches have also been applied to predict the lifetime of IGBT modules, achieving higher accuracy than conventional lifetime models [96]. Data-driven convolutional neural network (CNN) methods have enabled reliable classification of IGBT failure modes under varying operating conditions, highlighting their potential for condition monitoring and predictive maintenance [274]. Furthermore, [275] proposed a hybrid approach combining compact device models with ANNs to predict IGBT output characteristics, obtaining Hefner static model parameters such as  $V_{Gate}$  and  $V_{Anode}$  from structural parameters. Comparative evaluations of ML algorithms, including random forest, backpropagation neural networks,

and decision trees, have also been conducted for fault diagnosis of power electronic devices in converter systems, demonstrating their applicability across different operational scenarios [276].

In addition, they have been applied to lifetime estimation [96–98], condition monitoring and fault diagnostics [96, 99, 100], and performance prediction [101, 102, 277]. In [278], the remaining useful life of insulated gate bipolar transistors (IGBTs) was directly estimated using various ML models, followed by a comparative performance analysis. In [99], a method is proposed for early degradation detection of bonding wires. An ensemble learning approach was employed for state classification of the extracted features. Moreover, to improve the accuracy of random forest model classification, cross-validation and particle swarm optimization were also used in this study. Furthermore, in [104], ML is integrated with finite element analysis to estimate the equivalent resistivity and thermal conductivity of semiconductor chips under various operating conditions with improved accuracy. The authors in [105] investigated chip-level thermal mapping and the prediction of temperature change rates using a ML-based neural network model. Similarly, [279] proposed a model for IGBTs that employs ML algorithms, including linear regression, SVM, and random forest, to estimate junction temperature by using collector–emitter voltage ( $V_{CE}$ ) and collector current ( $I_C$ ) as input features.

## 2.7 Gap Analysis

Since high-power semiconductor devices, especially high-power diodes and thyristors, are designed to operate in critical power electronic applications such as HVDC transmission systems, traction drives, and industrial converters, their reliable operation under high electrical and thermal stress conditions has become significantly important. In particular, transient events such as surge currents may induce excessive power dissipation and rapid junction temperature rise, which can degrade device performance and lead to catastrophic failure. Hence, it is required to characterize device electrical and thermal behavior and evaluate junction temperature under transient and surge operating conditions. Numerous studies have been reported in the existing literature that had focused on thermal modeling, forward voltage drop, and junction temperature estimation of power semiconductor devices. However, most of these studies depend on steady-state thermal resistance, the isothermal assumption, or simplified transient models derived from static electrical characteristics and reliance on experimental tests. Such assumptions may result in inaccurate voltage and temperature prediction and can compromise the safety of the device during high-current surge events, where thermal capacitance and dynamic heat flow play a dominant role. Consequently, these

approaches may either underestimate the actual voltage drop and junction temperature or lead to overly conservative designs and may increase the risk of device safety and performance degradation. Although electro-thermal modeling techniques such as RC thermal networks and numerical methods have been reported in the literature, their application to surge current conditions is often limited by oversimplified and isothermal electrical models, insufficient experimental validation, and lower surge current levels. In addition, the influence of packaging technologies, particularly the comparative analysis of press-pack and insulated module configurations, both with identical specifications and power ratings, on transient thermal behavior and surge robustness has not been comprehensively investigated under high anomalous surge currents. To the best of our knowledge, a systematic comparative analysis of surge-induced junction temperature evaluation, surge handling capabilities, and failure behavior across different packaging technologies remains limited in the literature.

Furthermore, with the increasing diversity of high-power semiconductor devices, the nonlinear relationships between device geometry, electrical parameters, thermal behavior, and current-handling capability also became complex. Although ML techniques have recently been introduced in power electronics research, their application to device-level design parameters such as chip diameter and average current prediction is still not explored. Existing studies often lack physical interpretability and are rarely integrated with electro-thermal insights, thereby limiting their practical applicability for industrial design and reliability assessment.

## 2.8 Problem Formulation

As discussed earlier in Section 2.7, existing electro-thermal models reported in the literature are mostly insufficient to accurately predict the forward voltage drop and junction temperature under high surge current events. Consequently, an improved electro-thermal modeling methodology is required that accommodates transient thermal impedance, dynamic electrical and thermal behavior, and realistic packaging effects in order to enable accurate voltage and junction temperature estimation during surge events. Furthermore, the absence of data-driven predictive tools capable of linking device geometry and electrical parameters to current-handling capability highlights an additional limitation of existing design methodologies. In particular, an integrated methodology has not yet been developed that combines physics-based understanding with ML techniques to support reliable device selection, design decision-making, and performance assessment.

Therefore, this work addresses these challenges by proposing an electro-thermal and data-driven modeling framework that enables accurate characterization of transient thermal

behavior, surge current analysis and reliability, packaging-dependent performance and failure behavior, and predictive estimation of key device parameters such as chip diameter and average current. The proposed methodology is essential to enhance the reliability assessment and design of next-generation high-power semiconductor devices operating under extreme electrical and thermal stress conditions.

## 2.9 Scientific Contributions

The main contributions of this dissertation are summarized as follows.

### 1. Transient Thermal Impedance Characterization

An electro-thermal modeling framework is developed to accurately characterize transient thermal impedance in high-power press-pack semiconductor devices under high surge current levels. Moreover, thermal parameters, including thermal resistance and capacitance, are extracted, and an electrical equivalent Cauer thermal model is developed and subsequently transformed into a Foster thermal model. This contribution allows precise junction temperature estimation under transient conditions and improves thermal characterization of the device.

### 2. Surge Current Analysis and Electro-Thermal Behavior

An electro-thermal model is proposed based on rated currents and thermal simulations to accurately estimate forward voltage drop and junction temperature under high surge current conditions. A dedicated experimental setup is developed, generating a 10 ms half positive sine waveform, and a series of surge current tests are conducted, allowing direct measurement of forward voltage. The proposed model results are validated with the experimental results, while numerical simulations were also performed to further investigate thermal behavior of devices.

### 3. Impact of Packaging Technologies and Failure Behavior

A comparative analysis is performed in order to assess the surge current capability and study failure behavior in two different diode assemblies i.e, press-pack diodes and insulated module diodes. Both devices employ identical silicon chip dimensions, electrical specifications, and power ratings. Junction temperature is estimated using experimental measured current and voltages within electro-thermal simulations in PSIM. Furthermore, failure behavior and thermal limitations are systematically investigated to assess the robustness and surge current handling capability of both packaging technologies.

**4. Machine-Learning-Based Prediction and Classification of Chip Diameter**

A detailed survey is conducted for high-power thyristors commercially available in the market, and the role of chip diameter and current capacity in device performance is analyzed. Moreover, multiple ML frameworks are developed in order to predict and classify chip diameter based on electrical and thermal parameters extracted from manufacturer datasheets. The performance metrics of implemented models are also compared.

**5. Machine-Learning-Based Prediction and Classification of Average Current**

The average current capability of high-power semiconductor devices is classified and predicted by the development of multiple ML models. Moreover, Shapley Additive Explanations (SHAP) analysis is performed to quantify feature importance and enhance model interpretability. The performance of trained and tested models is evaluated with standardized performance metrics, enabling identification of optimal trade-offs between prediction accuracy, robustness, and computational efficiency.



## Chapter 3

# Transient Thermal Impedance Modeling of High-Power Press-Pack Diodes

This chapter explains the transient thermal impedance modeling of high-power press-pack diodes, enabling accurate thermal modeling and understanding of the dynamic thermal behavior of power semiconductor devices under transient operating conditions. Section 3.2 describes the physical structure and material characterization of press-pack diodes, where the internal structure of the device is examined to identify the heat transfer and thermal properties of the materials are also discussed. Section 3.3 presents the analytical calculation of thermal resistance and capacitance. Section 3.4 discuss the electro-thermal modeling framework used to represent the transient thermal behavior of the device. This section includes the development of the Cauer thermal network, which models the physical heat flow through the device layers. In addition, methods for parameter extraction are described, followed by the transformation and interpretation of the thermal model using Foster thermal networks, which are commonly used for system-level thermal analysis and manufacturer-provided data. In Section 3.5, the experimental setup is discussed, which is used to validate the proposed thermal model. Furthermore, Section 3.6 discusses the limitations of the study, and finally, Section 3.7 summarizes the main conclusions of the chapter.

### 3.1 Overview and Research Motivation

Since last few decades, power diodes have been widely used in power electronics and industrial applications due to their ability to handle high voltages and currents, including tasks like HVDC [1, 2, 280], electric vehicle fast charging [281, 282], hydrogen electrolysis, traction power supply [5], voltage regulation, conversion, and multi-level inverter [6, 7].

However, in high voltage applications, the optimization of diode design becomes crucial to ensure optimal performance and reliability. Among many other factors, including mechanical, electrical, and thermal, the risk of device failure increases significantly if the device is not properly designed to operate safely beyond a specific junction temperature [12] mainly caused by power dissipation. Hence, acquiring precise thermal characteristics of diodes is essential to accurately define their junction temperature. Transient thermal impedance is regarded as a critical thermal parameter for evaluating various characteristics of a device, including junction temperature, essential for designing an efficient thermal management system. For this purpose, both manufacturers and academic teams are introducing various tools and implementing different techniques to improve the device optimization and thermal management. Recently, Poseico S.p.A. has designed a new optimized diode in order to obtain the minimum thermal resistance. The main task to obtain this goal are:

1. Minimizing the internal thermal resistance due to contact using optimized structure between the different parts of device assembly by using very high quality surface and a good match between the two materials in contact.
2. Reducing the thickness of material with high thermal resistance to its minimum.
3. Increasing the diameter of various parts of the device.

This chapter aims to focus on studying the electro-thermal modeling of newly designed Poseico high power press pack diodes to obtain transient thermal impedance. Specifically, a diode device with a blocking voltage of 2800 V and a diameter of 46 mm is selected for the calculation of thermal parameters, including thermal resistance and thermal capacitance. These parameters are derived analytically based on the physical dimensions, geometry, and material type of the internal structure of the diode. Subsequently, an electric equivalent circuit known as the Cauer thermal network is designed in PSIM software using the derived thermal parameters. This circuit is utilized to identify the thermal impedance versus time curves. The Cauer thermal network is then transformed to Foster thermal network to extract thermal parameters such as thermal resistances,  $R_{th}$  and time constants  $\tau$ , which are commonly provided in device datasheets, and are then used to calculate the transient thermal impedance and estimate the junction temperature under various operating conditions. The data required for Foster thermal model is extracted from thermal impedance versus time curve in MATLAB® through curve fitting based on non-linear regression. This data is then employed to design a RC thermal network of the equivalent circuit for calculating the transient thermal impedance. Utilizing the resistance and time constant values derived from this curve, it becomes possible to predict the average current that a device can safely handle



under various pulse durations and pulse shapes. The simulated thermal resistance is validated through experimental measurement. Finally, the curves are compared with the analytical curve, and the results demonstrate the best fit between them.

## 3.2 Physical Structure and Material Characterization of Press-Pack Diodes

A typical press-pack diode, as shown in Figure 3.1, consists of a multilayer structure where different materials are stacked vertically next to each other. This configuration is used to evaluate a device's thermal and electrical performance under high surge current levels, resulting in extreme thermal conditions. Press-pack diodes exhibit a symmetrical heat dissipation pattern, where heat is generated at the center of the device, i.e., the silicon chip, and propagates equally in both upward and downward directions. The heat flow occurs from the silicon junction to the anode and cathode through multiple intermediate layers, such as molybdenum and copper. The heat then dissipates to the surrounding ambient environment through the case. Moreover, contact resistance, which exists at every interface where two different materials are in contact, also significantly influences the thermal performance of devices.

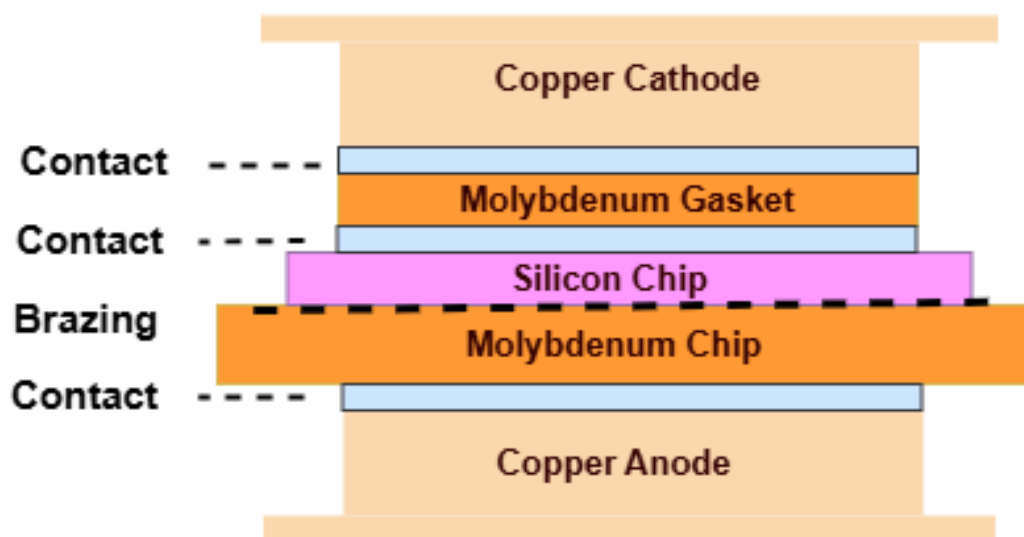


Fig. 3.1 Structural schematic of high power press pack diode.

### 3.3 Analytical Calculation of Thermal Resistance and Capacitance

The thermal resistance  $R_{th}$  and thermal capacitance  $C_{th}$  of each layer depend on their geometry, i.e., their diameter and thickness, as well as material properties including thermal conductivity, density, and specific heat capacity. Precise measurement of and comprehensive data on a material play a key role in the accurate estimation of the transient thermal responses of these devices. The  $R_{th}$  and  $C_{th}$  values of the device discussed in Section 3.2 can be obtained using the following equations:

$$R_{th} = \int_0^d \frac{1}{K_T A(z)} dz, \quad C_{th} = \int_0^d c_T \rho A(z) dz \quad (3.1)$$

where  $d$  is the layer thickness,  $K_T$  is the thermal conductivity,  $\rho$  is the material density,  $c_T$  is the specific heat capacity, and  $A(z)$  is the effective area at thickness  $z$ . Otherwise, contact thermal resistances are added between two layers where two different materials are nearly contacted [283–286]. The inclusion of these contact resistances helps to account the variation of temperature that occurs at the interface between two materials due to factors such as differences in planarity, surface roughness, and interface imperfections [287–289]. However, contact resistance is not considered in the case where two materials are brazed together.

### 3.4 Electro-Thermal Modeling Framework

In this section, the electro-thermal modeling framework implemented in this study is detailed and discussed to highlight the thermal dynamics of the device. Moreover, the development of the Cauer thermal network, parameter extraction, and its transformation into the Foster thermal network is also described.

#### 3.4.1 Development of the Cauer Thermal Network

Cauer model is considered as the realistic approach to represent the thermal response of a given device. The primary advantage of this model is its derivation from fundamental heat-transfer physics. In this type of thermal network, every node is directly connected to ground by a capacitor. Additionally, each pair of capacitors is connected through a resistor together. The grounded capacitor reflects the concept of heat transfer in one direction. The parameters calculated in Section 3.2 are relative to the thermal system and hence transformed to electrical parameters by analogy given in Table 3.1. In this analogy, thermal resistance and

thermal capacitance are equated to electrical resistance and capacitance, respectively. Heat flow (Power) is considered similar to electric current, while temperature difference is likened to electric voltage. Based on the analogy described in Table 3.1, a Cauer thermal equivalent electrical circuit is designed in PSIM as shown in Figure 3.2. Moreover, simulations were performed to obtain the transient thermal impedance  $Z_{th}$  curve [232, 290] as shown in Figure 3.3 by applying a step power dissipation to the thermal network while the case temperature was used as the reference. Where the steady state value indicates the thermal resistance calculated by simulation.

Table 3.1 Electrical and thermal analogy.

| Type       | Resistance                    | Potential                  | Flow                | Capacitance                |
|------------|-------------------------------|----------------------------|---------------------|----------------------------|
| Electrical | Ohmic Resistance ( $\Omega$ ) | Electrical Potential (V)   | Current (A)         | Electrical Capacitance (F) |
| Thermal    | Thermal Resistance (K/W)      | Temperature Difference (K) | Heat Flow/Power (W) | Thermal Capacitance (J/K)  |

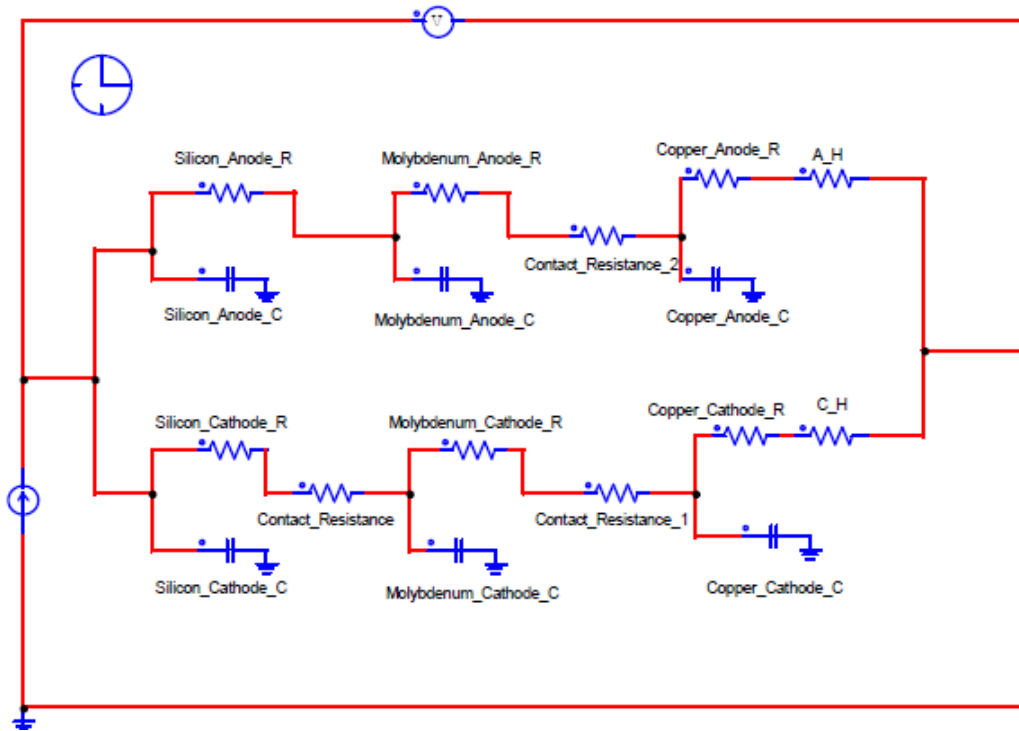


Fig. 3.2 Equivalent Cauer thermal network of the high-power press-pack diode structure in PSIM as described in Section 3.2.

### 3.4.2 Thermal Parameter Extraction for the Foster Thermal Network

To analyze the thermal behavior of a device, the Foster thermal network parameters are generally provided in datasheets, as this approach is considered convenient for estimating temperature rise since it does not include detailed material properties or layer dimensions. To design the Foster network, thermal parameters such as  $R_{th}$  and  $C_{th}$  are required. There are different methods to extract these thermal parameters, and a common approach is curve fitting. In curve fitting, measured data obtained through thermal measurements or data sheet are analyzed and mathematical models are fitted to these data points to extract the parameters of interest, e.g  $R_{th}$  and  $\tau$ . These parameters are crucial for accurately modeling the thermal behavior of the device and optimizing its design for better heat dissipation and thermal management. Curve fitting algorithms can vary depending on the nature of the complexity of the thermal system being analyzed and the type of data available. Common techniques include least squares fitting, non-linear regression and optimization algorithms.

In this study curve fitting technique is used to extract the thermal parameters in MATLAB® through non linear regression method, in particular  $R$  and  $\tau$ , from the transient thermal impedance versus time curve which is obtained from the Cauer thermal network in Section 3.4.1. The curve fitting process generates an interpolation fit to the data using an exponential equation given in Eq 3.2, aiming to align the model with the impedance curve. The thermal impedance versus time curve is shown in Figure 3.3. To determine the appropriate number of RC stages ( $i$ ) required to accurately represent the thermal response, the fitting procedure was repeated for increasing values of  $i$ , and the resulting fit quality was evaluated using the mean squared error ( $\sigma^2$ ) between the fitted curve and the impedance curve obtained through the Cauer network. A four-stage exponential model ( $i = 4$ ) was found to provide the best trade-off between fitting accuracy and model complexity, with negligible improvement in  $\sigma^2$  observed for higher-order fits. The proposed structure consists of four RC branches; the fitness function is obtained as

$$Z_{th} = \sum_{i=1}^4 R_i \times \left| 1 - \exp(-t/\tau_i) \right| \quad (3.2)$$

Where  $R_i$  is the thermal resistance and  $\tau_i$  is the time constant.

Using the above exponential equation, the curve fitting is performed and the resultant fitting curve is shown in Figure 3.4. The obtained data is given in Table 3.2. The  $\sigma^2$  error is 0.98% which shows a good accuracy of the estimated curve with the measured one.

Table 3.2 Extracted thermal parameters.

|          | 1      | 2      | 3      | 4      |
|----------|--------|--------|--------|--------|
| $R_i$    | 4.6207 | 1.1651 | 9.8269 | 1.0222 |
| $\tau_i$ | 0.1012 | 0.0036 | 1.4155 | 0.3844 |

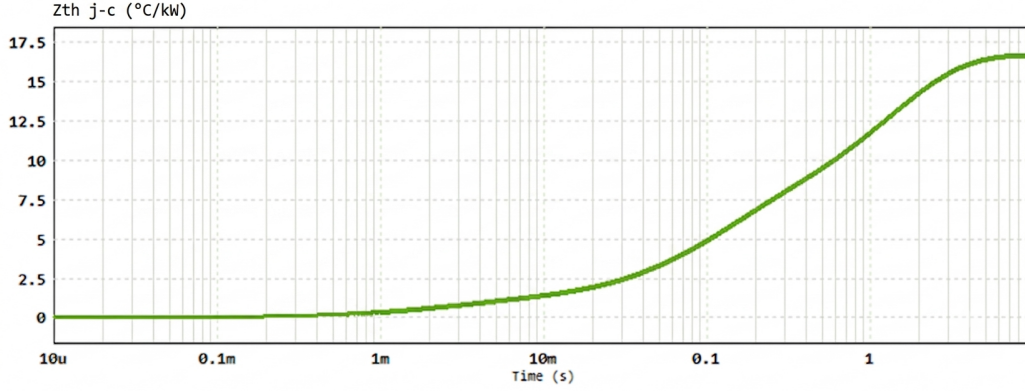


Fig. 3.3 Thermal impedance versus time curve obtained through cauer thermal model.

Once the  $R_i$  and  $\tau_i$  values are known, we can easily find the thermal capacitance  $C_i$  as follow

$$C_i = \frac{\tau_i}{R_i} \quad (3.3)$$

### 3.4.3 Transformation and Interpretation Using Foster Thermal Networks

Unlike the Cauer thermal network, Foster thermal network is not based on the physical dimensions and geometry of the device. Instead, they are a mathematical representation that considers the device as a single layer rather than multiple layers. The circuit diagram of the Foster network model, as depicted in Figure 3.5, reveals a notable characteristic where only one capacitor is connected to the ground. This scenario, while not entirely realistic, is a simplification used for thermal impedance modeling purpose of devices. The parameters are derived by using Eq 3.2 in Section 3.4.2. In the Foster thermal network, the RC connection is maintained independently of the physical arrangement of the device layers. Furthermore, the numerical values given in Table 3.2 for these elements are determined through curve fitting, and it is not necessary for the corresponding parameters to match the derived values precisely for each section of the designed circuit. However, the total sum of the thermal resistances and thermal capacitances must be similar, which is crucial. Figure 3.6 represents

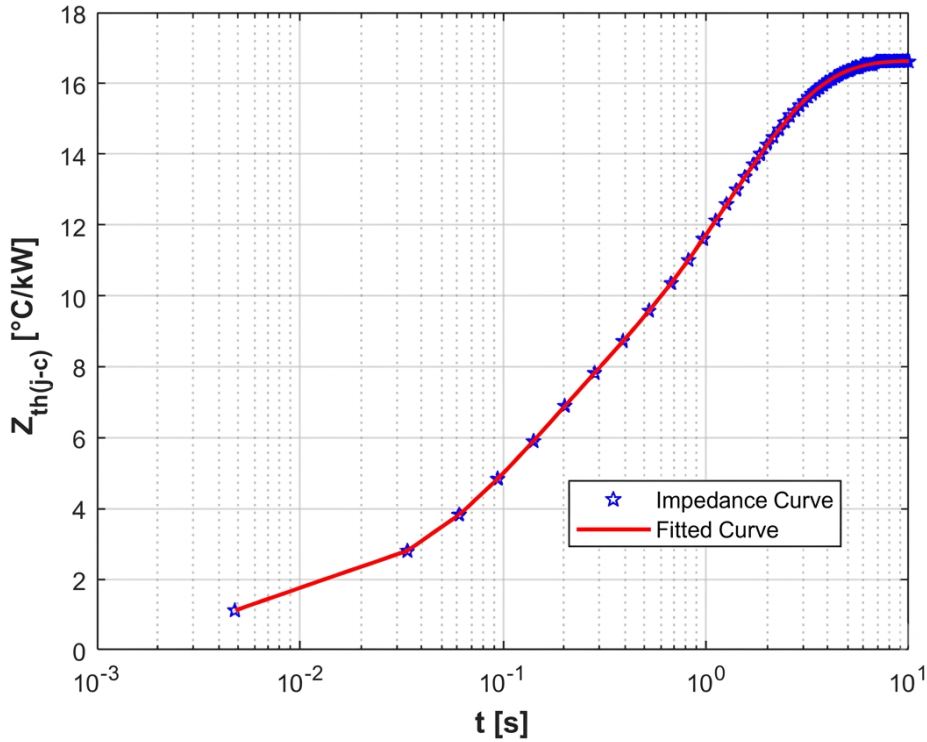


Fig. 3.4 Curve fitting in MATLAB®.

the transient thermal impedance obtained through the Foster thermal network, simulated in PSIM. Despite lacking a physical basis, the mathematical simplicity of the Foster model, along with its independence from device physical dimensions, and ability to yield results similar to other models makes the Foster model specifications valuable for manufacturers to provide to their customers to faster analyze the thermal management of device during different current waveforms.

### 3.5 Experimental Setup

In order to verify the thermal resistance obtained analytically and through simulations, a simple experimental method is introduced to measure the thermal resistance of high power semiconductor press pack devices. The experimental work was conducted in the Poseico laboratory for the simulated device with 46 mm copper pole diameter. The experiment consist of the use of a special equipment to investigate thermal resistance under controlled conditions. Within the test setup, the diode was positioned between an upper and lower aluminum cylinder within the frame of the press machine with appropriate pressure ranging

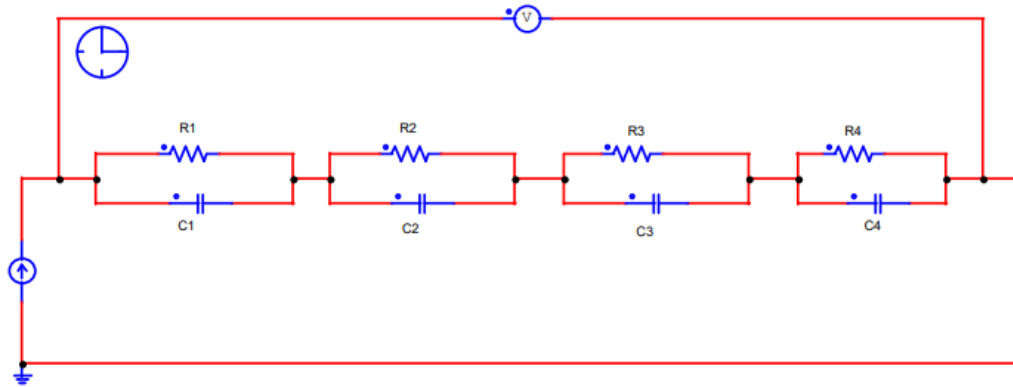


Fig. 3.5 Foster network circuit diagram.

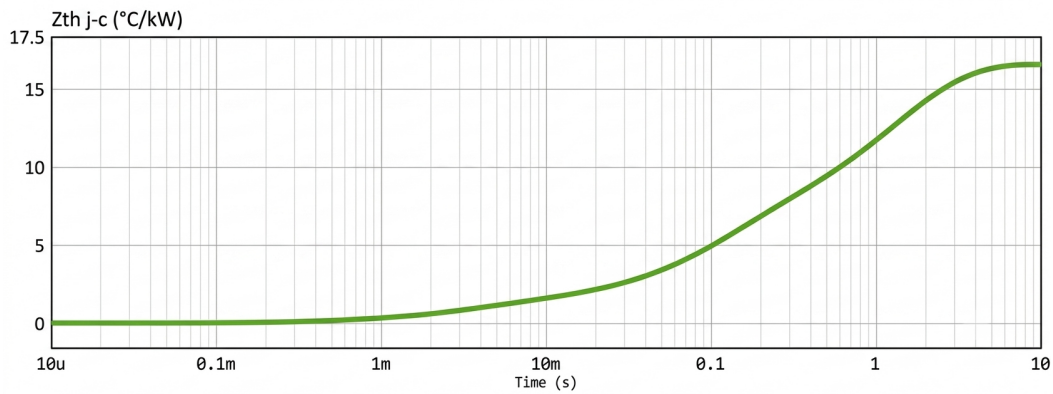


Fig. 3.6 Thermal impedance versus time curve obtained through foster thermal model.

from 22 kN to 28 kN as shown in Figure 3.7. No intermediate material was placed between the device under test (DUT) and the aluminum cylinders; a direct contact was established between the anode and cathode copper poles of the diode housing and the corresponding aluminum cylinders. The upper aluminum cylinder was connected to a heat plate with a constant temperature of 125°C. Conversely, the lower aluminum cylinder was connected to a cold plate to ensure a constant supply of 40°C water. Both aluminum cylinders have same diameters to the selected diode diameter and were equipped with thermo-couples as illustrated in Figure 3.8. To minimize lateral heat losses and promote predominantly axial heat flow through the stack, the assembly was wrapped with a thermally insulating material similar to that used for insulating boiler pipes and heating systems. These thermo-couples are connected to the data logger (GRAPHTEC midi LOGGER GL800) via an interface which enables real-time temperature monitoring.

Initially, at the beginning of the experiment, the heat plate initiates transfer of heat to the upper aluminum cylinder. Simultaneously, the lower aluminum cylinder acted as a thermal



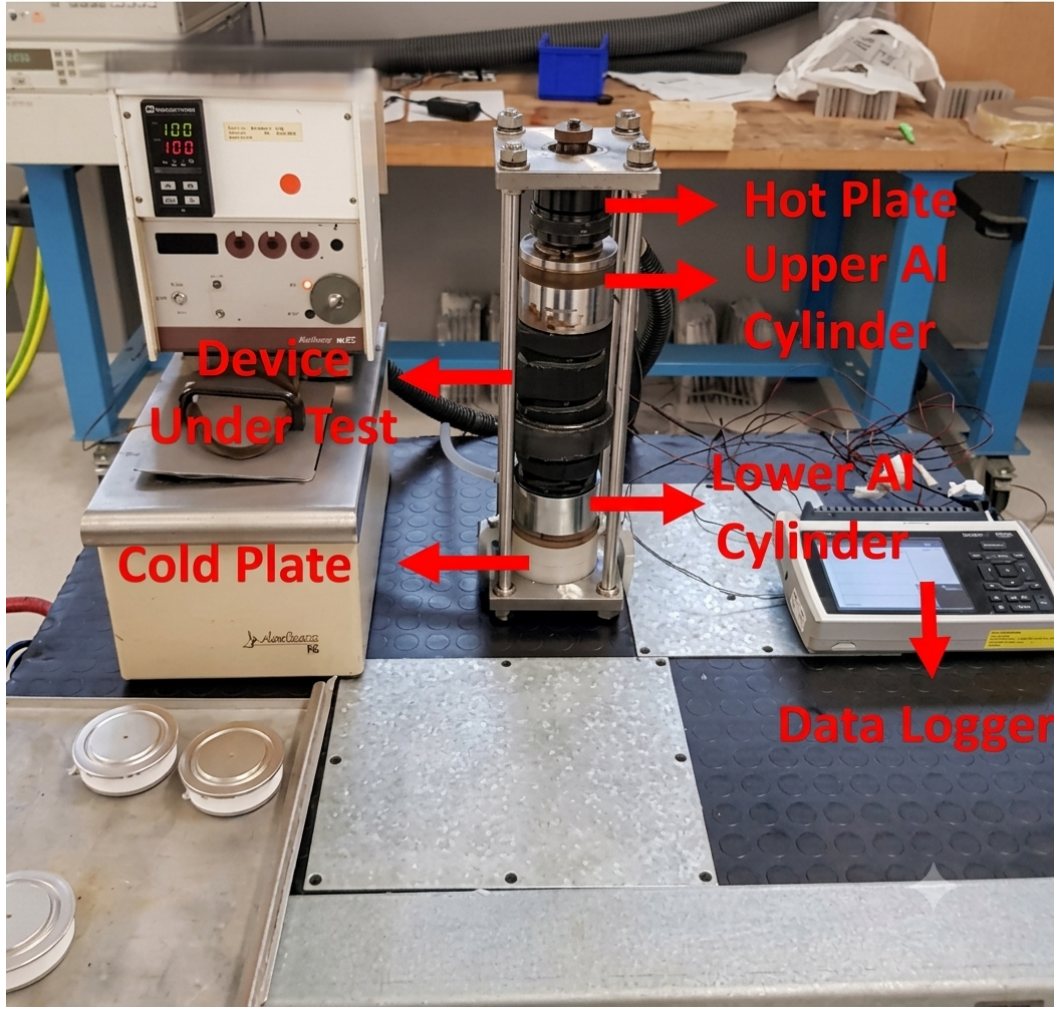


Fig. 3.7 Experimental setup for thermal resistance measurement.

sink, dissipating heat into the cold plate. After a specific period of time, thermal stability was achieved for both interconnected aluminum cylinders, and the resultant temperature changes were recorded by the data logger through thermo-couples as given in Table 3.3 The heat flow at upper aluminum cylinder can be evaluated as follows:

$$Q_1 = \frac{T_1 - T_2}{R_{th1}} \text{ W} \quad (3.4)$$

where  $Q_1$  is the amount of heat flow at upper aluminum cylinder,  $T_1, T_2$  are temperatures measured by the respective thermo-couples, and  $R_{th1}$  are the thermal resistance of respective cylinder.

Putting the value of  $R_{th1}$  and measured values of  $T_1$  &  $T_2$  in Eq (3.4), The calculated value of



Table 3.3 Temperature measured at each thermocouple.

| T1   | T2   | T3   | T4   |
|------|------|------|------|
| 70.9 | 47.6 | 40.2 | 27.9 |

$Q_1$  is

$$Q_1 = 122 \text{ W} \quad (3.5)$$

Similarly the heat flow at lower aluminum cylinder may be calculate as

$$Q_2 = \frac{T_3 - T_4}{R_{th2}} \text{ W} \quad (3.6)$$

where  $Q_2$  is the amount of heat flow at lower aluminum cylinder,  $T_3, T_4$  are temperatures measured by the respective thermo-couples, and  $R_{th2}$  are the thermal resistance of respective cylinder.

By solving Eq (3.6) with measured values of  $T_3$  &  $T_4$ , the value of  $Q_2$  is given as

$$Q_2 = 122 \text{ W} \quad (3.7)$$

The thermal resistance of diode  $R_{thdiode}$  can be given as

$$R_{thdiode} = \frac{T_2 - T_3}{Q_1} \text{ } ^\circ\text{C/kW} \quad (3.8)$$

Where the thermal resistances  $R_{th1}$  and  $R_{th2}$  of the two cylinders are evaluated using the thermal conductivity of aluminum and their geometrical dimensions. In order to obtain a correct measurement, the heat flow must pass through all the blocks without significant heat losses. The comparison between the  $Q_1$  and  $Q_2$  values could be used to check this condition. The value of  $R_{thdiode}$  calculated from Eq (3.8) is given as follow

$$R_{thdiode} = 60.3^\circ\text{C/kW} \quad (3.9)$$

The total thermal resistance from anode to cathode of the press-pack diode is the result of the series of two equal resistance i.e.  $R_{th(j-h)anode}$  and  $R_{th(j-h)cathode}$

$$R_{thdiode} = R_{th(j-h)anode} + R_{th(j-h)cathode} \quad (3.10)$$

$$= 2 \times R_{th(j-h)anode} = 2 \times R_{th(j-h)cathode} \quad (3.11)$$

In normal functioning, it is assumed that heat generates inside the diode junction and goes out both in anode and cathode directions. Therefore the correct diode  $R_{th(j-h)}$  value is the parallel of the two equal resistances i.e.  $R_{th(j-h)anode}$  and  $R_{th(j-h)cathode}$  given as:

$$R_{th(j-h)} = \frac{R_{th(j-h)anode} \times R_{th(j-h)cathode}}{R_{th(j-h)anode} + R_{th(j-h)cathode}} \text{ } ^\circ\text{C/kW} \quad (3.12)$$

$$= \frac{1}{2}R_{th(j-h)anode} = \frac{1}{2}R_{th(j-h)cathode} \quad (3.13)$$

Using the above equations it is possible to obtain the relation between the measured valued  $R_{thdiode}$  and the real thermal resistance of the diode  $R_{th(j-h)}$ :

$$R_{th(j-h)} = \frac{R_{thdiode}}{4} \quad (3.14)$$

Using the above equation, The total calculated thermal resistance  $R_{th(j-h)}$  is given as

$$R_{th(j-h)} = 15^\circ\text{C/kW} \quad (3.15)$$

The measured thermal resistance value is  $15^\circ\text{C/kW}$ , whereas the simulation yields a value of approximately  $16^\circ\text{C/kW}$  as reported in Figures 3.3, 3.4, 3.6, and 3.9. The obtained results indicate a close match and show the best fit between the simulation and experimental measurement.

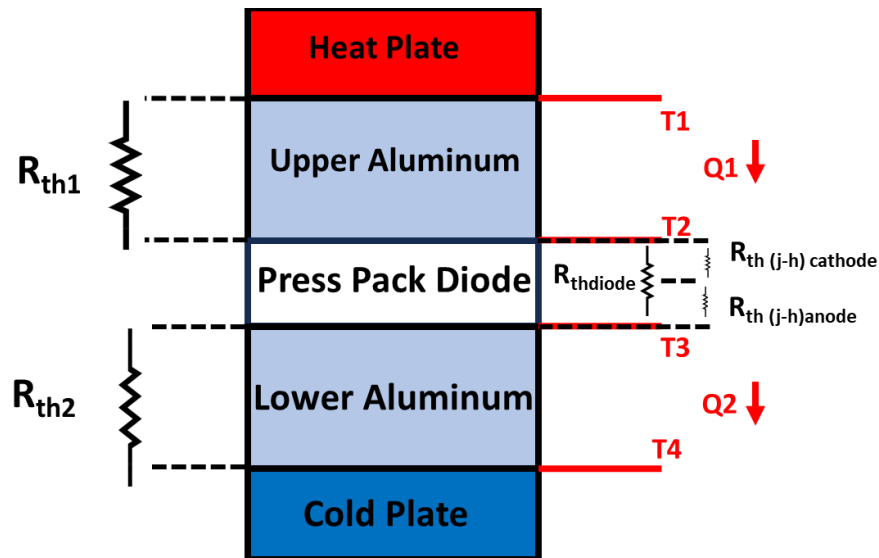


Fig. 3.8 Test equipment scheme.

### 3.5.1 Experimental Validation and Discussion

The thermal impedance curves obtained in the previous sections from both the Cauer network and the Foster Network are compared with analytical results obtained through Eq 3.2. The comparison among Cauer, Foster, and analytical models are shown in Figure 3.9. The comparison indicates a strong alignment between the obtained results. Moreover, it is also evident from the comparison, that the thermal parameters and time constants extracted from the Cauer model for designing the Foster network are very accurate.

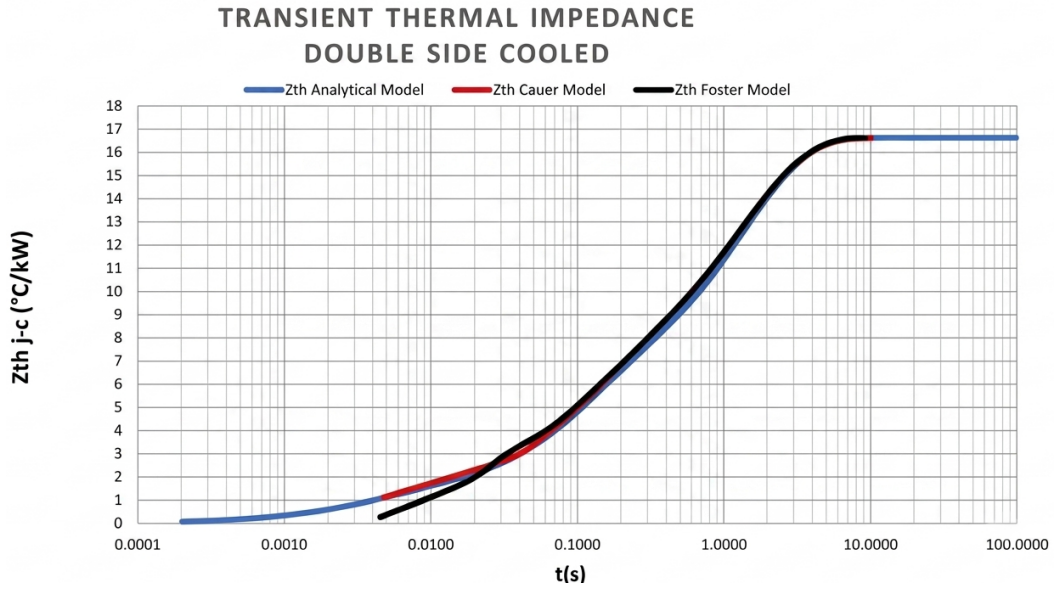


Fig. 3.9 Comparison of the cauer, foster and analytical model.

## 3.6 Limitations

This chapter primarily focuses on the analysis of transient thermal impedance. However, in practical applications, power semiconductor devices are sometimes exposed to high surge current conditions, which play a critical role in determining device safety and reliability. During these events, the power dissipation increases rapidly within a very short time duration, which may result in high electro-thermal stress. Therefore, accurate modeling of electrical parameters such as voltage under high surge conditions and the corresponding temperature is crucial. These aspects, however, are beyond the scope of this chapter and are not addressed in the present analysis.

### 3.7 Conclusion

This chapter presents a comprehensive approach to model the transient thermal impedance of high power press pack diodes. Thermal parameters such as thermal resistance and thermal capacitance are analytically calculated by the physical dimensions and material properties of the diode. Furthermore, an electric equivalent circuit, known as Cauer thermal network, is developed in PSIM software. Simulations were performed to obtain transient thermal impedance over time curve, which are then transformed into a Foster thermal network for further analysis and simulations. The parameters required to design a Foster thermal network were extracted using the curve fitting technique in MATLAB<sup>®</sup> by nonlinear regression. The extracted parameters, such as thermal resistances and time constants, help to provide an insight into device thermal behavior under different operating conditions and also allows to estimate the average current that a device can safely handle at different pulse durations and shapes. In addition, thermal resistance values obtained by simulations are validated through experimental measurement, which enhances the reliability of the proposed modeling approach. Moreover, the curves obtained through Cauer model and Foster model simulations are compared with the analytical curve, which shows strong agreement, demonstrating the effectiveness of the methodology to accurately estimate the transient thermal behavior of the diode. In summary, this study contributes to improve the understanding of thermal management in high power press pack diodes and provides valuable insights for optimizing their performance and reliability in various applications, especially industrial applications.

#### Publication Related to this Chapter

This chapter reproduces material from the following publication:

**F. Ahmad**, F. Portesine, M. Ashero, and L. Vaccaro, “*Transient Thermal Impedance Characterization of New High-Power Press Pack Diodes*,” in **Proceedings of the 2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)**, Jun. 2024. DOI: [10.1109/SPEEDAM61530.2024.10608828](https://doi.org/10.1109/SPEEDAM61530.2024.10608828)



# Chapter 4

## Surge Current Electro-Thermal Modeling and Junction Temperature Estimation

This chapter discusses electro-thermal modeling and junction temperature estimation for high-power devices under higher surge current levels. In section 4.2 the surge wave generator is developed, and its design and operating principle are explained. Moreover, section 4.3 highlights a proposed electro-thermal model to estimate the junction temperature under anomalous surge conditions. In addition, the experimental setup is presented in Section 4.4. This section discuss the validation procedure and analysis, where the measurement system and testing methodology are also discussed. Section 4.5 provides the corresponding test results and validates the model accuracy. Subsequently, Section 4.6 gives further analysis of the device behavior under surge conditions, focusing on the electrical and thermal characteristics. Furthermore, in section 4.7 the modeling and simulation approaches, including the resistance–capacitance (RC) equivalent method and the FEM are presented. Section 4.8 detailed discussed the simulation results, where the predicted thermal responses are evaluated and compared with experimental tests. The limitations of the study are outlined in section 4.9. Finally, Section 4.10 summarizes the main conclusions of the chapter.

### 4.1 Overview and Research Motivation

Initially, semiconductor devices, mostly based on silicon, were designed for low-power applications where operations required a limited range of power density with efficient thermal performance. However, with advancements in semiconductor technology, the demand of robust power conversion systems has increased, resulting in a growing need for the development of high-power semiconductor devices. These high-power devices are developed with modern

engineering methods and techniques with improved critical electric and thermal designs, enabling them to operate reliably at higher currents and temperatures. Additionally, to further increase power ratings, packaging technologies and chip designs have also been improved in order to reduce thermal resistance, allowing more efficient heat dissipation. In particular, the development of press pack devices employing PCT has enhanced the cooling efficiency of devices by enabling double-sided cooling. Moreover, a number of studies are available in the literature that are focused on improving heat sink and cooling techniques to optimize thermal management. Despite these advancements, the performance of semiconductor devices remains susceptible to extreme surge events, leading it to degrade. For example, in abnormal scenarios, such as short circuits across devices, the current can increase instantaneously to a higher level within milliseconds, resulting in a fast and significant rise in temperature [291]. Such abrupt thermal excursions can critically effect the structural integrity and long term reliability of the devices. Therefore, it is crucial to evaluate the thermal and electrical characteristics of the devices to define safe surge current limits, ensuring reliable operation under fault conditions. To address this problem, manufacturers generally provide surge current ratings in device data sheets. These ratings are based on extensive experimental tests and electro-thermal simulations, as outlined by different standardized procedures, including those defined by the JEDEC and IEC [67, 68]. These standardized methodologies provide a benchmark for device qualification under transient surge conditions, highlighting that higher junction temperatures are a key factor that may degrade device performance, leading to chip failure and the degradation of key electrical parameters such as the on-state resistance. These parameters can directly affect the voltage drop across the device during conduction. In this context, extensive research has been conducted to assess the junction temperature, current and voltage capabilities of devices in various conditions, resulting in the development of innovative temperature measurement techniques, as well as the formulation of various models with which to analyze electrical and thermal behavior of these devices. However, existing models in the literature either oversimplify critical factors, including spatial temperature variations and non-uniform current distribution, or depend on measurement-based methods. These limitations primarily arise from a model's dependence on static I–V characteristics, which significantly constrain model accuracy under practical surge conditions. Consequently, the extraction of key electrical parameters, such as forward voltage drop ( $V_F$ ) and slope resistance ( $r_T$ ), becomes limited. Moreover, the direct measurement of temperature and forward voltage for high surge current is not feasible due to device safety concerns. To address these challenges, this chapter proposes a forward voltage and temperature evaluation methodology for high-power semiconductor devices under high-surge conditions. The main contributions of this chapter are as follows:

1. An electro-thermal model is proposed that integrates electrical parameters at the rated current with thermal simulation data to estimate forward voltage and  $r_T$  characteristics under surge conditions.
2. An experimental setup is developed to perform high-surge-current tests to measure the forward voltage, and the obtained results are used to validate the model's accuracy.
3. Simulations are performed to evaluate thermal behavior and temperature under surge conditions.
4. The proposed model provides a reliable framework for assessing chip-level surge capabilities and improving the modeling of device behavior under high-current stress.

## 4.2 Surge Wave Generator

The simulation setup includes a surge wave generator circuit, as illustrated in Figure 4.1, which generates a wide range of peak surge currents at different voltage levels. A sinusoidal voltage source drives a full-wave single-phase rectifier connected in series with a diode, a current sensor, and an adjustable resistor  $R_1$  to set the desired voltage and current levels. A controlled switch regulates the conduction interval and enables the generation of surge currents for a specified duration. The surge waveform is controlled using a step voltage source and a gate-triggered switching sequence, allowing the generation of surge pulses. The voltages  $V_1$  and  $V_2$ , which are measured across the diode and the series resistor, respectively, are used to evaluate the instantaneous current and corresponding power applied to the device under test (DUT). This power profile is then used within the thermal network to determine the diode's transient thermal response, enabling the assessment of junction temperature variations and possible failure mechanisms.

## 4.3 Proposed Model

The proposed forward-voltage prediction model is based on the surge current profiles generated by the surge-wave generator described in Section 4.2. Forward voltage drop is considered a key parameter that can influence the temperature of high-power semiconductor devices. Therefore, an accurate and precise measurement of forward voltage is critical to maintain reliable and efficient operation, especially under high-surge-current conditions. Existing approaches in the literature, widely employed by manufacturers and researchers, can be



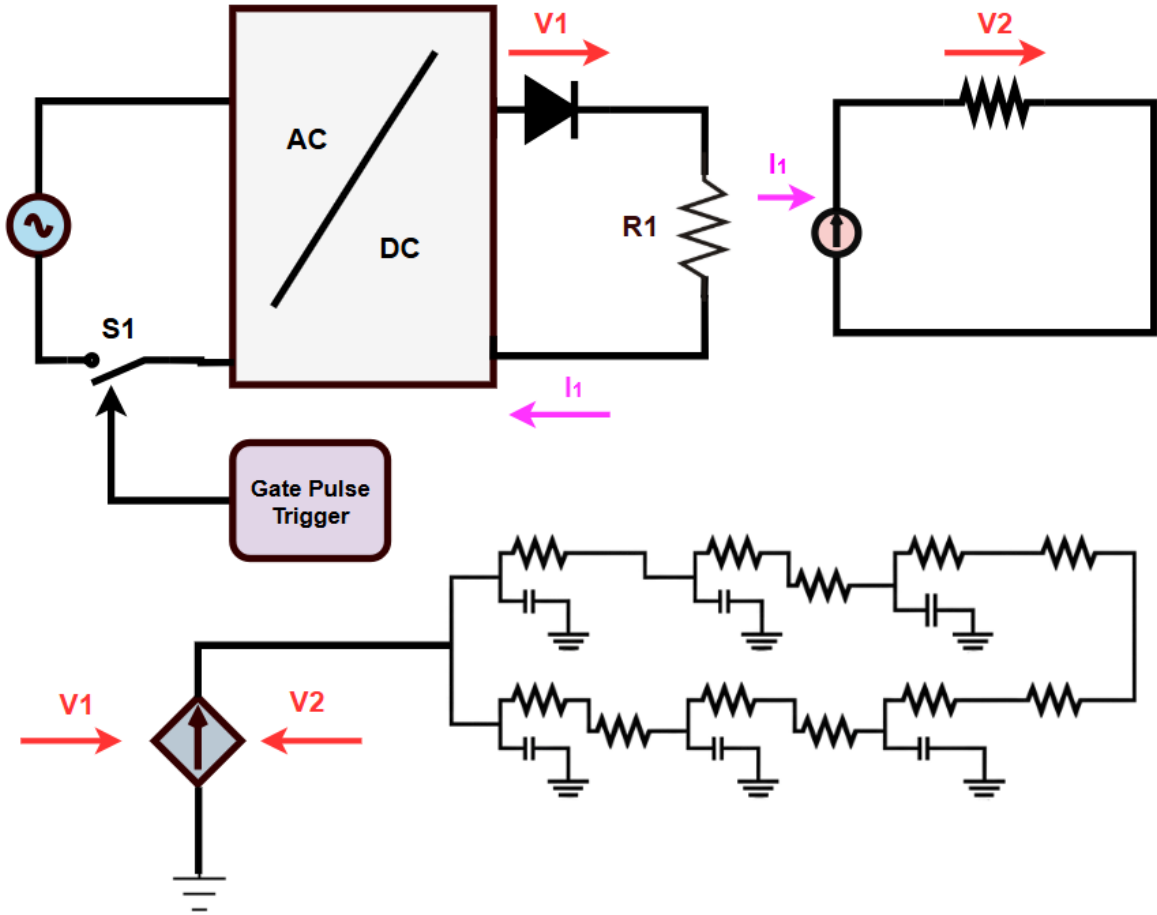


Fig. 4.1 Schematic representation of the surge wave generator setup.

broadly categorized into static I–V models and direct experimental tests. The forward voltage,  $V_F$ , can be calculated using a static forward I–V curve as follows:

$$V_F = V_{T_0} + r_{T_0} \cdot I(t) \quad (4.1)$$

where  $V_{T_0}$  and  $r_{T_0}$  represent the threshold voltage and slope resistance, respectively, which are functions of the diode's geometry and material properties. These are discussed in detail in Section 3.2, and are mostly provided by the manufacturers in the device datasheet for rated current and voltage.

Static I–V models neglect the electro-thermal coupling effect that occurs during transient surge currents because they are calculated based on steady-state device characteristics. As a result, they are not able to incorporate the nonlinear and dynamic behavior of devices under higher current densities and elevated junction temperatures, which can lead to significant errors in estimations. In contrast, performing experimental tests under surge conditions

provides direct measurements; however, they exhibit critical limitations. High surge currents can result in elevated temperatures and increased electrical stress in the device, potentially leading to performance degradation and catastrophic failure, which are irreversible. This can compromise the reliability of the device and also increase costs, which can limit the repeatability of performing tests. To address these issues, there is a need for an accurate modeling approach that is capable of predicting accurate forward voltage drops during surge events without depending on destructive testing or simplified static models. There-

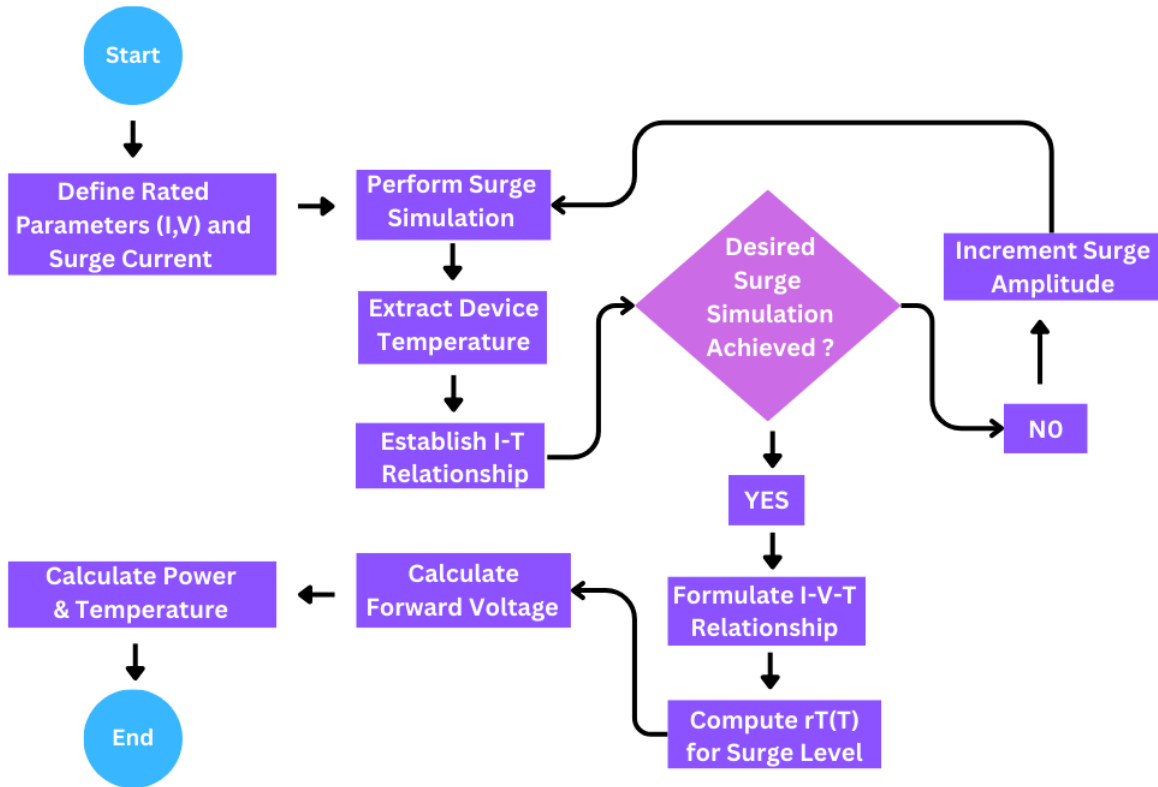


Fig. 4.2 System model of the proposed forward voltage prediction model.

fore, the proposed model, illustrated in Figure 4.2, incorporates the relationship between temperature and surge current (derived from the surge current generator in Section 4.2 to overcome the limitations of existing models). At rated currents and voltages, the temperature is evaluated for surge currents with various pulse amplitudes ranging from the rated current to the desired level over a duration of 10 ms, as shown in Figure 4.3a. The results show progressively increasing temperature with higher current levels, resulting in higher peak temperatures, as depicted in Figure 4.3b. By extracting the junction temperature values from the thermal simulations at different surge current levels, a curve-fitting procedure was applied to establish the temperature–current relationship. This procedure enables the establishment of a temperature–current relationship by fitting a second-order polynomial. The increase in

simulated temperature displays a smooth and continuous nonlinear dependency on device current, and a second-order polynomial offers optimal capability to accurately capture this behavior while avoiding unnecessary complexity in the model. This makes the polynomial form the best choice and a computationally efficient method to approximate thermal response across the simulated current range. The second-order fitted polynomial is given as follows:

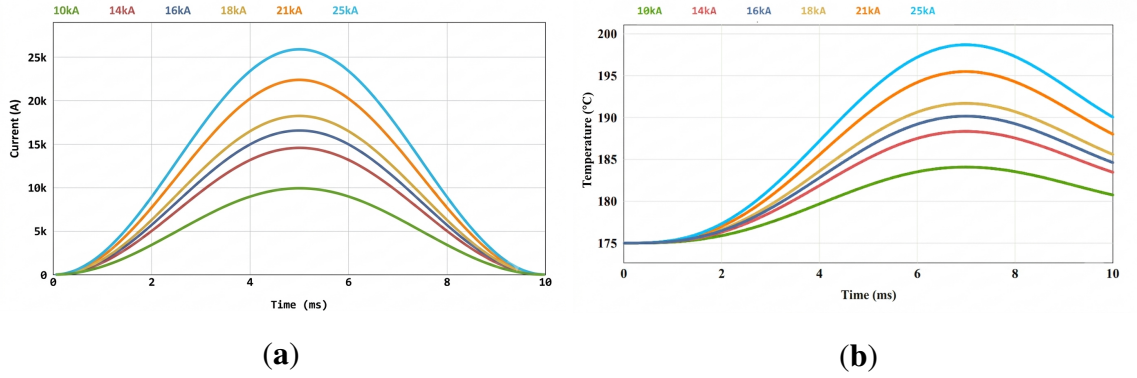


Fig. 4.3 Simulated results under varying peak surge current conditions: (a) instantaneous power dissipation profiles; (b) corresponding transient temperature responses.

$$T = 5 \times 10^{-8} I^2 + 0.0005 I + 170 \quad (4.2)$$

where  $I$  is the desired surge current. This relation is then employed to compute a temperature-dependent slope resistance for higher surge currents, as follows:

$$r_T(T, t) = r_{T_0} \cdot (1 + \alpha \cdot (\Delta T)) \quad (4.3)$$

where  $\alpha$  is the temperature coefficient of resistivity, depending on the extent of doping on the silicon chip. The resulting forward voltage under surge conditions can be expressed as follows:

$$V_F = V_{T_0} + r_T(T) \cdot I(t) \quad (4.4)$$

The proposed model, hence, accommodates thermal effects induced by surge currents into a process of voltage prediction, resulting in an accurate, non-destructive approach to predict forward voltage across a wide range of surge currents. Unlike static I–V models, the proposed model dynamically accommodates temperature changes, while avoiding the risks associated with direct surge testing.

Using this temperature-dependent voltage, the instantaneous power dissipation can be calculated as follows:

$$P(t) = V(t) \cdot I(t) \quad (4.5)$$

Substituting these values into Equation (4.5), the power dissipation equation can be rewritten as follows:

$$P(t) = V_{T_0} \cdot I(t) + r_T(T) \cdot I^2(t) \quad (4.6)$$

The root mean square (RMS) peak current is given by the following:

$$I_{rms}^2 = \frac{I_{Peak}^2}{\sqrt{2}} \quad (4.7)$$

## 4.4 Experimental Setup, Validation and Analysis

### 4.4.1 Experimental Setup

The experiment employs the resistance-capacitor charge and discharge method, where the capacitor is charged to a predetermined value to achieve the desired peak discharge current. The capacitor  $C_1$ , is charged using an external power supply through thyristor  $X_1$ , as depicted in Figure 4.4. The experimental setup also includes a press machine designed to maintain

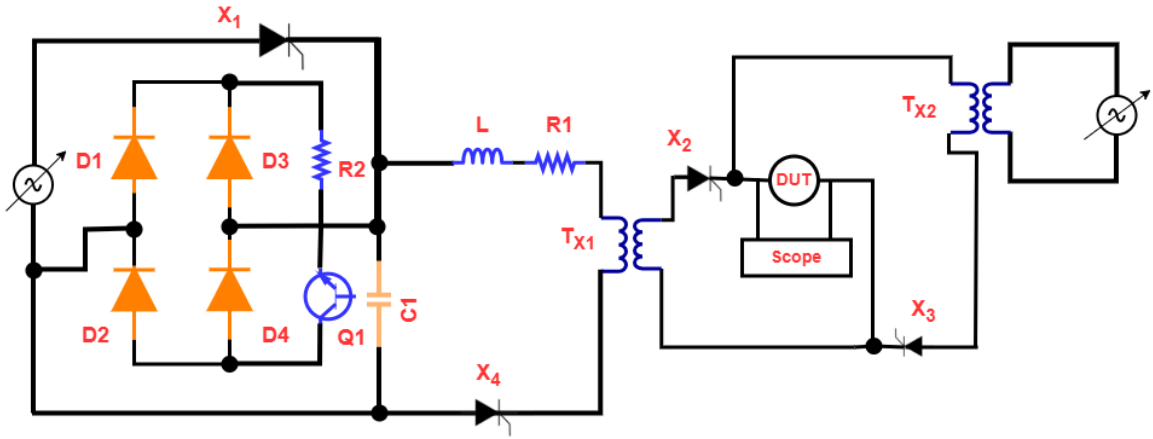


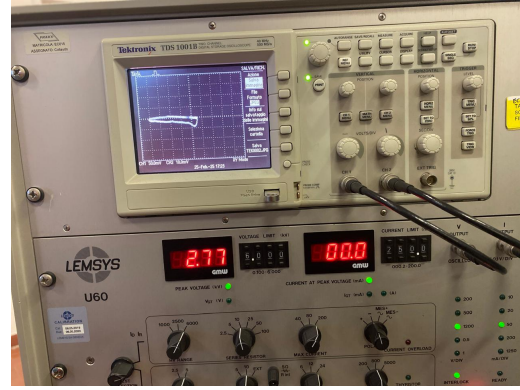
Fig. 4.4 Schematic representation of the experimental surge current test setup, including the surge generator and the DUT.

the DUT at specific temperature and pressure conditions. The experiment was performed in accordance with the IEC 60747–2 standard [68] using a device with a repetitive peak reverse voltage  $V_{RRM}$  of 4400 V and a diameter of 48 mm. A pre-surge test was performed on the device under test, preliminarily checking the forward voltage  $V_F$ ,  $V_{RRM}$ , and repetitive peak

reverse current  $I_{RRM}$  values, as shown in Figure 4.5. The press machine was connected to a transformer, which, in turn, was linked to an inductor via a resistor to regulate the current through the DUT. For safety concerns, the equipment was enclosed within a protective grill.



(a)



(b)

Fig. 4.5 Experimental equipment setup used for pre- and post-surge electrical characterization: (a) forward conduction test setup. (b)  $V_{RRM}$  and  $I_{RRM}$  test setup.

To generate a surge current, capacitor  $C_1$  was isolated from the external power supply by disengaging the gate of the thyristor  $X_1$ . During the charging phase, for the positive half-cycle of the power supply, thyristors  $X_4$  and  $X_2$  were triggered, allowing the current to flow through the capacitor and inductor. The flowing current was multiplied by the transformer  $T_{X1}$  turns ratio to obtain the maximum desired peak current. Upon completion of the positive cycle, the negative half-cycle began, and thyristor  $X_3$  was triggered as the current crossed zero. As the current decreased, thyristor  $X_2$  turned off. The voltage on  $C_1$  was then reversed and subsequently discharged through an appropriate resistor. To measure the current, a Rogowski probe was connected on the primary of the  $T_{X1}$  transformer. The surge was set to a period of 10 ms by using a board and measured through a four-channel oscilloscope, as shown in Figure 4.6. To completely study the behavior of the device and evaluate its performance under surge conditions, a series of experimental tests were conducted across varying currents. The surge current levels were systematically increased by adjusting the voltage and capacitance of the power supply and capacitor, as detailed in Table 4.1. Moreover, a 2 min interval pause was kept between successive pulses for each test, allowing the device to cool down. The output results were recorded using an oscilloscope, with the peak values of current waveforms and corresponding voltages depicted in Figure 4.7. Notably, in this study, no additional heat sink or active cooling mechanism was employed. The absence of a cooling system meant that the investigated thermal behavior can only be attributed to the device's intrinsic thermal dissipation properties.



Fig. 4.6 Experimental setup used for measuring the forward voltage of the DUT across various surge current levels.

Table 4.1 Measured surge current and corresponding forward voltage.

| Capacitor (Supply) [V] | Surge Current [A] | Forward Voltage ( $V_F$ ) [V] |
|------------------------|-------------------|-------------------------------|
| 200                    | 6400              | 3.6                           |
| 250                    | 8600              | 4.4                           |
| 300                    | 10,800            | 5.4                           |
| 350                    | 14,400            | 6.2                           |
| 400                    | 16,800            | 7.3                           |
| 450                    | 18,600            | 7.4                           |
| 500                    | 20,400            | 7.8                           |

## 4.5 Results and Validation

In order to verify the accuracy of the proposed model in predicting voltages under high-current and -voltage conditions, a series of surge current tests were carried out, as discussed in Section 4.4.1. For each surge current pulse, the measured forward voltage drop was recorded to monitor the device's electrical response, as shown in Figure 4.7. The experimental results closely aligned with the simulated voltages, as shown in Figure 4.8, demonstrating the accuracy of the model and its efficiency across a range of performed tests, as also shown in Table 4.1. In a lower range of currents and voltages, the static I–V model aligns closely with both the measured and proposed model values, due to the minimal effect of self heating. However, as the current level increases, the voltage rises and the dissipated energy is rapidly converted into heat, leading to an increase in temperature. Consequently, a significant deviation begins between the static I–V and the proposed model's results. For example, at a surge current with a peak value of 20.5 kA, the static I–V model results in a forward voltage of 9 V, while the proposed model results in 7.5 V. Notably, compared to traditional



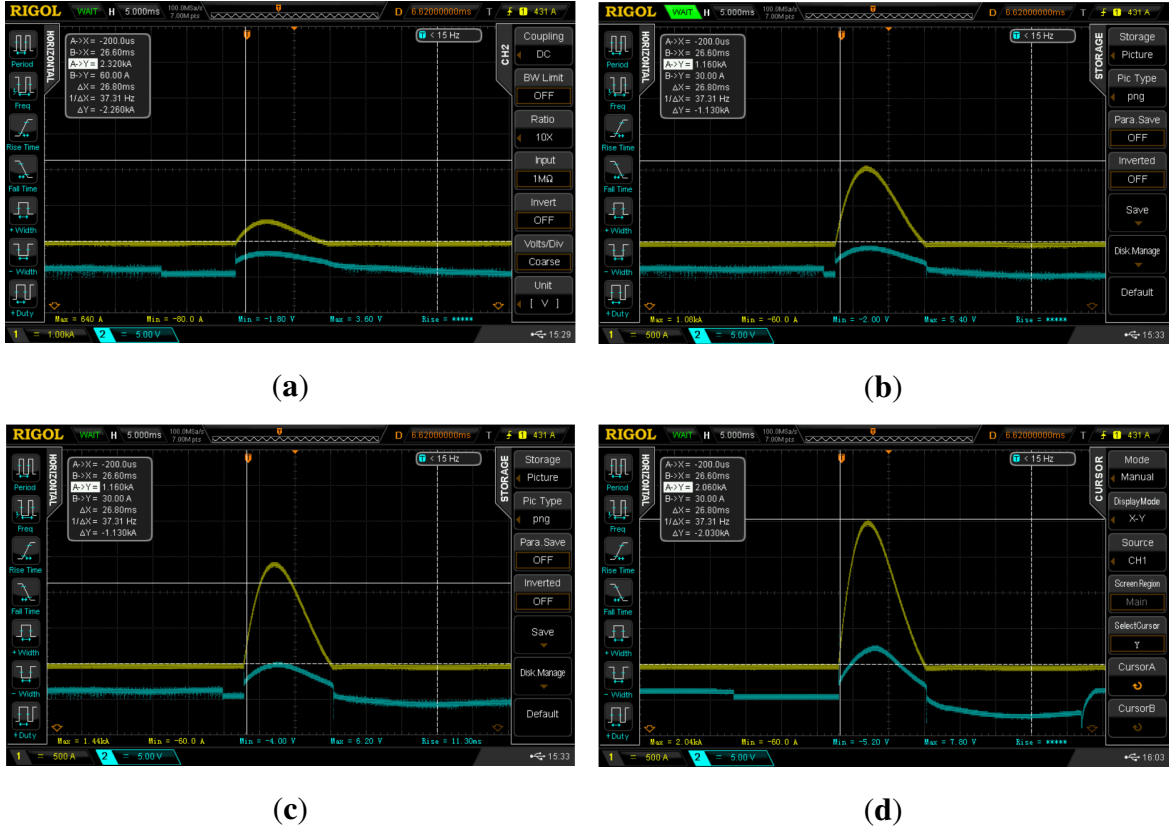


Fig. 4.7 Surge current conditions and corresponding forward voltages: (a) 6400 A,  $V_F = 3.6$  V (b) 10,800 A,  $V_F = 5.4$  V (c) 14,400 A,  $V_F = 6.2$  V (d) 20,400 A,  $V_F = 7.8$  V. In each subplot, the yellow trace denotes the surge current and the teal trace denotes the forward voltage.

static I–V models, which differ due to their isothermal assumption, the proposed model accurately captures negative differential resistance and the resulting current saturation caused by temperature rises. This validation under higher and nonlinear conditions highlights the proposed model’s suitability for applications in which reliability is necessary, including short-circuit protection design, surge arrester operation, and fault analysis in power systems.

## 4.6 Analysis

The experimental results show a continuous increase in the slope ( $dI/dV$ ) of the I–V characteristic curve, highlighting a significant rise in differential conductance. This phenomenon is related to the direct influence of the electro-thermal relationship within the device, i.e., an increase in temperature can result in higher current conduction across the device. Hence, as the voltage increases, the temperature of the device increases, which lowers the resistance, and hence also increasing the current. In contrast, the static I–V model behaves isothermally,

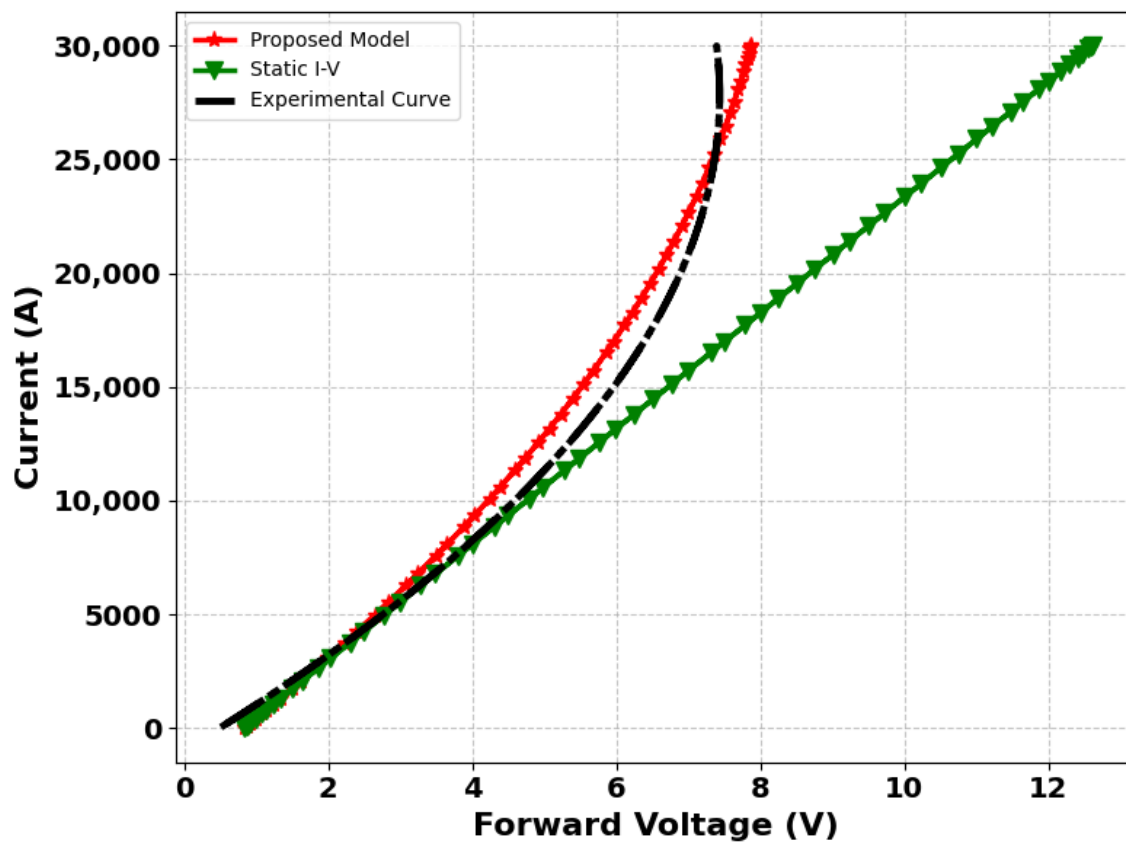


Fig. 4.8 Comparison of static, experimental, and proposed models for diode forward voltage characteristics.

neglecting the effect of increasing temperature with an increase in applied voltage, resulting in a constant slope, which lowers the differential conduction. Therefore, the model results in an underestimation of the current level for a given voltage and indicates a higher voltage level for the actual current. The difference between the actual and predicted parameters can lead to errors in optimal device design and in the selection of critical parameters such as power ratings and heat sink capacity for effective thermal management. Such oversimplification may prevent accurate identification of the underlying physical mechanisms, potentially resulting in degraded performance or even device failure. Therefore, it is very important to account for the effect of temperature in the modeling of this kind of device for the analysis and evaluation of device performance and reliability.



## 4.7 Modeling and Simulations

To evaluate temperature under the high surge levels of high-power diodes, transient thermal distribution simulations were performed using the FEM and the resistance capacitance (RC) equivalent method.

### 4.7.1 Resistance Capacitance Equivalent Method

In order to estimate the device's temperature through the R-C equivalent method, an equivalent circuit model was designed in PSIM to perform electrothermal simulations, as shown in Figure 4.1. The simulation setup consists of a surge wave generator circuit, as detailed in Section 4.2, which generates a range of peak surge currents at varying voltages, with the corresponding power dissipation summarized in Table 4.2. This study investigates a 48 mm high-power press-pack diode with a blocking voltage of 2800 V to characterize its thermal behavior. Thermal resistance and capacitance were analytically extracted from the geometric dimensions and material properties of the diode, as described in Section 3.2, and subsequently used to construct a Cauer thermal network model. The system model, as depicted in Figure 4.2, outlines the process of extracting electrical parameters by integrating experimental measurements at the rated current with thermal simulation data.

Table 4.2 Extracted parameters under different surge current conditions.

| Current (A) | Temperature (°C) | Slope Resistance $r_T$ ( $\Omega$ ) | Forward Voltage $V_F$ (V) |
|-------------|------------------|-------------------------------------|---------------------------|
| 6400        | 22               | 0.000322                            | 2.892                     |
| 8600        | 32               | 0.000318                            | 3.561                     |
| 10,800      | 50               | 0.000310                            | 4.183                     |
| 14,400      | 80               | 0.000303                            | 5.199                     |
| 16,800      | 110              | 0.000299                            | 5.848                     |
| 18,600      | 132              | 0.000294                            | 6.298                     |
| 20,400      | 152              | 0.000292                            | 6.779                     |
| 30,000      | 310              | 0.000238                            | 8                         |

### 4.7.2 Finite Element Method

To evaluate the thermal behavior and temperature of the diode under surge conditions, a three-dimensional finite element model replicating the manufacturer-specified geometry, as discussed in Section 3.2, was developed in ANSYS 2025 R2, as illustrated in Figure 4.9. The applied heat source was defined as a time-dependent power dissipation, calculated

from the product of the current and voltage, as detailed in Section 4.3, and applied directly to the silicon chip. The average chip temperature,  $T(t)$ , was selected as the primary output metric. In the simulation setup, the flux derived from power dissipation was imposed on the diode chip uniformly, while the anode and cathode were treated as convective boundaries. The ambient temperature was fixed at 22 °C. The heat conduction within the multilayer diode structure (silicon die, molybdenum, and copper) was modeled using the governing heat equation:

$$K_T \left( \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) = \rho c_T \frac{\partial T}{\partial t} \quad (4.8)$$

where  $K_T$  is the thermal conductivity,  $\rho$  is the material density, and  $c_T$  is the specific heat capacity. The applied heat flux  $q''(t)$  can be expressed as follows:

$$q''(t) = \frac{P(t)}{A_{chip}} \quad (4.9)$$

where  $A_{chip}$  is the corresponding face of the silicon chip, as discussed in Section 3.2. Convective heat exchange was applied identically to both anode and cathode surfaces with same convection coefficient and case temperature:

$$q''_{Conv} = h(T_c - T_a) \quad (4.10)$$

with  $h$  denoting the convective heat transfer coefficient,  $T_c$  denoting the case temperature, and  $T_a$  denoting the ambient temperature.

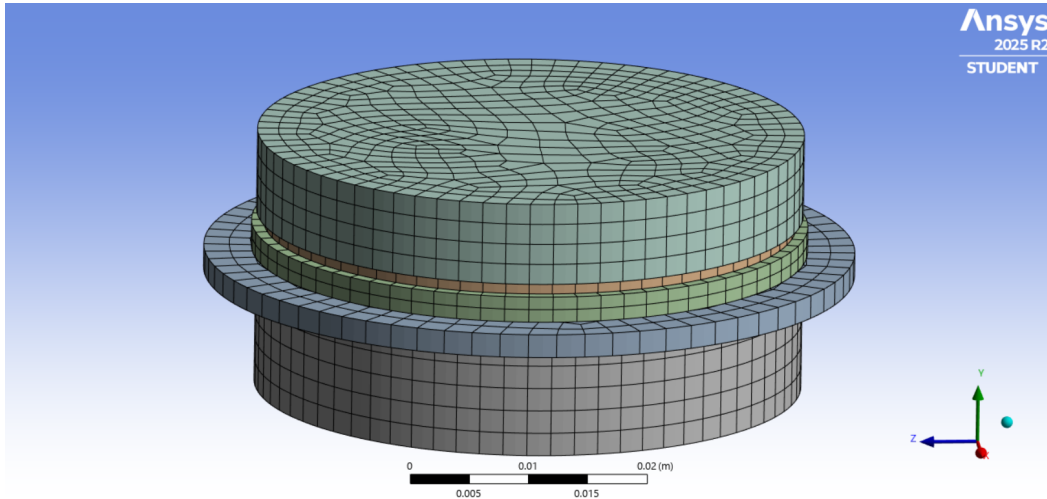


Fig. 4.9 Geometry of the diode and corresponding finite element mesh developed in ANSYS for evaluating electro-thermal behavior under high-surge-current conditions.

## 4.8 Simulation Results and Discussion

The thermal step response  $Z_{th}$  from the junction to the case is measured using the cauer thermal model discussed in Section 3.4, as depicted in Figure 4.10a. The simulation results are consistent with the experimental measurements. The simulated temperature results for different peak surge currents are presented in Figure 4.11. The results present the transient temperature rise from an ambient temperature of 22 °C for surge currents ranging from 6 kA to 30 kA. As the amplitude of the current increases, the temperature of the device

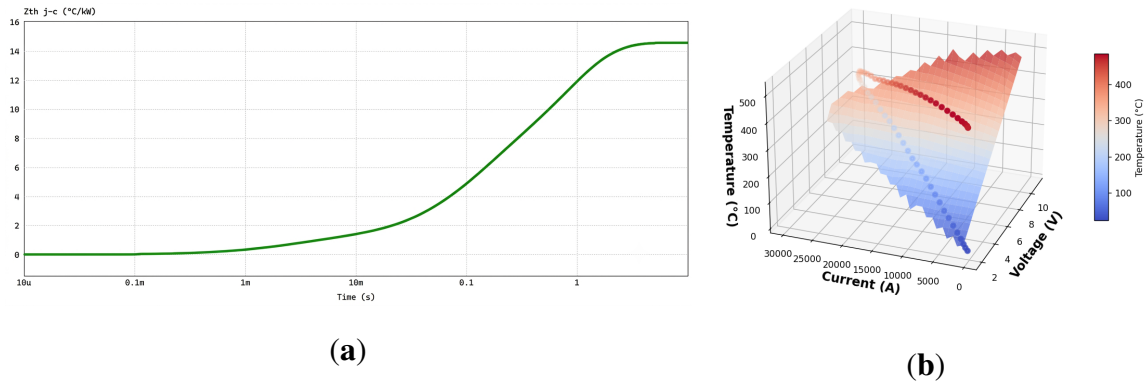


Fig. 4.10 Thermal characterization of the DUT: (a) thermal impedance versus time curve; (b) voltage, current, and peak temperature dynamics under the surge current.

also starts increasing correspondingly. The peak temperature increase, along with the surge current amplitude, following an exponential rise and fall characteristic of the device's thermal time constant. After the current reaches its peak value, the temperature still continues to increase for a few more milliseconds, indicating the presence of significant thermal lag. It is also noted that lower surge currents (6–8 kA) cool down within 10 ms, but higher current surges (18–30 kA) maintain elevated temperatures, highlighting the need for optimal thermal management to prevent potential performance degradation, device failure, and thermal runaway. The possibility of device failure, mainly initiating with metallization, increases as the temperature rises, which is directly related to the device's electrothermal response. Figure 4.10b shows the relationship between surge current, voltage, and temperature. It shows that power dissipation influences increases in temperature. At higher voltage and current levels, a sudden increase in peak temperature is noted and highlights regions of very high thermal stress. This temperature rise occurs as the device resistance decreases due to enhanced carrier activity, which further accelerates current conduction and can lead to thermal instability through localized joule heating. The influence of temperature on forward voltage is further investigated in Figure 4.12a, where the forward voltage is analyzed under consistent current

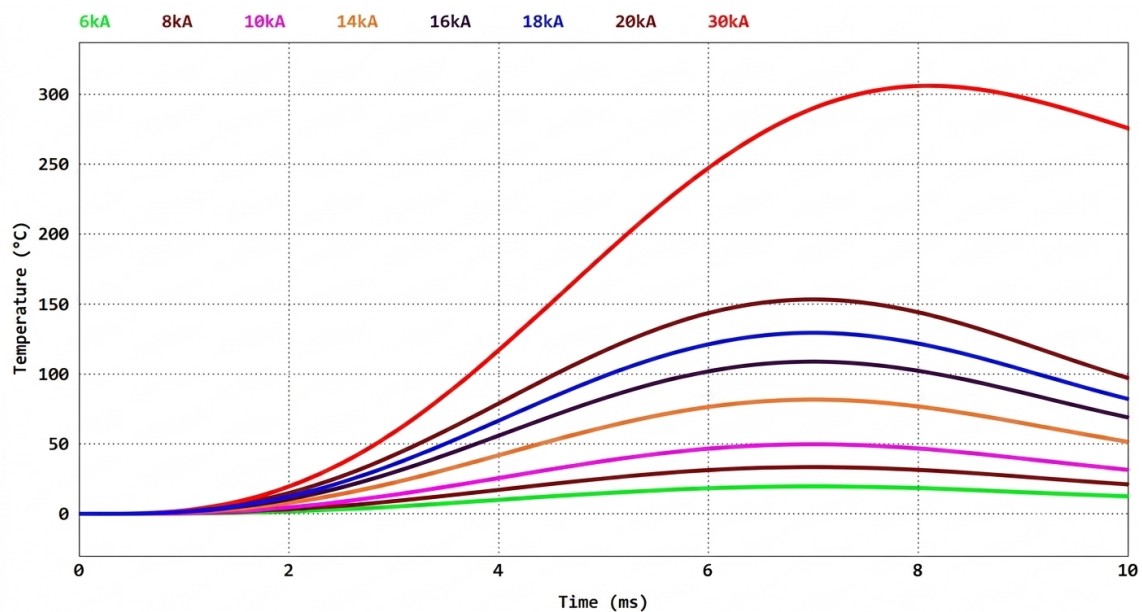


Fig. 4.11 Average temperature of the DUT obtained from simulation across multiple surge currents.

conditions at varying temperatures. Forward voltage measurements reveal that, at high current densities, self-heating effects become significant. Under fixed current conditions, joule heating raises the junction temperature, and the resulting increase in lattice scattering reduces carrier mobility, leading to a rise in the effective device resistance. To maintain the fixed surge current, the forward voltage must increase, rising from 2 V at 25 °C to 12 V at 175 °C for 30 kA. This voltage escalation results in increased power dissipation from 60 kW to 360 kW, causing a severe electro-thermal feedback loop that triggers thermal instability, defining its operational limits, leading to catastrophic failure operating beyond defined high-surge conditions. Figure 4.12b shows the time-dependent relationship of current, voltage, and temperature during a surge current. The current rises rapidly and reaches its peak value first, followed closely by the voltage, while the temperature response displays a lag due to thermal inertia. As the surge achieves its peak value, the current starts decaying; however, at high currents, the carrier mobility decreases, but carrier concentration increases more, and this leads to negative temperature coefficient regions with a behavior that is not purely linear. Meanwhile, the temperature continues to rise exponentially, driving the device toward thermal runaway. It is also examined that even when the surge current begins to decay, the voltage level remains relatively high. This behavior indicates that the current is not the only factor leading to device performance degradation and failure. Therefore, in the design of protection systems, voltage monitoring should also be taken into consideration. During the surge simulation, the device temperature increased continuously from room temperature

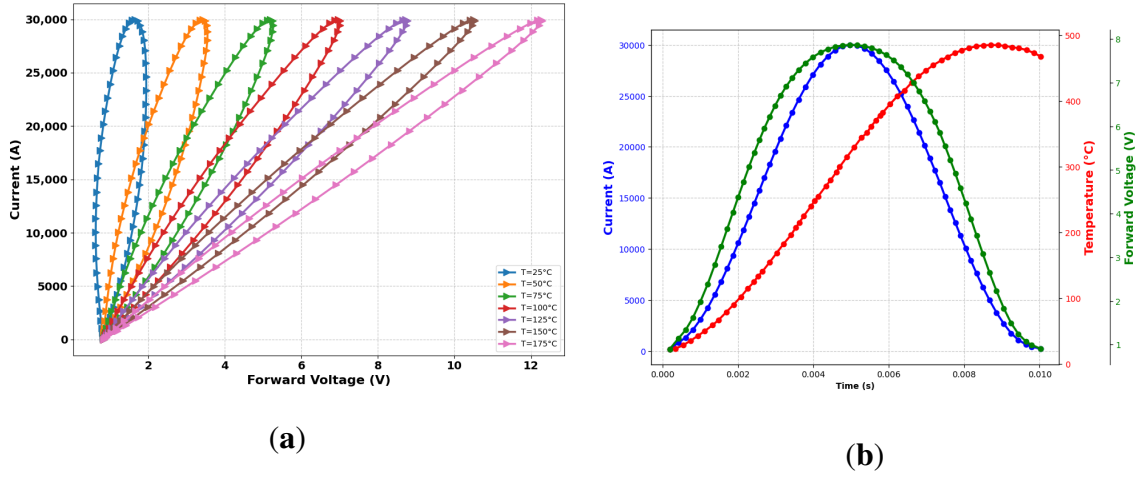


Fig. 4.12 (a) Impact of temperature on forward voltage under fixed surge current. (b) Characteristics of time evolution of voltage ( $V_F(t)$ ), current ( $I(t)$ ), and maximum junction temperature  $T_{j_{max}}(t)$

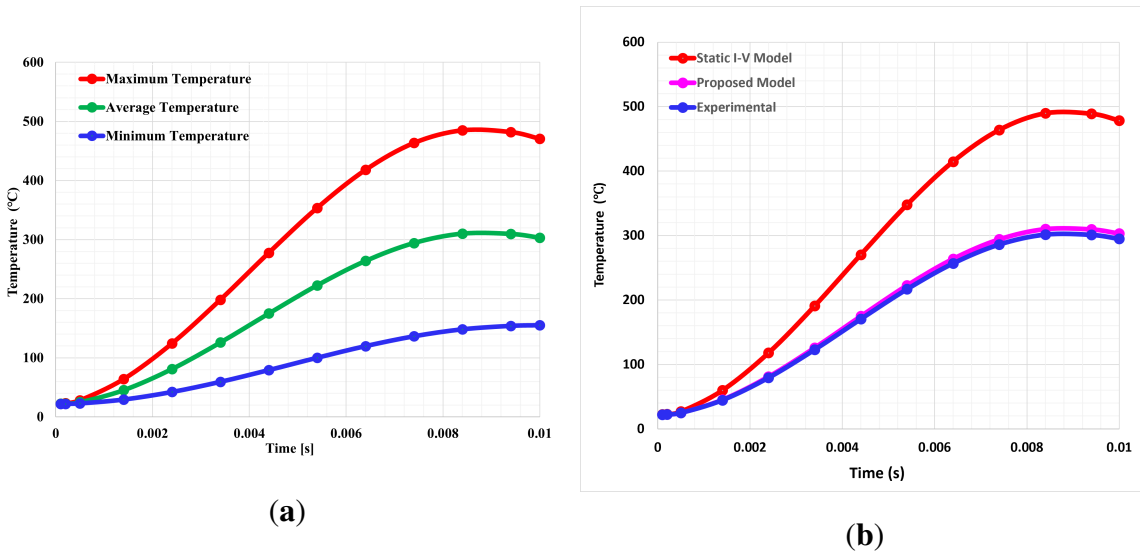


Fig. 4.13 (a) Minimum, average, and maximum temperatures estimated by the proposed model for a surge current. (b) Average temperature comparison: proposed model vs. experimental data and static I–V model.

at lower current levels to significantly higher values as the current increased, leading to a corresponding variation in the voltage drop across the device. At a surge current of 30 kA, the maximum chip temperature reached approximately 485 °C, while the average temperature was about 310 °C, as illustrated in Figure 4.13a. Although the maximum temperature of the diode approached its upper thermal limit at 30 kA, no degradation in blocking capability

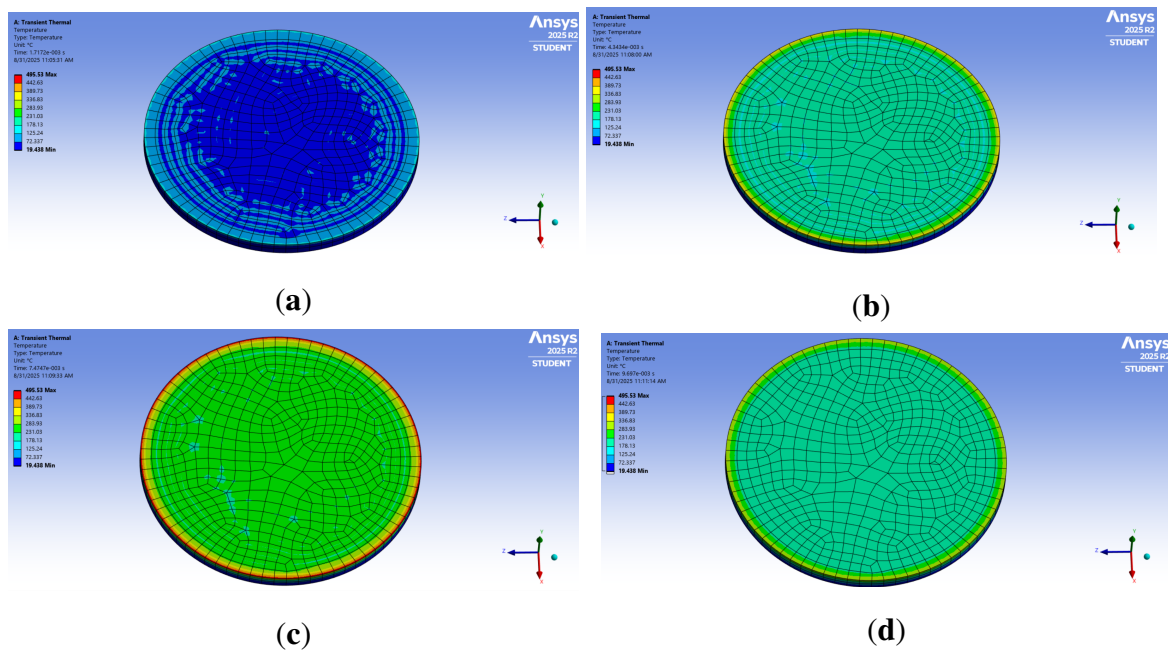


Fig. 4.14 Temperature distribution in the silicon chip under the surge current at different time instances: (a) 1 ms, (b) 4 ms, (c) 7 ms, and (d) 9 ms.

was observed during the intermediate measurements. The simulated maximum temperature of 485 °C occurred at 8 ms, whereas the maximum surge current was observed at 5 ms, as illustrated in Figure 4.13a. This thermal delay is attributed to continuous Joule heating and thermal inertia, where power dissipation persists even after the peak current has passed. Although power loss begins to decrease after 5 ms, residual thermal energy and the finite thermal diffusivity of materials cause a delayed temperature peak. Figure 4.13b shows the transient temperature obtained from power dissipation based on each model's voltage output. The static I–V model deviates significantly from the experimental reference due to its inability to capture accurate voltage, resulting in inaccurate thermal estimation. In contrast, the proposed model closely matches the experimental results, which confirms its accuracy and ensures reliable voltage prediction. The temperature distribution, as shown in Figure 4.14, indicates that the maximum temperature occurs within the silicon chip, and peak values occurs at the edges, as also shown in Figure 4.15. Moreover, the heat flux distribution across the silicon chip is shown in Figure 4.16. A persistent hotspot remains localized throughout the transient response. At earlier points, the chip is relatively cool; however, as time progresses, the high-flux region expands laterally, reflecting the propagation of thermal energy driven by localized power dissipation that is strongly influenced by the device's structural and electrical properties. Figure 4.17 compares the estimated junction temperature obtained using the 3-D RC equivalent circuit in PSIM and the FEM-based simulation in ANSYS. Both methods



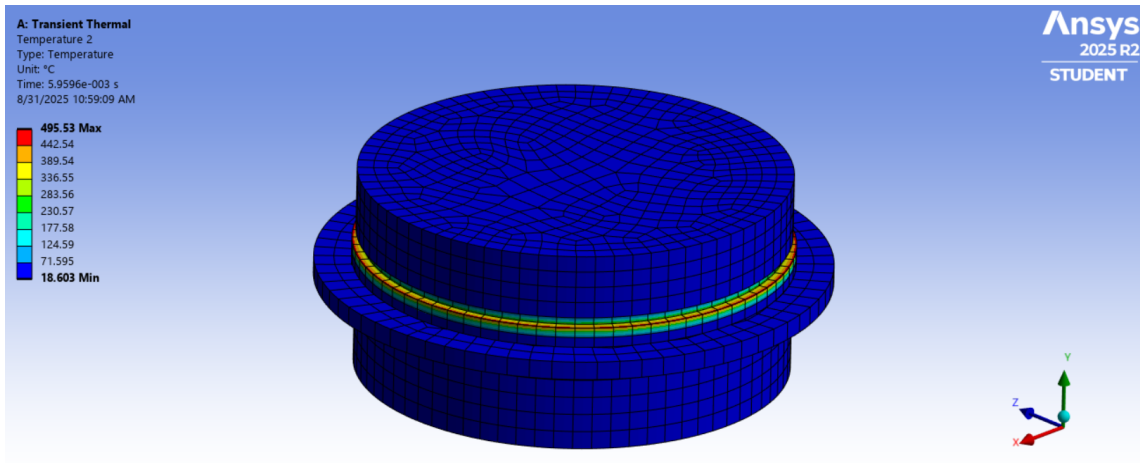


Fig. 4.15 Temperature distribution across the entire device under the surge current.

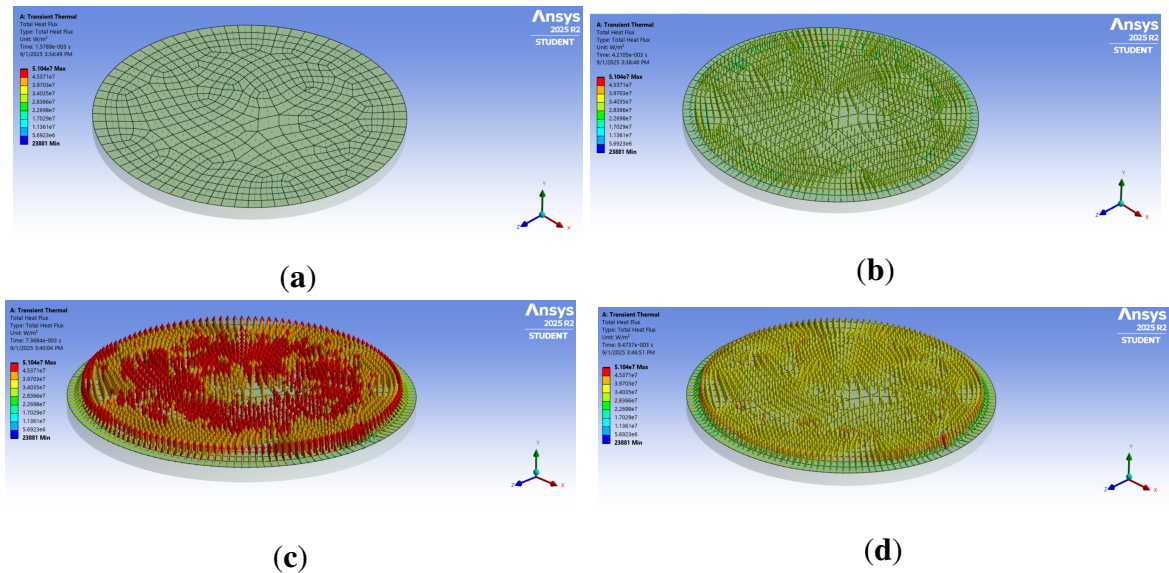


Fig. 4.16 Heat distribution in the silicon chip under the surge current at different time instants: (a) 1 ms, (b) 4 ms, (c) 7 ms, and (d) 9 ms.

show excellent agreement in predicting the maximum temperature and its occurrence time. A minor discrepancy is observed at the beginning of the transient, which arises because the FEM simulation initializes at 22 °C, which is a slightly higher temperature than that in the initial condition assumed in the RC model.

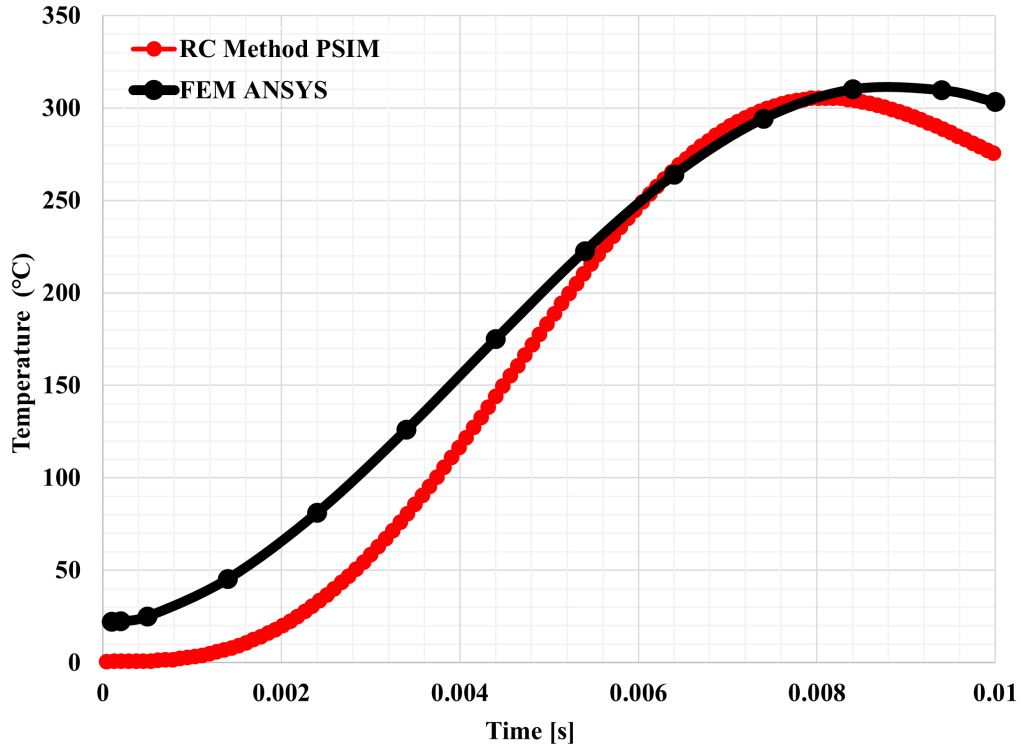


Fig. 4.17 Comparison between the junction temperature estimated using the RC equivalent circuit in PSIM and the FEM-based simulation in ANSYS.

## 4.9 Limitations

In this chapter, an electro-thermal model is proposed to estimate the forward voltage and evaluate junction temperature of the device. However, this study does not address the analysis of failure mechanisms under high surge current conditions. In addition, the influence of different packaging technologies on device reliability is also not considered. These limitations are addressed in the following chapter.

## 4.10 Conclusion

In this chapter, an electrothermal model is proposed to estimate junction temperature for high-power diodes. The proposed model integrates electrical parameters at the rated current with thermal simulation data to estimate forward voltage and slope resistance characteristics under surge conditions. In order to verify the accuracy of the proposed model under various surge conditions, a number of experimental tests were conducted, showing that the estimated forward voltage of the diode matched the experimental results. Moreover, simulations were



performed to estimate the device's temperature at respective current levels in PSIM and ANSYS. The results accurately capture the nonlinear thermal–electrical behavior, providing valuable insights into device thermal limits and supporting the improved design and reliability assessment of high-power systems.

**Publication Related to this Chapter**

This chapter reproduces material from the following publication:

**F. Ahmad**, L. Vaccaro, A. A. Nkembu, M. Marchesoni, and F. Portesine, “*Surge Current Analysis of High-Power Press Pack Diodes: Junction Temperature and Forward-Voltage Modelling*,” **Electronics**, vol. 14, no. 24, p. 4899, Dec. 2025.  
DOI: [10.3390/electronics14244899](https://doi.org/10.3390/electronics14244899)



# Chapter 5

## Comparative Analysis of Surge Reliability and Failure Mechanisms in Press-Pack and Insulated Module Diodes

This chapter introduces the impact of packaging technology on surge reliability and failure behavior of power semiconductor devices. Section 5.2 presents the structural and packaging differences between press-pack diodes and insulated module diodes. In Section 5.3 the experimental test methodology used to evaluate device performance under surge current conditions are discussed. Moreover, the experimental results focused on the electrical and thermal responses of the devices during surge events are discussed in Section 5.4. Section 5.5 outlines the numerical acquisition and data processing methods used to analyze the measured waveforms. In addition, Section 5.6 describes the simulation setup, including the modeling framework and boundary conditions used for thermal analysis and the simulation results and junction temperature comparison are subsequently presented in Section 5.7. Section 5.8 analyzes the failure mechanisms and reliability aspects associated with different packaging technologies, followed by the limitations of the study in Section 5.9, and finally, Section 5.10 summarizes the main conclusions of the chapter.

### 5.1 Overview and Research Motivation

The increasing demand for high power densities in these applications has motivated manufacturers to develop advanced power semiconductor devices with improved designs and new packaging techniques to optimize power dissipation to meet the required power ratings. However, the increase in current beyond the limits may trigger more power, which may increase

the temperature and result in inducing electro-thermal and associated stresses in the device. [144, 292]. Therefore, accurate estimation of the junction temperature is essential to optimize power dissipation and avoid performance degradation, improve reliability, and increase lifespan by ensuring operation within specified thermal limits. Among many other factors influencing thermal resistance and impedance, including material composition, geometry, and contact surface quality, the junction temperature can be optimized through appropriate device architecture and packaging design as shown in Table 5.1, alongside effective thermal management.

Table 5.1 Technology aspects of high power semiconductor devices.

| Technology                  | Assembly Type              | Chip Structure                  | Devices               | Advantages                                                                                                                                    | Disadvantages                                                                                                                                    |
|-----------------------------|----------------------------|---------------------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| PCT technology              | Press pack ceramic housing | Monolithic, Silicon Round Shape | Diode, Thyristor      | Double side cooling. Low junction temperature at same dissipated power. Very high reliability. Hermetic encapsulation no degradation          | Requires precise clamping force; limited packaging flexibility; larger footprint                                                                 |
| PCT technology              | PCT insulated modules      | Monolithic, Silicon Round Shape | Diode, Thyristor      | High reliability. Electric insulation from heat sink                                                                                          | Single side cooling. High junction temperature at same dissipated current. Encapsulation with resin possibility of degradation                   |
| Brazing and welding contact | Insulated module           | Multi-chip, Square Shape        | Diodes, IGBT, MOS-FET | High modularity multichip connection in parallel. Lower costs at same power range. Possibility of use different type of devices including SiC | Single side cooling High junction temperature at same dissipated current. Lower reliability. Encapsulation with resin possibility of degradation |

High-power semiconductor devices have traditionally been implemented using insulated module-based architectures as illustrated Figure 2.7, using brazing and welding contact technology, where semiconductor chip and multiple layers of various materials (Si, AlN, AlSiC, Copper) are connected together and external electrodes via soldering and welding wires. However, this packaging approach supports only low- to medium-current operation because heat ( $Q$ ) flows through a single conduction path from the chip to the heat sink before being dissipated to the ambient  $Q_w$ . This limited thermal pathway reduces reliability, and long-term operation is often compromised due to degradation mechanisms such as bonding wire lift-off and solder joint cracking, which lead to performance degradation and eventual device failure [142, 143].

In these devices, multiple layers are stacked together by clamping force, ensuring direct electrical and thermal contact without the need for wire bonds or solder joints. Moreover, in switching devices, such as thyristors and IGBTs, etc., the gate connections to the terminals are replaced by gate springs. The gate springs make them more reliable and robust to performance degradation and failure. The insulated module assemblies commonly employ monolithic, silicon, round-shaped diodes and thyristors. This configuration enhances the

device's reliability and supports medium to high current ratings while reducing the risk of failure by eliminating soldered interconnections. For applications with very high currents, the use of PCT in the press-pack ceramic housing designs further improves the reliability and thermal performance. This configuration enables two-sided cooling, supported by heat sink A and heat sink B, with corresponding heat dissipation paths  $Q_{wa}$  and  $Q_{wb}$  respectively, as depicted in Figure 2.9. However, increased current levels  $I_T$  from anode (A) to cathode (K) beyond the limits can make all these packaging configurations susceptible to failures such as fretting damage, micro-eroding, and spring fatigue. Additionally, press-pack devices lack encapsulation, decreasing the risk of chip rupture and explosion under fault conditions. The failures are primarily driven by excessive junction temperatures caused by surge currents and thermal cycling, inducing thermo-mechanical stresses that ultimately compromise device reliability [144]. In the existing literature, the surge current capability of power devices is typically evaluated at relatively low current levels ranging from several amperes, such as 50 A [113], 110 A [114] and 400 A [115] to few hundred amperes, 1200 A [116] and 1500 A [117]; which is insufficient for practical high-power applications, where devices results in very high fault currents (several kA), leading to high temperature rise and overheating. Therefore, it is essential to assess surge current limits at significantly higher levels to ensure reliable operation. The main contributions of this chapter are summarized as follows:

- A comparative analysis is conducted between a PCT press-pack diode and a diode module, both having identical silicon chip dimensions, electrical specifications, and power ratings, under high-surge current conditions.
- A 10 ms high half-sine surge current waveform generator is developed both experimentally and in PSIM to analyze surge events at different power levels for both diode packaging types.
- Simulations were performed to estimate Junction temperatures by utilizing measured currents and voltages.
- The estimated junction temperature are evaluated by electro-thermal model in order to study behavior of device during high-stress surge conditions.
- Failure mechanisms and thermal limitations are investigated to assess the robustness and surge current handling capabilities of both diode technologies.
- The findings offer practical guidance on the thermal-electrical trade-offs between press-pack and module diodes for use in high-power applications.

## 5.2 Press-Pack and Insulated Module Diodes

A typical power semiconductor packaging design, for high power PCT insulated module diode and advanced PCT press pack ceramic diode, consists of a multilayer structure with different materials, as shown in Figure 5.1. These configurations are analyzed and compared

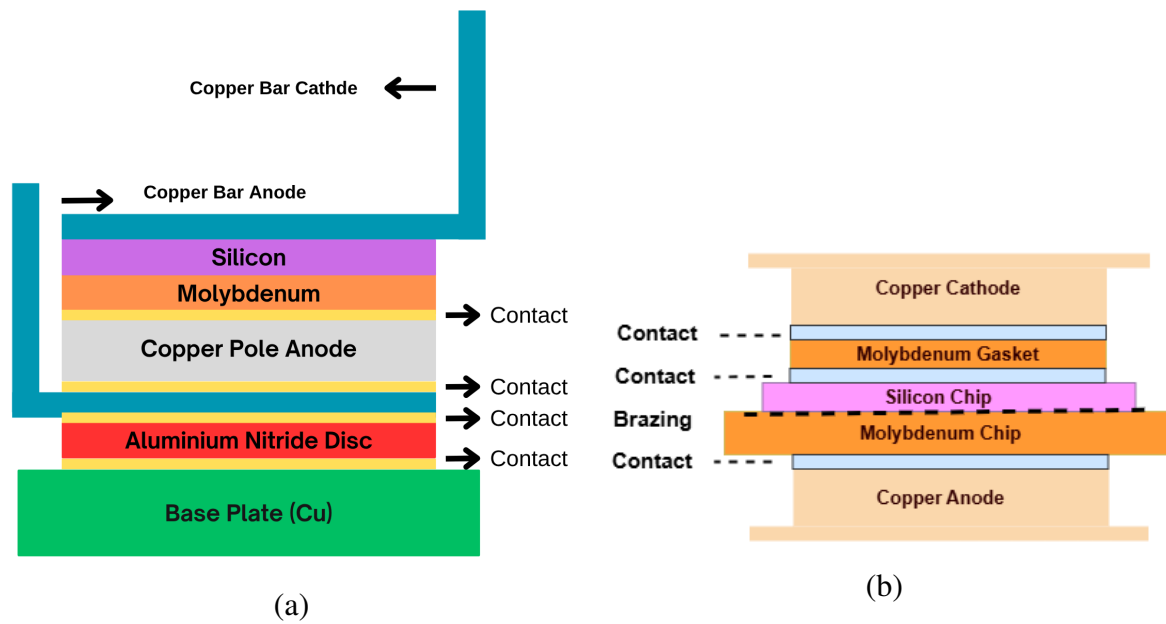


Fig. 5.1 Device structure (a) PCT insulated module diode (b) PCT press pack diode.

the thermal performance of different packaging designs under higher current events with extreme thermal conditions. The insulated module diode structure consists of a silicon chip interfaced with copper anode and cathode electrodes via molybdenum contact layers to optimize electrical and thermal performance. Copper reinforcement bars are employed at both electrode terminals as depicted in Figure 5.1 (a) to ensure the flow of current from anode towards junction. On the anode side, an aluminum nitride disc is also incorporated between the reinforcement bar and the copper base plate, enabling the electric isolation, to avoid any electric discharge from the chip and any other metallic part to the base plate. The cathode side mirrors the anode architecture, maintaining the copper reinforcement bar to ensure electric current symmetry, but omitting the aluminum nitride disc. In contrast, press-pack diodes interface the silicon junction with the copper anode and cathode electrodes through intermediate molybdenum layers as shown in as depicted in Figure 5.1 (b). However, they lack copper reinforcement bars and aluminum nitride discs and rely on brazed joints between the silicon chip and molybdenum layers to achieve mechanical stability. The device exhibits a symmetrical heat dissipation pattern, with heat generated at the center and propagating equally toward the anode and cathode sides. Heat flow from the silicon junction to the

external terminals is influenced by various factors including, thermal properties, geometry, and dimensions of the adjacent layers. Thus, the generated heat ultimately dissipates to the ambient environment through the device case and heat sink. Furthermore, the overall thermal capability in both assemblies are significantly influenced by the thermal contact resistances at each material's interface, where mismatches in material properties introduce additional thermal barriers.

### 5.3 Experimental Test

Experimental tests were carried out on a PCT press-pack diode and a PCT insulated diode model, both from the same manufacturer and unused, with  $V_{RRM}$  ratings of 4400 V and 4500 V, respectively. The devices had similar specifications and featured chip diameters of 48 mm. The experimental setup, designed in accordance with the IEC 60747–2 standard [68], illustrated in Figure 4.4, is designed to generate controlled surge current pulses using a single-phase full-wave rectifier connected to a transformer  $Tx_1$  via a resistor  $R_1$  and an inductor. The surge current, as shown in Figure 5.2, ranging from 6400 A to 36700 A, is generated through a resistor-capacitor (RC) charge–discharge mechanism.

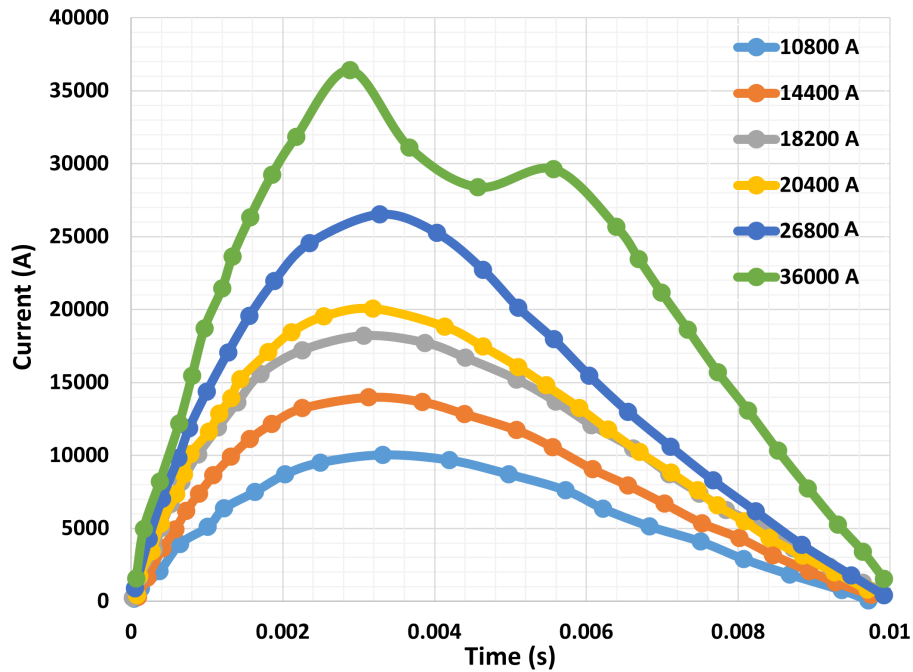


Fig. 5.2 Surge current waveforms for the performed experimental surge tests.

## 5.4 Experimental Results

A series of surge current tests were performed experimentally as detailed discussed in Section 4.4.1. The test was started at a lower level current having peak amplitude of 6.4 kA and gradually increased up to device failure. For each surge level, the corresponding forward voltage drop was recorded to monitor the electrical response of the device, as shown in Figure 5.3 and 5.4. After the surge test, electrical tests were carried out that confirmed that the diode's electrical characteristics were only slightly changed compared to prior characteristics, confirming no performance degradation or failure in the device. Furthermore, the PCT press-pack diode demonstrated robust performance under high surge

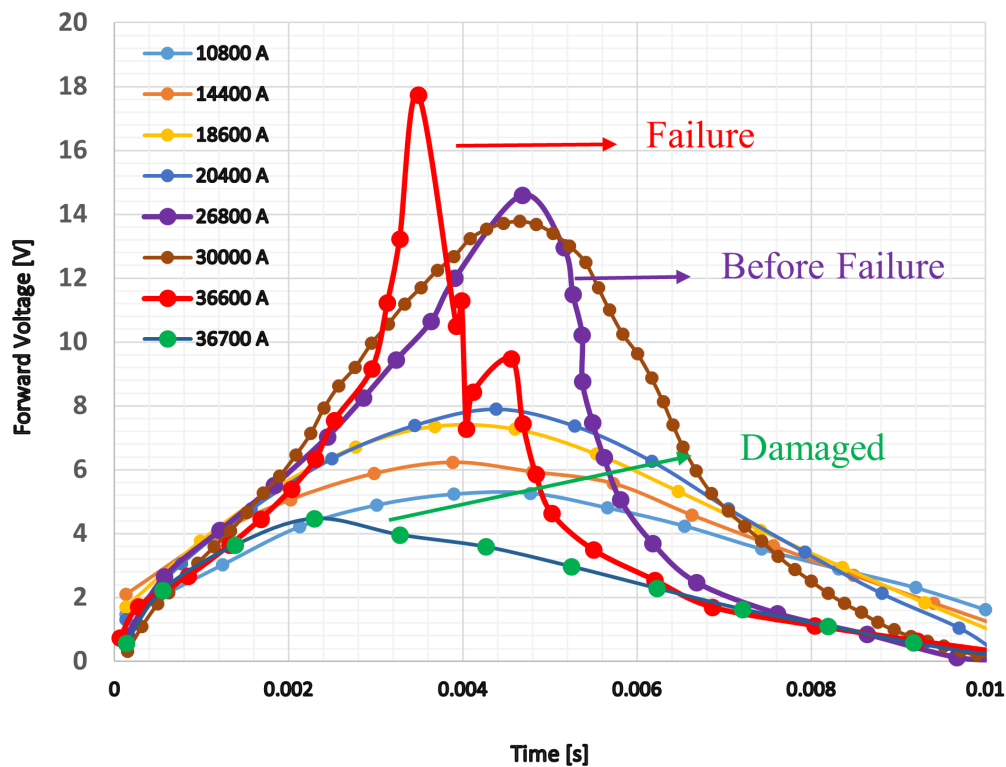


Fig. 5.3 Measured voltages for PCT press pack diode.

current conditions, withstanding peak currents of up to 36 kA, approximately 11 times its nominal current rating, without failure. However, irreversible failure was noted after this, thereby defining the threshold of surge current under the specified test parameters. Moreover, prior to device failure, at a surge current of 30 kA, metallization of aluminum nitride was observed, indicating the start of performance degradation. Moreover, prior to device failure, at a surge current of 30 kA, metallization of aluminum nitride was observed, indicating the



start of performance degradation. The module diode, on the other hand, showed metallization evaporation at 26.8 kA, while a chip failure occurred at a lower current level of 30 kA. These

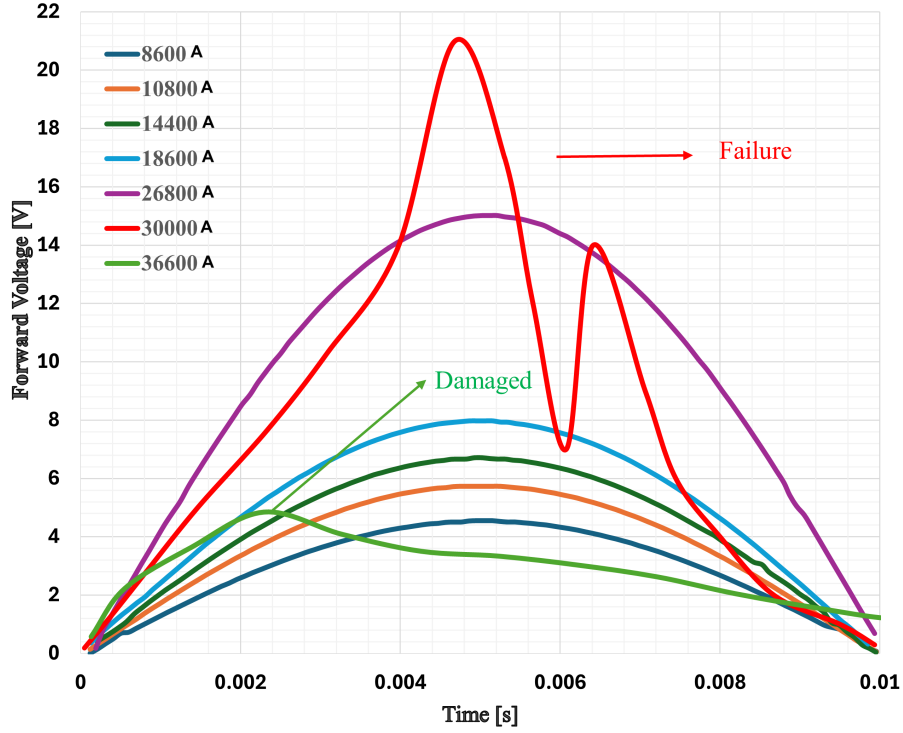


Fig. 5.4 Measured voltages for diode module for corresponding surge currents.

results show that the PCT device is capable of handling better surge current than the module diode. Additionally, it also provides critical insight into their respective failure mechanisms under higher surge current as discussed in Section 5.8. These results clearly demonstrate that the module diode exhibits higher thermal resistance, resulting in a greater voltage drop and a more rapid temperature rise, as a result of its limited power dissipation capability, and thereby reliability of device at higher current levels are compromised.

## 5.5 Numerical Acquisition and Processing

The current and voltage waveforms, recorded by a digital four channel oscilloscope during the experimental tests, represented in Figure 5.5 and detailed discussed in Section 5.4 were exported as numerical datasets. These waveforms were subsequently imported into Python for quantitative analysis and preliminary power calculations as shown in Figure 5.6 (a). The instantaneous power, capturing both the peak values and the total pulse energy, can be given

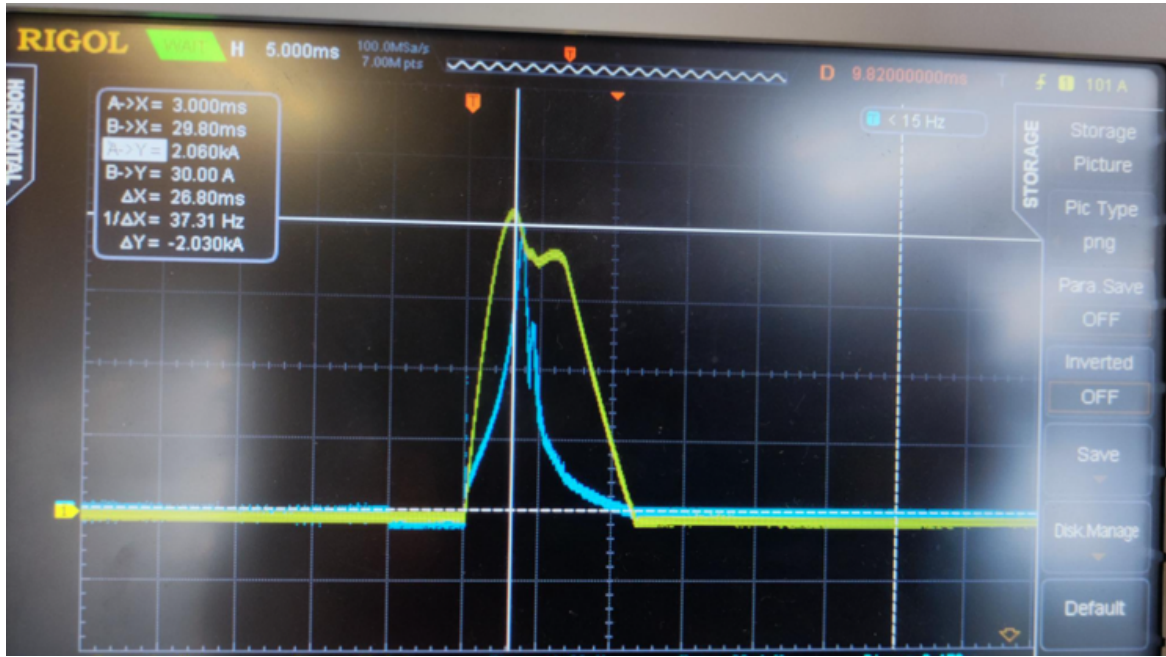


Fig. 5.5 Current and voltage waveforms recorded during the experiment using an oscilloscope. The yellow traces represent the surge current, while the teal traces correspond to the forward voltage.

as follows;

$$P(t) = V(t) \cdot I(t) \quad (5.1)$$

The resulting time-dependent power profiles were then used as inputs for the thermal model described in Section 5.6, enabling accurate prediction of the transient temperature evolution under the same operating conditions as the experiment. The instantaneous power can be modeled as

$$P(t) = P_0 \sin\left(\frac{\pi t}{T}\right) \left[ 1 - \beta \exp\left(-\frac{(t-t_0)^2}{2\sigma^2 t/T}\right) \right] \quad (5.2)$$

where  $P_0$  is the peak amplitude of power,  $T$  is the total pulse duration and  $t$  is the instantaneous time at which power is evaluated. The first term  $\sin(\pi t/T)$ , represents the fundamental sinusoidal behavior of the surge waveform over the time period  $T$ . Moreover, the second term introduces a Gaussian dip, implemented as an exponential modulation, which locally attenuates the power around  $t_0$ .  $t_0$  is the time shift that indicate the occurring time of dip. The attenuation coefficient  $\beta$ , control the depth of dip while its temporal spread is determined by  $\sigma$ . This expression captures deviations from an ideal sinusoidal surge, accounting for non-ideal damping and transient thermal-electrical interactions, thereby providing a power profile that closely matches experimental results, as shown in Figure 5.6 (b).

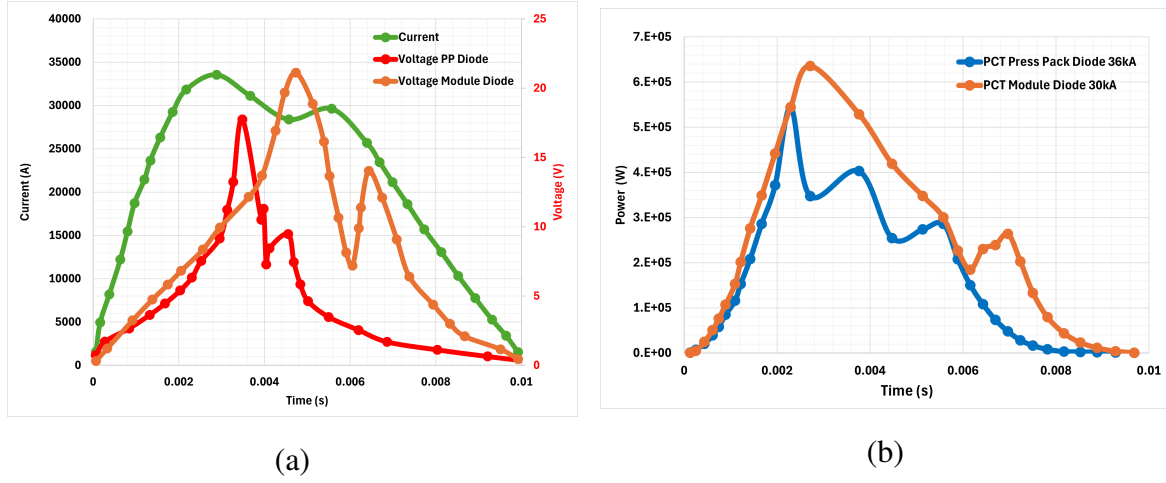


Fig. 5.6 Parameter waveforms during surge operation: (a) Measured current and voltage waveforms, (b) Acquired time-dependent power based on corresponding electrical parameters.

## 5.6 Simulation Setup

To investigate failure behavior, the transient thermal distribution of the DUT is simulated using PSIM software [293] as discussed in Section 4.7. The simulation setup includes a surge wave generator circuit, as illustrated in Figure 4.2, which produces a peak surge current of 36 kA. The generated power is applied to the DUT to monitor its thermal response and assess junction temperature variations and thermal stress. Simulations are constrained to the experimentally measured failure thresholds to ensure simulation accuracy with physical device limits. Simulation is terminated once these limits are reached in order to avoid generating non-physical data beyond the onset of destructive behavior. Failure mechanisms are then evaluated based on the electro thermal behavior of device.

## 5.7 Simulation Results and Junction Temperature Comparison

A transient thermal simulation were performed for both PCT press-pack diode and diode module to evaluate the temperature rise under various single half-sine peak current pulses. The simulation parameters are described in Table 5.2 and represented in Figure 5.7. The peak current amplitude was progressively increased until thermal runaway and subsequent device failure were observed. The results indicates that while the increase in temperature remains moderate at lower current for both devices, the diode module experiences a significantly

Table 5.2 Comparison of electrical and thermal characteristics: Press pack vs module.

| Peak Current (A) | Peak Voltage (V) |        | Peak Temperature (°C) |        |
|------------------|------------------|--------|-----------------------|--------|
|                  | Press Pack       | Module | Press Pack            | Module |
| 6400             | 3.6              | 3.85   | 42                    | 44     |
| 8600             | 4.4              | 4.5    | 55                    | 58     |
| 10800            | 5.4              | 5.7    | 72                    | 77     |
| 14400            | 6.2              | 6.7    | 102                   | 112    |
| 18600            | 7.4              | 8      | 152                   | 162    |
| 20400            | 7.8              | 8.9    | 174                   | 197    |
| 26800            | 13.8             | 15     | 347                   | 390    |
| 30000            | 14.6             | 21     | 427                   | 632    |
| 36600            | 17.7             | 4.8    | 597                   | -      |
| 36700            | 4.4              | -      | -                     | -      |

steeper temperature increase compared to the press-pack diode, especially at higher current level. In particular, for the PCT press-pack diode, the junction temperature of 427°C is reached at a peak current of approximately 30 kA. Beyond this, evaporation of metalization begins, resulting in cracking of silicon chip at a junction temperature of around 597°C with a peak current of 36.6 kA. In contrast, the failure of module diode occurs much earlier, the maximum junction temperature i.e., 390°C reached at only 26.8 kA of current, and silicon cracking was observed at approximately 30 kA. These simulation results clearly demonstrate

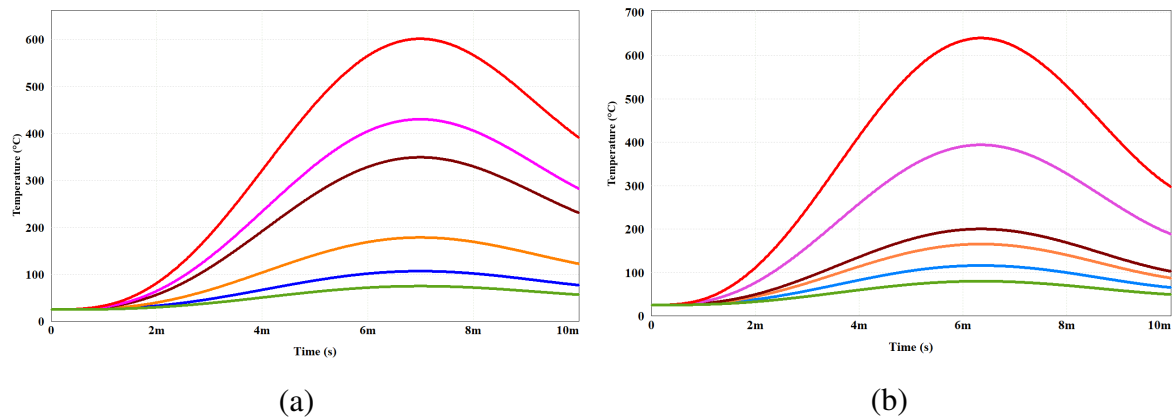


Fig. 5.7 Temperature under different surge peak (a) Press pack diode (b) Diode module.

that the diode module has inferior thermal performance compared to the press-pack diode. The single side current flow and presence of additional aluminum nitride support bars within the module package increase the thermal resistance of module, resulting in inefficient heat dissipation, leading to reduced thermal capability. The corresponding data of current and

temperature are presented in Figure 5.8, this time as a function of the forward voltage rather than time. This alternative representation highlights the impact of temperature rise on the forward voltage drop and, consequently, on power dissipation of device. As the junction temperature of device increases, the dynamic resistance also increases until device failure, leading to a higher forward voltage drop as shown in Figure 5.9 (a) and 5.9 (b). This, in turn, causes an increase in power dissipation (the product of forward current and voltage), thereby accelerating the temperature rise, leading to a typical mechanism of thermal runaway. Figure 5.9 (b), corresponds to the diode module, clearly illustrate this effect: despite identical current pulse shapes and device ratings, the forward voltage of the module is noticeably higher compared to the press-pack diode. This increased forward voltage is directly linked to the elevated junction temperature. This behavior arises from differences in current distribution, double-sided in press-pack devices and single-sided in modules, as well as the additional presence of the AlN disc in modules, which substantially exacerbates the risk of thermal runaway.

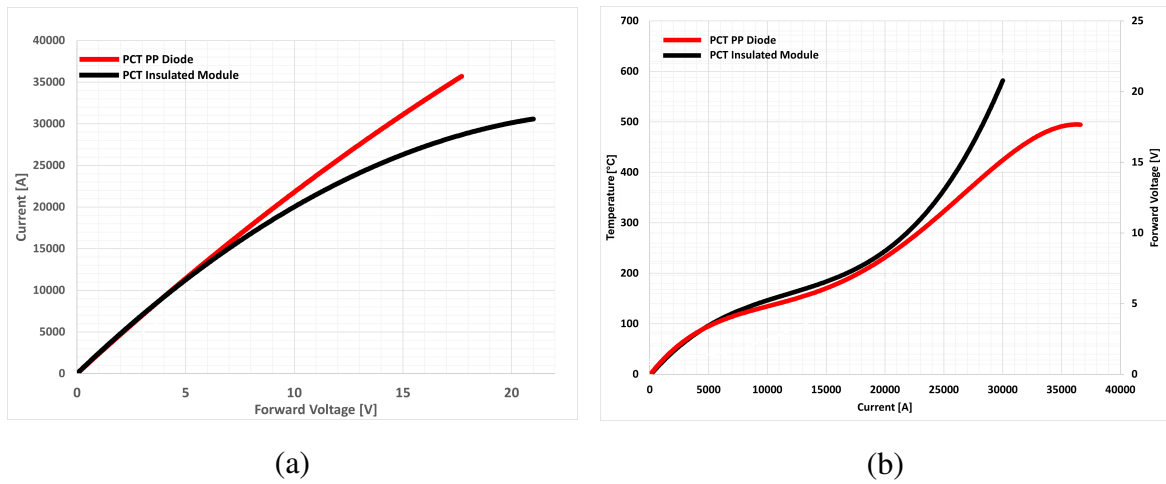


Fig. 5.8 (a) Surge trajectory, I-V curve (b) V-T, I-T and  $T_{max}$ .

## 5.8 Failure Mechanisms and Reliability Assessment

After subjecting the DUT to surge current stress and performing experimental tests, the failure mechanisms under two different scenarios were analyzed. In the case of press pack diodes, device failure, micro-eroding, is primarily attributed to heating induced by the high surge current. As the surge current begins to increase, the concentration of carriers is also increased, that in turn increase the forward voltage drop of the device and hence the temperature is also increased. With further increase of surge peak, the concentration of carriers are increased,

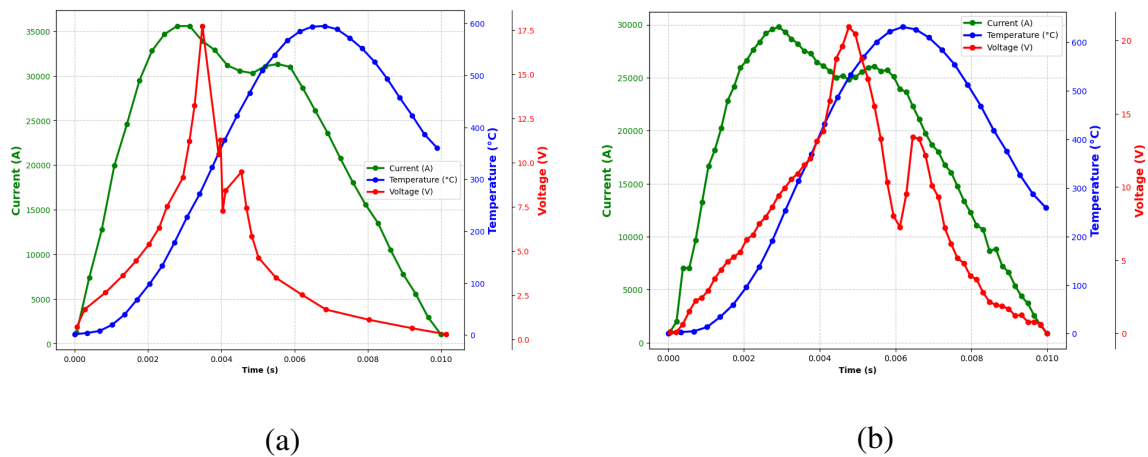


Fig. 5.9 Surge trajectory and I-V curve, V-T, I-T and  $T_{max}$  (a) Press pack PCT (b) PCT module.

which results in effecting the mobility of carriers, and hence the slope of I-V curve is slowly reduced. However, the change in the forward voltage drop of the diode remains linear until the 30 kA surge current is applied. When subjected to a 30 kA surge current, the forward voltage drop of diode increases from 7.4 V to 13.8 V, and a minor change in the shape of waveform is also noted. Moreover, sharp falling time and the evaporation of metalization is noted on the silicon chip as shown in Figure 5.10. When subjected to a surge current of 36

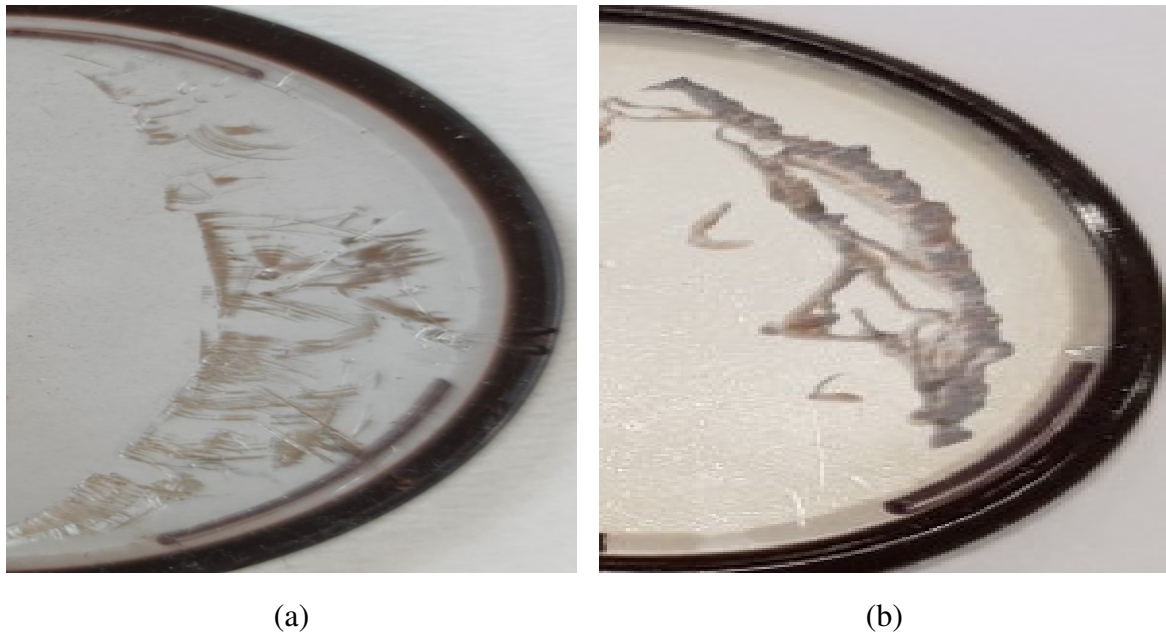


Fig. 5.10 Impact of evaporation of metal on silicon chip (a) Press pack diode (b) Module diode.



kA, the voltage drop increases to approximately 17.7 V. Notably, the 2 peak voltages occurs i.e., at 3 ms and 5 ms, which is significantly earlier than the typical 4 ms peak observed under lower stress conditions. This shift leads a nonlinear relationship between forward voltage and junction temperature at high current levels. The reduction in voltage can be attributed to an increased internal resistance caused by non-uniform current conduction. This non-uniformity results from localized damage or failure within the device, i.e, evaporation of metallization and cracking of silicon chip, which disrupts the normal conduction and degrades overall device performance. Upon unpacking the device, it is noted, molybdenum

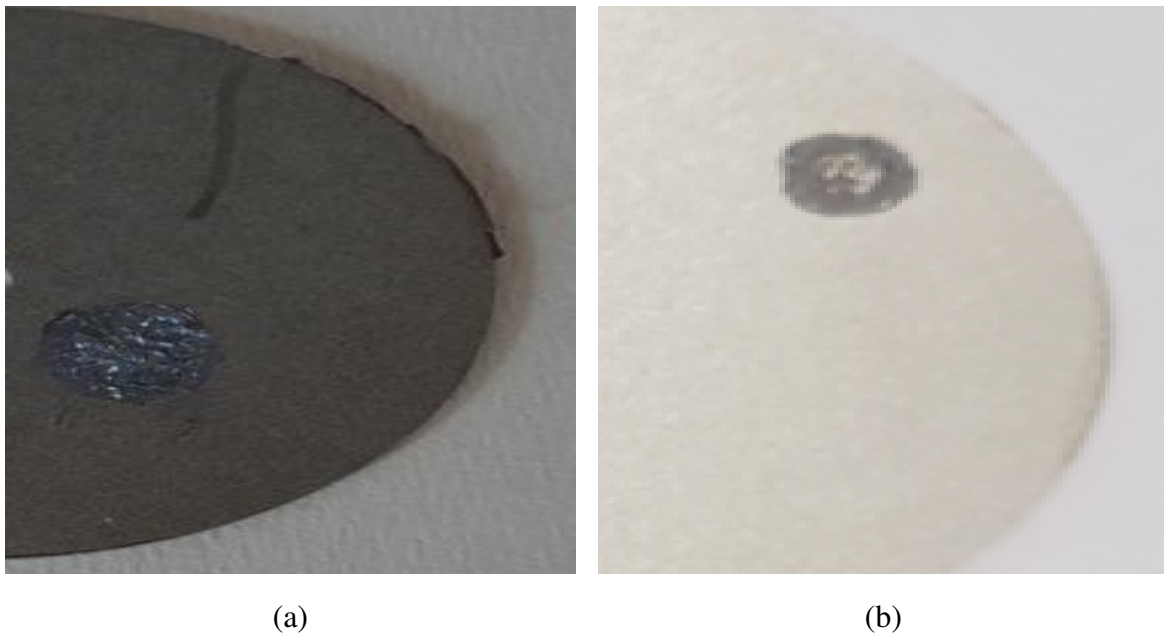


Fig. 5.11 Impact of surge on molybdenum (a) Press pack diode (b) Module diode.

is damaged as shown in Figure 5.11, and attached to the silicon chip, by detaching, a rupture was observed at the outer edges of the molybdenum and silicon die, as shown in Figure 5.12. Consequently, device performance is degraded; however, the silicon chip remains partially functional, defining the limit of forward voltage and maximum junction temperature.

At peak amplitude of 36 kA, the high surge current leads to elevated temperature, which is a typical phenomenon for failure. In addition to this, the chip at an elevated temperature exhibits a large strain and localized current at the beginning due to the increased concentration of carriers. As there is barrier to the free movement of carriers, the temperature continues to rise, there is a high possibility for the newly induced strain to give rise to chip breakage as shown in Figure 5.13 (a). The higher defect densities in the chip with this kind of failure can be originated from the thermal stress on the Si. As a result, the higher defect density contributes to the more concentrated heat distribution locally during surge current. It leads to

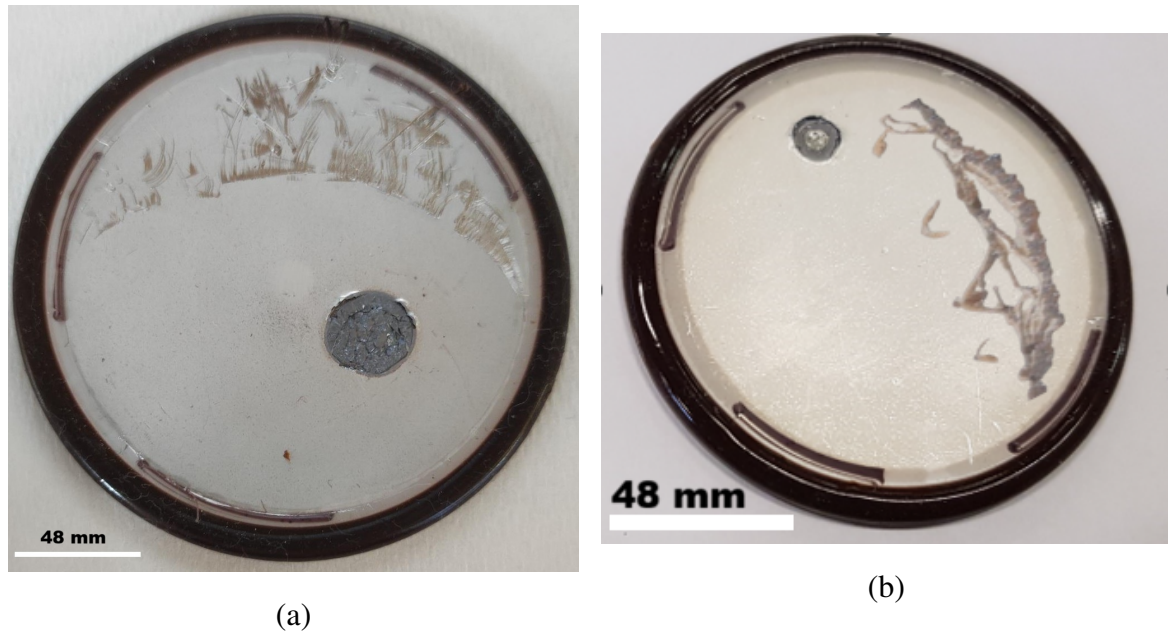


Fig. 5.12 Failure of silicon chip (a) Press pack diode (b) Module diode.

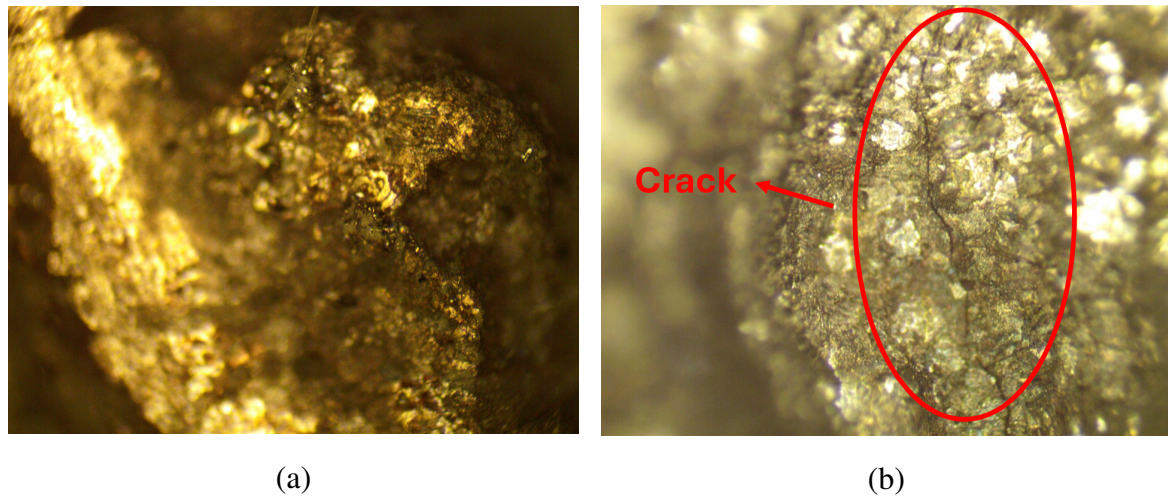


Fig. 5.13 Optical microscope images showing failure of silicon chip after surge test (a) With no crack at sides. (b) With crack at center.

more thermal stress thereby reducing the mechanical strength of chip. Thus, the breakage of the chip appears at the place where its defect states or residual stress is high as shown in Figure 5.13 (b). This result also indicates the surge current failure is closely connected to Si substrate quality. Moreover, it is noted that, although the module diode exhibits significantly higher thermal resistance compared to the PCT diode, the thermal resistance over a 10 ms pulse shows minimal difference as shown in Figure 5.14. These thermal resistance



values were experimentally extracted following the measurement procedure reported earlier in chapter 3. As a result, a lower temperature rise difference and eventual device failure are observed in both cases. Notably, while the failure mode which is characterized by metallization evaporation and chip rupture is consistent across both devices, however, the extent of metal evaporation is more severe in the module diode as compare to press pack diode. Moreover, the results also highlight that surge events of shorter duration of time can lead to an increased forward voltage, resulting in defects in the silicon chip. In contrast, surge events of longer duration may result in higher thermal resistance, which is influenced by the device packaging technique. Although this study focuses on monolithic silicon diodes, the main conclusions are primarily driven by packaging architecture and thermal management mechanisms rather than silicon material properties alone. Therefore, the qualitative trends regarding junction temperature rise, surge robustness, and failure behavior are expected to remain applicable to SiC devices, albeit with different quantitative limits due to SiC's higher thermal conductivity and allowable junction temperature. Moreover, for multi-chip module architectures, additional effects such as current sharing imbalance and increased interface-related thermal resistance may further influence surge performance. Nevertheless, the electro-thermal methodology and packaging-related insights presented in this work remain directly applicable.

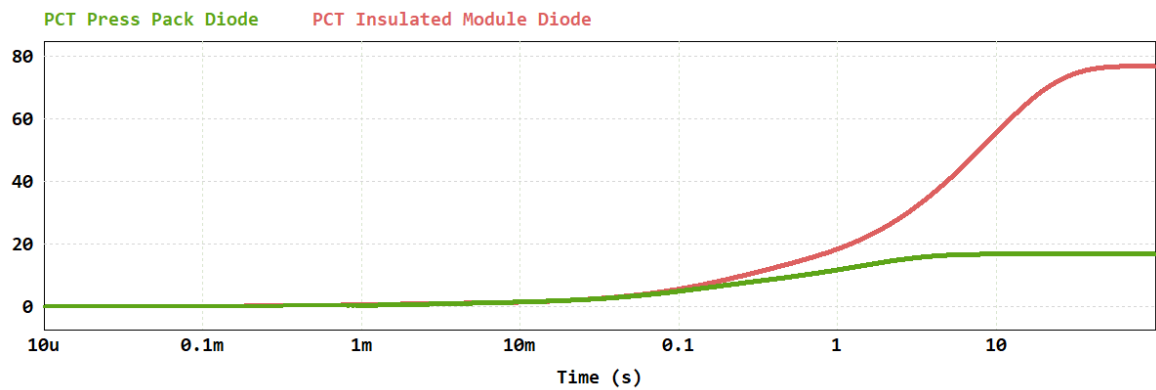


Fig. 5.14 Comparison of thermal impedance between PCT press pack diode and PCT module diode.

## 5.9 Limitations

This chapter discusses the influence of packaging technology and analyzes the failure behavior of the device under surge conditions. However, data-driven approaches such as ML, which are increasingly used in power electronics applications, are not considered in this study. In

particular, the use of ML techniques to predict optimal chip diameter and related design parameters is not addressed and therefore represents a limitation of the present analysis. These aspects are therefore beyond the scope of the present chapter and are investigated in the following chapter.

## 5.10 Conclusion

This chapter presents a comparison between two high-power diode technologies, a press-pack diode and a diode module based on PCT with identical electrical ratings, under high-surge current conditions. A 10 ms half-sine surge generator was developed and implemented both experimentally and in simulation to represent realistic surge events. Moreover, experimental tests were performed on several devices to measure forward voltage and current waveforms. The measured waveforms were used to evaluate device performance, reliability and robustness. Electro-thermal simulations were also performed to estimate the junction temperature during surge events. The results highlights the impact of packaging technology on thermal performance and surge current robustness of device. It is noted that press-pack diode exhibited superior thermal performance, lower junction temperatures, and improved surge handling capability. In contrast, the diode module result in steeper temperature rise and earlier onset of thermal limitations. Moreover, short-duration surge events mainly cause silicon defects through increased forward voltage, while long-duration surges increase thermal resistance due to packaging effects. Additionally, failure analysis also revealed a dominant degradation mechanisms associated with each packaging type. These results highlights the critical role of packaging technology in determining the electro thermal behavior and reliability of high-power semiconductor devices, providing a practical guidance for selecting diode technologies in high power applications. Future work will focus on statistically evaluating surge failure thresholds across multiple devices to assess repeatability and variability. The influence of interface-related parameters such as clamping force, surface condition, and aging on junction temperature and surge robustness will also be investigated. In addition, the proposed electro-thermal methodology will be extended to SiC devices and multi-chip module architectures to quantify material- and packaging-dependent effects on surge performance.

### Publication Related to this Chapter

This chapter reproduces material from the following publication:

**F. Ahmad**, L. Vaccaro, A. A. Nkembi, M. Marchesoni, F. Portesine, and G. Anyanwu, “*Junction Temperature and Failure Behavior of High-Power Press Pack vs. Module Diodes Under High Anomalous Surge Currents*,” **Electronics**, vol. 15, no. 1, p. 121, Dec. 2025. DOI: [10.3390/electronics15010121](https://doi.org/10.3390/electronics15010121)



# Chapter 6

## Machine Learning-Based Classification and Prediction of Chip Diameter in High-Power Devices

This chapter presents a machine learning based modeling framework for the classification and prediction of chip diameter in high-power semiconductor devices. The chapter highlights how geometric variations influence electrical and thermal performance. In Section 6.2, the influence of chip diameter and thickness on device performance is investigated. This section also discuss the effect of variations in material thickness, followed by the evaluation of the impact of chip diameter variation on the electrical and thermal characteristics of the device. Section 6.3 discussed the methodology developed for the ML. This section includes highlighting the data acquisition process, data augmentation and feature optimization methods to improve model performance. The implementation of several ML models, such as SVM, ANN, and ensemble learning methods, is detailed explained in Section 6.4. In addition, in Section 6.5 the results are presented and discussions are detailed, including a comparison of classification accuracies, detailed confusion matrix analysis, and the prediction of chip diameter using optimized models. Moreover, Section 6.6 states the limitations, and finally, Section 6.7 summarizes the main conclusions of the chapter.

### 6.1 Overview and Research Motivation

In recent years, the integration of ML and Artificial Intelligence (AI) has significantly expanded across various domains; however, their application in power electronics is still evolving. Before the advent of these technologies, semiconductor manufacturers focused

on developing devices with reduced size and higher power densities. These advancements have optimized the design and operation of power devices such as power converters [294] and motor drives [295], enabling them to handle higher currents and power levels. Despite this progress, efficient power dissipation remains a challenge, as it is crucial to maintain safe operation within the rated junction temperature limits to prevent device failure. In high-power semiconductor devices, a decrease in diameter may increase resistance, leading to reduced current flow and overheating. Conversely, a larger diameter improves heat dissipation by reducing thermal resistance through distribution over a larger surface area, thereby lowering the risk of failure. Manufacturers like ABB, Infineon, and Poseico Power Electronics have developed high-power semiconductor devices such as press-pack diodes and thyristors with enhanced current and voltage capabilities. ABB, for instance, progressed from a 78mm thyristor (4310A, 1800V, 125°C) to larger 143mm variants for traction, energy, and industrial applications, offering ratings of 8500V/5499A and 7200V/6220A at 110°C. Similarly, Infineon designed a 5200V/3400A thyristor for crowbar and pulsed power applications with full blocking capability at 50/60Hz over a wide temperature range. Moreover, Poseico Electronics developed multiple devices with diameters up to 101mm, voltage ratings from 800V to 6000V, and average currents from 3344A to 8099A, operating at 120°C for industrial and traction applications. Increasing chip diameter generally reduces electrical and thermal stresses, enabling higher power and current capabilities, this can result in non-uniform current distribution and localized hotspot formation. Hence, the selection of an optimal diameter remains a critical preliminary design consideration in high-power semiconductor devices [296].

Manufacturers typically rely on conventional analytical formulations to determine these parameters on the basis of material properties, thermal limits, and electrical performance requirements. However, such formula-based approaches may not fully capture complex inter-dependencies among multiple design variables such as on-state voltage drop, thermal impedance, and transient current handling capability, particularly when operating conditions vary between applications. In this context, data-driven prediction and classification methods offer a complementary pathway, enabling designers to explore the optimal diameter within the feasible operational envelope and tailor device specifications more precisely to target application requirements. ML techniques primarily rely on data-driven models trained on specific scenarios, eliminating the need to manually formulate complex analytical expressions and compute design parameters. These models possess self-learning capabilities, achieving high accuracy even with larger datasets while maintaining computational efficiency. ML can be broadly categorized into supervised and unsupervised learning. Supervised learning is used to develop models in which predictions are made based on both input and output data,

enabling accurate forecasting. It can be further divided into classification and regression; classification assigns data to predefined categories, while regression predicts numerical values based on previous data patterns. These models are widely employed in power electronics and semiconductor applications, transforming processes from design and manufacturing to testing and optimization [269, 270]. Recent studies have demonstrated the effectiveness of ML techniques in modeling [271], prediction [270], and fault diagnosis of IGBTs and power electronic devices [272]. In [273], junction temperature and device degradation were estimated by predicting the on-state voltage using K-NN, SVM, and Decision Tree (DT) models. ML approaches have also been applied to predict the lifetime of IGBT modules, achieving higher accuracy than conventional lifetime models [96]. Data-driven convolutional neural network (CNN) methods have enabled reliable classification of IGBT failure modes under varying operating conditions, highlighting their potential for condition monitoring and predictive maintenance [274]. Furthermore, [275] proposed a hybrid approach combining compact device models with ANNs to predict IGBT output characteristics, obtaining Hefner static model parameters such as  $V_{Gate}$  and  $V_{Anode}$  from structural parameters. Comparative evaluations of ML algorithms, including Random Forest, backpropagation neural networks, and decision trees, have also been conducted for fault diagnosis of power electronic devices in converter systems, demonstrating their applicability across different operational scenarios [276]. These advances demonstrate the versatility of ML across semiconductor manufacturing, device modeling, and predictive analysis. Despite significant progress, most existing studies emphasize reliability assessment, failure mode classification, and prediction of electrical parameters. However, modeling frameworks capable of predicting and classifying fundamental design parameters, such as chip diameter in high-power devices (e.g., diodes and thyristors) remain largely unexplored. Moreover, the existing literature shows that datasets available for training and evaluating ML model performance are limited for various applications in the semiconductor manufacturing industry and power electronics. Especially, datasets related to chip diameter, which can provide valuable predictive insight into design and cost trade-offs. The development of such domain-specific datasets would provide deeper insights into model behavior under varying diameters and electrical parameters, thereby assisting manufacturers in achieving optimized device designs and optimal chip diameter for specific applications. Additionally, SHAP analysis is incorporated to highlight the importance of crucial parameters and to identify the impact of each parameter on model outputs. This can reduce design complexity by guiding parameter tuning towards optimal diameter configurations. Consequently, all influential parameters can be prioritized according to design requirements during device development. This work may enable manufacturers and researchers to optimize parameter selection for specific application requirements. The

applicability of the developed dataset from the manufacturer datasheet extends well beyond the scope of this study, providing a foundational resource for ML models to predict and classify a variety of critical parameters, such as thermal resistance and average current, in high-power semiconductor devices. Furthermore, the proposed methodology can be utilized to design or evaluate the performance of other types of power electronics components, such as IGBTs and diodes, etc. The main contributions of this chapter are as follows:

1. A comprehensive market survey of high-power thyristors is conducted, analyzing the role of chip diameter and current capacity in device performance.
2. A dedicated dataset is developed by extracting electrical parameters from datasheet of multiple leading semiconductor manufacturers.
3. The influence of chip diameter and thickness on electrical and thermal performance is investigated.
4. Multiple ML algorithms are implemented and compared, including ANN, SVM, and Ensemble methods.

## **6.2 Influence of Chip Diameter and Thickness on Electrical and Thermal Performance**

The geometry and dimensions of materials significantly influence thermal management, structural integrity, and electrical properties in semiconductor devices, thereby affecting thermal resistance and, in turn, power dissipation. In particular, thickness and diameter play critical roles in defining the threshold voltage and slope resistance. The effects of these parameters were simulated for various materials under different operating conditions, as detailed below, providing design guidance for optimizing diameters in high-power semiconductor devices.

### **6.2.1 Effect of Change in Material Thickness on Device Performance**

This section presents the influence of material thickness on thermal impedance, for silicon, copper, and molybdenum. Simulations capture both transient and steady-state behavior, exhibiting the direct relationship between thickness and thermal resistance as shown in Figure 6.1(a), (b), and (c). Both copper and molybdenum exhibit negligible variation in transient response at shorter times. However, at steady state, copper shows greater deviation with thickness due to its higher thermal conductivity, while molybdenum demonstrates comparatively smaller differences. In contrast, silicon shows nonlinear deviations at short

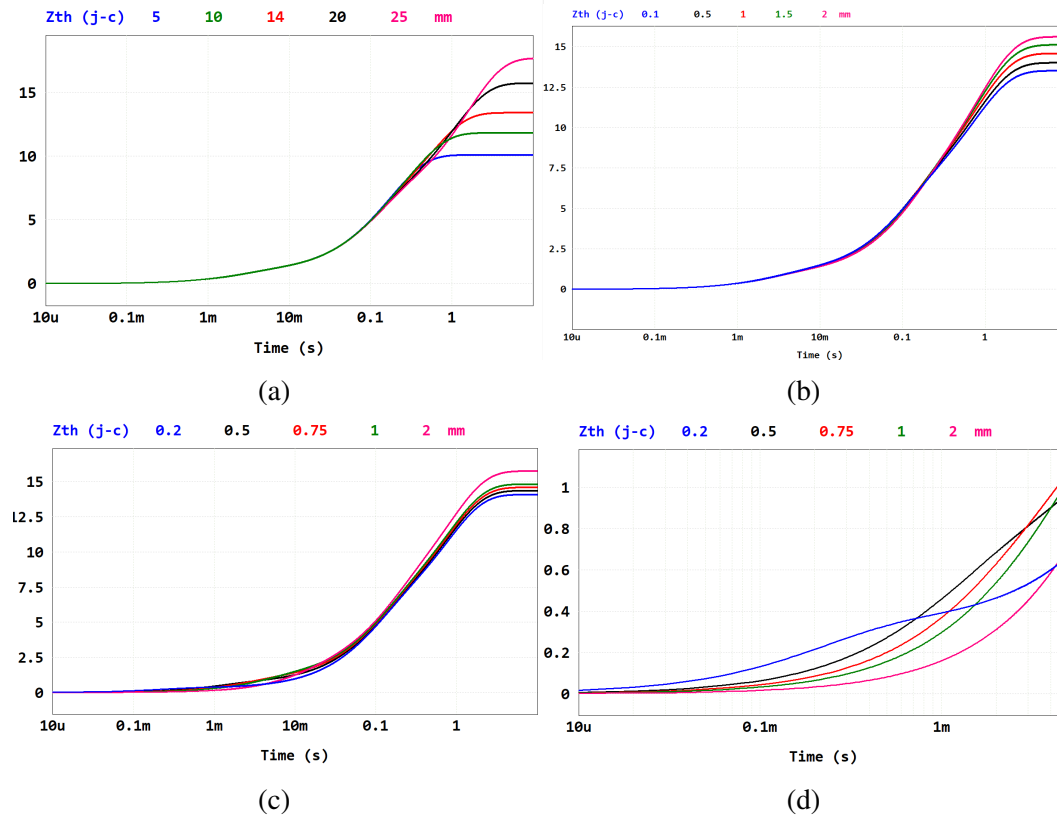


Fig. 6.1 Impact of change in thickness on thermal resistance in different materials (a) Copper. (b) Molybdenum. (c) Silicon. (d) Silicon at 5 ms.

time scales as shown in Figure 6.1(d): for pulses below 10 ms, thicker materials exhibit lower transient thermal impedance when the chip diameter exceeds approx 0.8 mm, as illustrated in Figure 6.2. An increase in thickness leads to higher thermal resistance, which limits power-handling capability and causes elevated temperatures under high current and voltage conditions. This compromises reliability, accelerates device degradation and failure, and requires enhanced cooling strategies.

## 6.2.2 Impact of Change in Material Diameter on Device Performance

The device is simulated to investigate the effect of diameter variation on performance, while keeping the thickness constant. The results indicate that increasing the diameter reduces thermal resistance as shown in Figure 6.3, as the heat is distributed over a larger surface area. Consequently, devices with larger diameters can operate at higher power ratings; however, larger diameters also result in higher capacitance, which may reduce switching speed. Furthermore, uneven current distribution at the edges of larger chips can



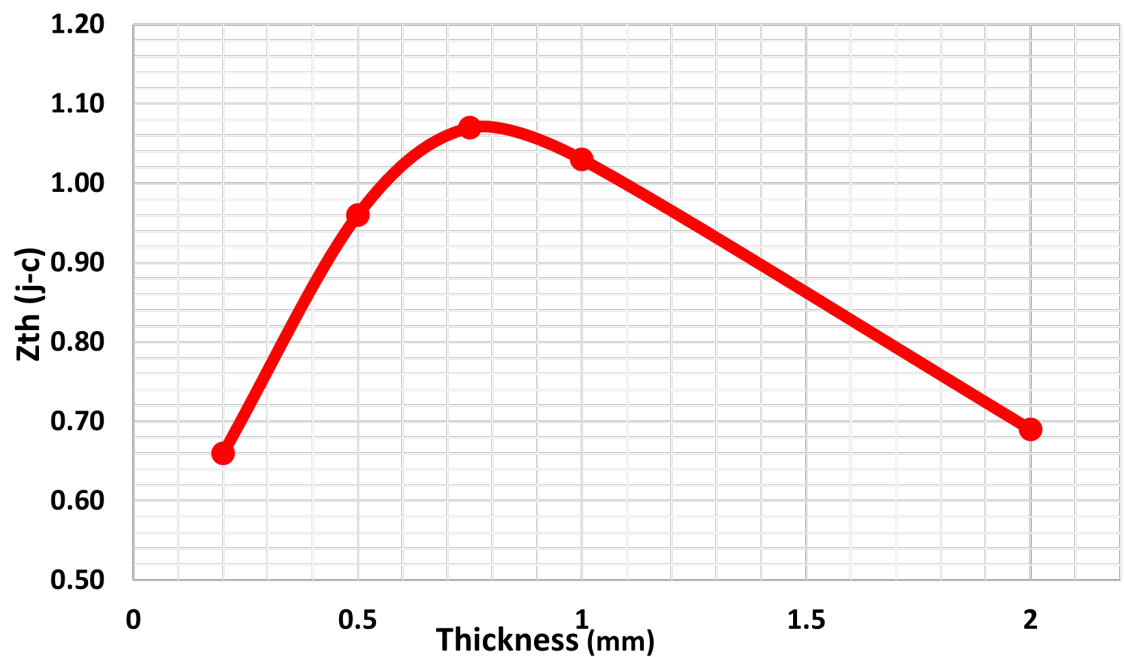


Fig. 6.2 Behavior of device performance due to change in thickness at 5 ms.

lead to localized hotspots and larger temperature gradients across the die during high-power operation, potentially causing performance mismatches within the same device.

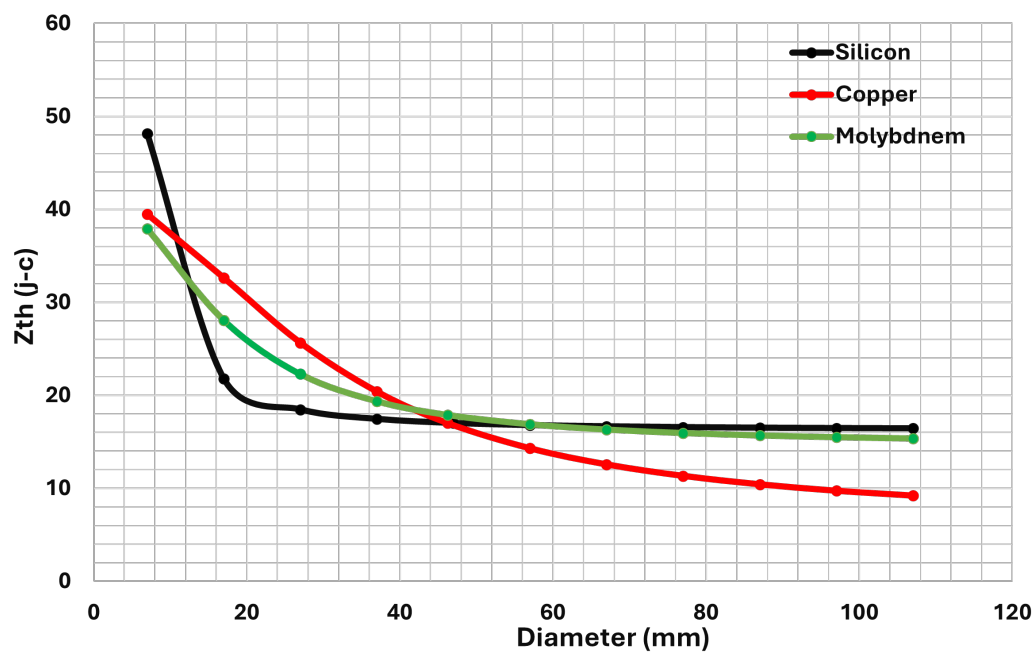


Fig. 6.3 Impact of change in diameter on device thermal impedance.

### 6.2.3 Performance Evaluation of Geometric Variations

As discussed in the previous sections, it is evident from simulation results that variations in the diameter and thickness of the material significantly influence the device characteristics. In particular, changes in these parameters affect the thermal resistance. The performance of device is evaluated in terms of current capability as shown in Figure 6.4. The results clearly

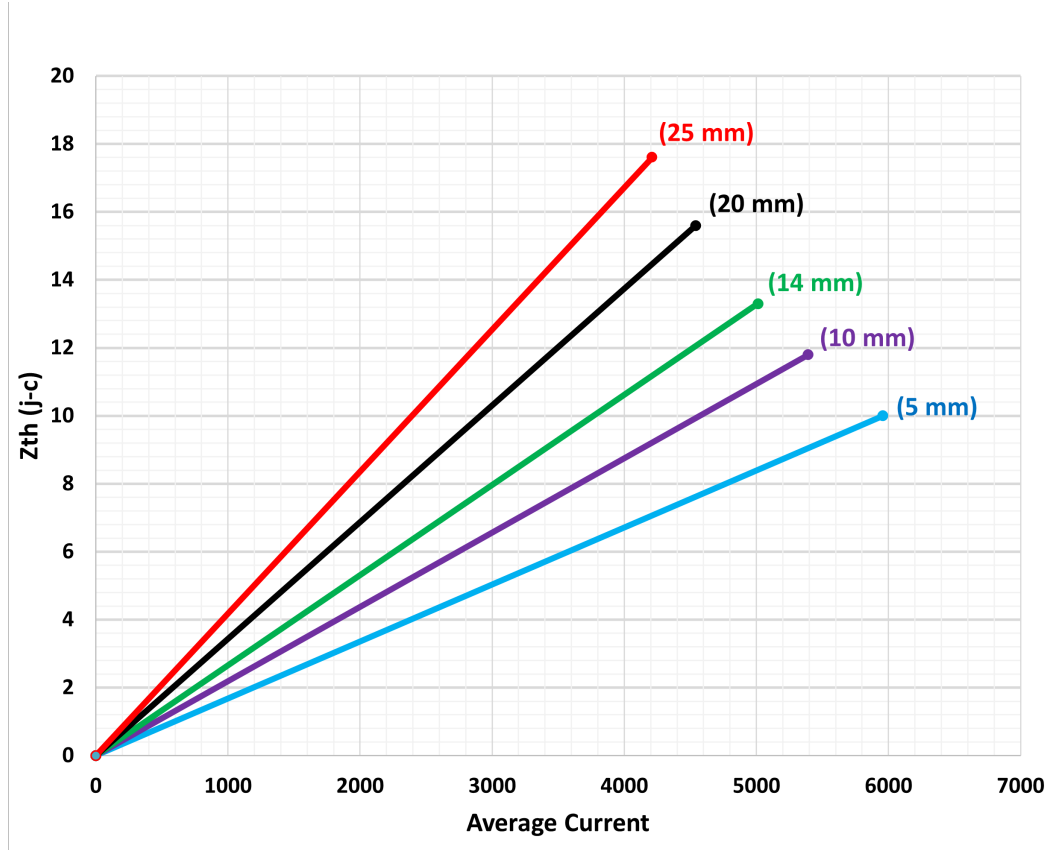


Fig. 6.4 Impact of change in material geometry on device average current in copper.

demonstrate the influence of geometric parameters on device performance. A reduction in thickness decreases the thermal resistance, thereby enabling higher current capability, and vice versa, as summarized in Table 6.1 and Table 6.2 for silicon and molybdenum, respectively. Conversely, an increase in diameter enhances the current capability. While most parameters affecting device characteristics are reported in manufacturer datasheet, a comprehensive analysis of these factors is essential for optimized device design. Other parameters such as device diameter,  $V_{th}$  and  $rT$  etc are kept constant, however, all parameters are interdependent. These findings emphasize the critical role of material geometry in

governing overall device behavior.

Table 6.1 Change in silicon current.

| Thickness (mm) | $R_{th}$ | Current |
|----------------|----------|---------|
| 0.2            | 14       | 4856    |
| 0.5            | 14.3     | 4793    |
| 0.75           | 14.5     | 4752    |
| 1              | 14.8     | 4692    |
| 2              | 15.7     | 4523    |

Table 6.2 Molybdenum current variation.

| Thickness (mm) | $R_{th}$ | Current |
|----------------|----------|---------|
| 0.1            | 13.5     | 4966    |
| 0.5            | 14       | 4856    |
| 1              | 14.5     | 4752    |
| 1.5            | 15       | 4653    |
| 2              | 15.6     | 4541    |

## 6.3 Methodology

### 6.3.1 Data Acquisition

The dataset used in this study is derived from the technical datasheets of leading thyristor manufacturers, namely ABB, Infineon, Dynex, and Posieco Power Electronics. Six key electrical parameters such as peak reverse repetitive voltage ( $V_{RRM}$ ), average current ( $I_{AV}$ ), threshold voltage ( $V_{TH}$ ), thermal resistance ( $R_{th}$ ), slope resistance (rT), and device diameter were systematically extracted and standardized to ensure cross-manufacturer comparability. The dataset comprises 250 thyristor devices, with diameters ranging from 19 mm to 115 mm,  $V_{RRM}$  ratings from 800 V to 8500 V, and average current ratings up to 15000 A. For subsequent analysis, diameters were categorized into defined classes as shown in Table 6.3, enabling a structured representation of characteristics.

Table 6.3 Diameter classes and corresponding included diameters.

| Diameter Class | Included Diameters |
|----------------|--------------------|
| 25             | 19, 25, 31         |
| 38.5           | 35, 38, 41         |
| 47             | 44, 47, 51         |
| 63             | 57, 63             |
| 76             | 73, 78, 80         |
| 100            | 100, 101           |
| 112            | 110, 115           |

This detailed data set provides a wide range of industrial thyristors with various electrical characteristics, thereby providing a robust foundation for ML models aimed at performance prediction, classification, and supporting design decisions. Table 6.4 shows the six features of the dataset which have been considered for the proposed model to classify the diameter of

the chip. All features have numerical values assigned. All these features impact the device performance and help in determining the size of device using the ML system.

Table 6.4 Sample of dataset features used in the proposed model.

| $I_{AV}$ | $R_{th}$ | $V_{RRM}$ | $V_{th}$ | $r_T$  | Diameter (mm) |
|----------|----------|-----------|----------|--------|---------------|
| 1609.56  | 56.59    | 811.23    | 0.7219   | 0.2523 | 25            |
| 2143.54  | 38.68    | 995.51    | 0.7129   | 0.1259 | 38.5          |
| 3370.69  | 18.11    | 2513.90   | 0.7786   | 0.1607 | 48            |
| 4718.06  | 9.16     | 1713.85   | 0.9849   | 0.0692 | 63            |
| 5458.89  | 9.16     | 1852.87   | 0.7451   | 0.1033 | 76            |
| 7157.89  | 6.98     | 1826.56   | 0.7812   | 0.0630 | 100           |
| 9621.60  | 4.41     | 4799.44   | 0.7994   | 0.0711 | 112           |

### 6.3.2 Data Augmentation

Although a variety of thyristor devices are available in market with different specifications, still the availability of data sheets of well known manufacturers are limited, especially for each diameter which reduce the size of data set. In order to balance the classes, data augmentation were performed in MATLAB<sup>®</sup> to increase the sample of classes in data set.[297–299]

Augmentation was performed by generating synthetic samples through controlled random perturbations applied within manufacturer specified tolerance ranges. All parameters were varied by injecting Gaussian noise at a fractional level of  $\pm 5\%$  relative to their nominal values, simulating measurement uncertainties and natural parameter variations. This noise-based approach preserves the underlying statistical distribution and inter parameter relationships inherent to each device class but does not introduce fundamentally new physical variability beyond the sampled tolerance ranges. Consequently, the augmented dataset may not fully represent variability arising from factors outside the manufacturer-specified tolerances, such as manufacturing defects, aging, or extreme operating conditions. Mathematically, for each original feature vector  $\mathbf{x}$ , multiple augmented samples  $\mathbf{x}'$  were created as:

$$\mathbf{x}' = \mathbf{x} + \varepsilon \odot \mathbf{x}$$

where  $\varepsilon$  is a Gaussian noise vector with zero mean and a standard deviation corresponding to the specified noise level, and  $\odot$  denotes element-wise multiplication. To ensure physical plausibility, augmented parameter values were constrained within manufacturer specified limits; for instance,  $V_{RRM}$  was bounded between 800 V and 8500 V, and thermal resistance  $R_{th}$  was restricted to positive, realistic values. Augmentation was applied separately for each

device class to maintain class-specific characteristics, generating five synthetic samples per original instance. This process increased the dataset size significantly and improved class balance, particularly for underrepresented diameter categories. A controlled augmentation of 1:5 was applied to maintain balance in all data classes throughout the data set by normalizing each class relative to its original sample size, ensuring that the effective representation after augmentation remained proportionally consistent across all classes. To verify augmentation quality, statistical comparisons demonstrated substantial overlap between the distributions of original and augmented data. Furthermore, principal component analysis (PCA) revealed that synthetic samples projected onto the first principal component (PC1) lie entirely within the range of the original data distribution, as illustrated in Figure 6.5. PC1 represents the direction of maximum variance in the dataset, whereas the second principal component (PC2) captures the next highest variance along a direction orthogonal to PC1. Moreover, the PCA scores showed variation in the original and augmented datasets were very similar, with variance decreasing by about 2.6% on PC1 and 2.5% on PC2. This highlights that the augmentation results in higher sample density while keeping the original data distribution the same. Subsequently, these results also confirm that the augmentation process did not introduce unrealistic parameter combinations or distort the original data manifold.

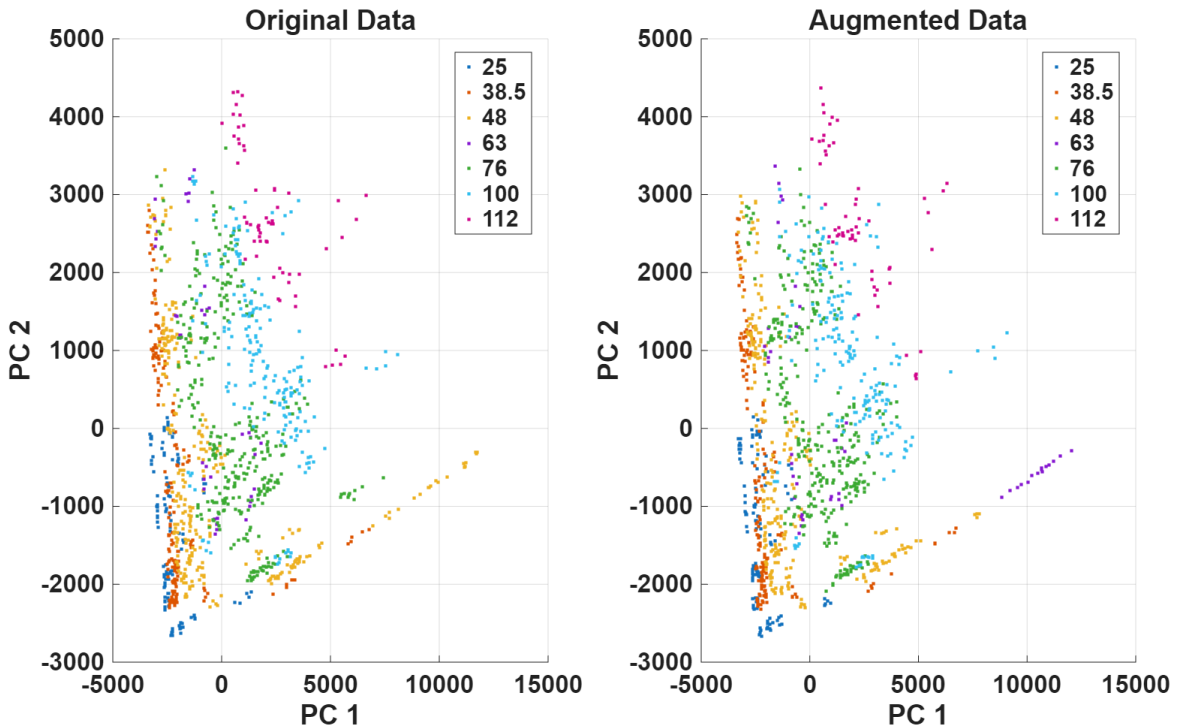


Fig. 6.5 Validation of original data and augmented data.

### 6.3.3 Feature Optimization

To identify the most relevant features contributing to the classification and prediction performance of the ML models, the Minimum Redundancy Maximum Relevance (MRMR) algorithm was employed [300–303]. MRMR selects features that maximize relevance with the target variable while minimizing redundancy among features, thus ensuring an optimal subset that balances information content and independence. Applying MRMR to the dataset revealed that parameters such as  $R_{th}$ ,  $I_{AV}$ , and  $V_{RRM}$  contribute most significantly to accuracy as shown in Figure 6.6, consistent with their critical roles in the performance of thyristor. Other parameters showed lower importance scores, but were retained to preserve structural

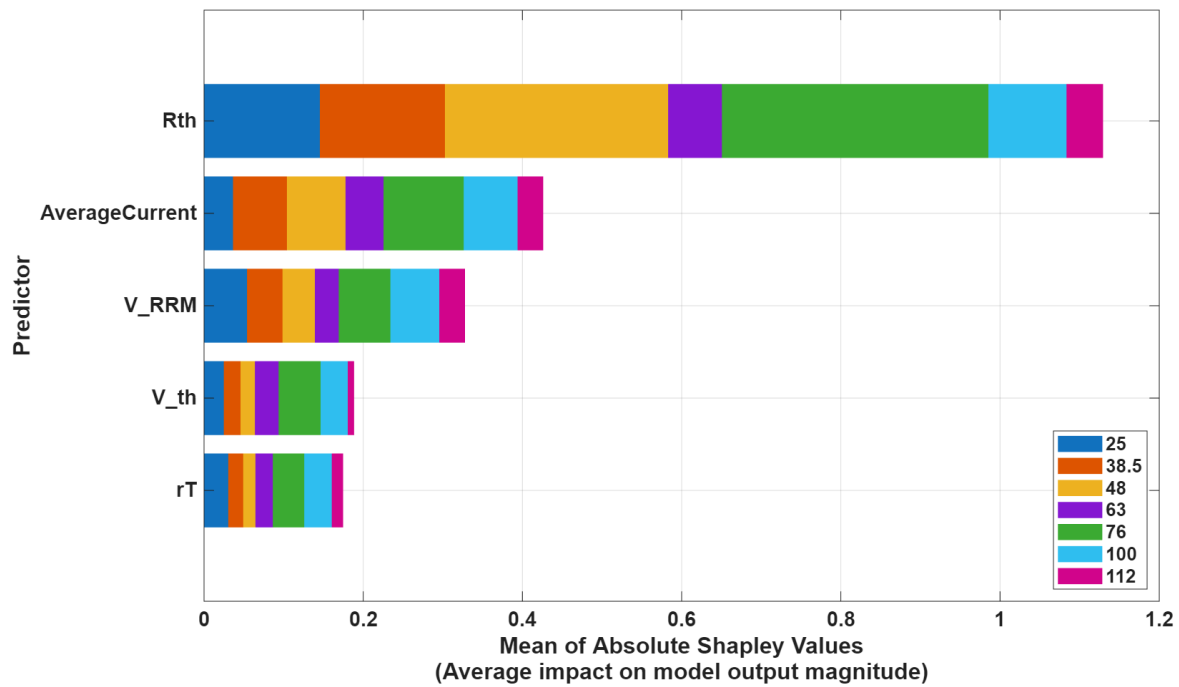


Fig. 6.6 Contribution of feature on output for diameter classification.

information. Based on these results, models trained with the top-ranked features demonstrated improved efficiency and comparable or better accuracy, validating the effectiveness of the feature optimization process in refining the dataset for ML applications.

## 6.4 Implementation of Machine Learning Models

To ensure robust classification and prediction of chip diameter, three ML models were implemented as shown in Figure 6.7 and compared, including SVM, ANN, and ensemble learning. These algorithms were selected due to their complementary strengths in handling

complex, non-linear relationships, diverse dataset distributions, and high-dimensional feature spaces. The architecture of implemented models are listed in Table 6.5. All models were

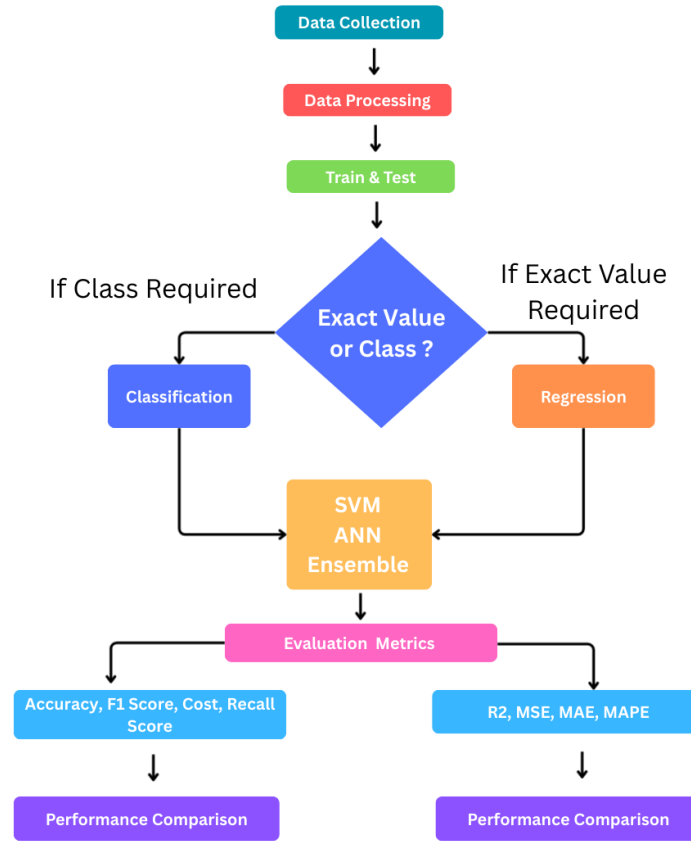


Fig. 6.7 Methodology for diameter classification and prediction.

trained and evaluated using identical dataset partitions, with 90% of the data allocated for training and 10% for testing. Performance was measured using accuracy, F1-score, precision, and recall, averaged over 7-fold cross-validation. Hyperparameter were tuned via Bayesian optimization for each model to ensure optimal performance.

### 6.4.1 Support Vector Machine

Support Vector Machine is a widely used ML algorithm, particularly effective for both classification and regression tasks across diverse application domains. Its strength lies in the ability to model both linear and nonlinear relationships within data by constructing an optimal decision boundary, defined by maximizing the margin between the hyperplane and the closest data points, known as support vectors. These support vectors are critical in determining the classification boundary, as they alone influence the separation of data into distinct categories. In contrast, SVM regression constructs a predictive function by fitting

Table 6.5 Architecture of machine learning models.

| Model    | Architecture                               |
|----------|--------------------------------------------|
| ANN      | Hidden layers: 1                           |
|          | Number of neurons in each layer: 263       |
|          | Activation function: Tanh                  |
|          | Optimizer: Bayesian optimization           |
|          | Learning rate: $9.2024 \times 10^{-09}$    |
| Ensemble | Method: Bagging                            |
|          | Splits: 1023                               |
|          | Learners: 13 (base learner: Decision Tree) |
| SVM      | Kernel: Cubic                              |
|          | Regularization parameter: $C = 1$          |
|          | Kernel scale: 25.5                         |

the model within a specified tolerance margin known as epsilon, ensuring that deviations smaller than this margin do not contribute to the prediction error. During the implementation, the classification model employs a cubic kernel function with a box constraint of 25.5 and a one-vs-one multiclass coding scheme, while the regression model uses a quadratic kernel with a box constraint of 3.7, an epsilon of 2.09, and hyperparameters optimized via Bayesian optimization; the different kernels were chosen to provide flexible nonlinear separation for classification and smooth function fitting for regression. The algorithm automatically determined the optimal kernel value during training through iterative optimization within the range of 0.001–1000.

### 6.4.2 Artificial Neural Network

The ANN model was implemented in MATLAB® 2025a classification learner framework using a feedforward architecture with single hidden layer. Generally, ANN model with multiple hidden layers can be mathematically expressed as:

$$y = f\left(\sum_{i=1}^n w_i x_i + b\right),$$

where  $x_i$  are the inputs,  $w_i$  the corresponding weights indicating the importance of each feature,  $b$  the bias term, adjusting the output independently of the input values and  $f(\cdot)$  the activation function. the values of  $w_i$  and  $b$  are adjusted to reduce errors between its predictions and actual data. In this study, Bayesian optimization was employed to tune the hyperparameter and determine efficient ANN architectures. For classification, the optimal configuration



consists of single hidden layer with 263 neurons, utilizing a tanh activation function and trained for 1000 iterations to achieve stable convergence. For regression, the optimized architecture comprises two hidden layers with 296 and 3 neurons, respectively, employing a rectified linear unit (ReLU) activation function for effective nonlinear approximation. These architectures were selected to balance model complexity with generalization capability, ensuring reliable performance across both tasks.

### 6.4.3 Ensemble Methods

Ensemble methods are ML techniques that combine multiple learners trained on the same dataset to improve prediction accuracy and robustness. Two commonly used strategies are bagging and boosting. In bagging, multiple models are trained on random subsets of the dataset, and predictions are aggregated by averaging (for regression) or voting (for classification). Boosting, in contrast, trains a sequence of weak learners iteratively, increasing the weights of misclassified samples to reduce errors in subsequent rounds, with the final prediction obtained by combining weighted outputs. In this study, bagging, a decision tree ensemble classifier was employed for classification, where maximum number of splits is 1023, and the ensemble consisted of 13 learners. For regression, a bagging ensemble was used, with decision trees having a minimum leaf size of 2 and considering 4 variables at each split with 13 number of learners; predictions were averaged across all trees to reduce variance. Hyperparameter for both classification and regression ensembles were optimized using Bayesian optimization to achieve robust architecture and improved generalization performance. Bagging was employed for both classification and prediction to improve the stability and accuracy of the model. Both techniques are fundamental to ensemble learning, aiming to enhance the overall predictive performance and robustness of ML algorithms [304].

## 6.5 Results and Discussion

### 6.5.1 Comparison of Classification Accuracies

This study determined that ML algorithms can be used to accurately classify the diameter of high power thyristors. Both ANN and SVM classifiers achieved an accuracy of 95%, while Ensemble resulted in an accuracy of 96.7%. The performance of all algorithms are satisfactory in this study and achieved an accuracy of over 95% as listed in Table 6.6. For each diameter class  $i$ , true positives ( $TP_i$ ), false positives ( $FP_i$ ), false negatives ( $FN_i$ ), and true negatives ( $TN_i$ ) were obtained from the confusion matrix. Overall accuracy was computed as

the ratio of correctly classified test samples to the total number of test samples:

$$\text{Accuracy} = \frac{\sum_i TP_i}{N_{\text{total}}} \quad (6.1)$$

Table 6.6 Model performance on validation and test datasets.

| Parameter           | Artificial Neural Network | Ensemble | Support Vector Machine |
|---------------------|---------------------------|----------|------------------------|
| <b>F1 score</b>     |                           |          |                        |
| Test                | 95.1                      | 96.6     | 95.1                   |
| Validation          | 96.1                      | 94.8     | 96.0                   |
| <b>Recall score</b> |                           |          |                        |
| Test                | 95.0                      | 96.7     | 95.0                   |
| Validation          | 96.1                      | 94.8     | 96.1                   |
| <b>Accuracy</b>     |                           |          |                        |
| Test                | 95.0                      | 96.7     | 95.0                   |
| Validation          | 96.1                      | 94.9     | 96.1                   |
| <b>Precision</b>    |                           |          |                        |
| Test                | 96.4                      | 96.8     | 95.6                   |
| Validation          | 96.1                      | 94.9     | 96.0                   |

Among the evaluated models, the ANN achieves the best overall performance, delivering 95.0% testing accuracy along with stable F1-score and recall i.e., 96.1% across validation, demonstrating robustness against overfitting. In comparison, the SVM model attains a similar accuracy of 95% but shows lower F1 score and recall of 96% and 96.1% respectively, while the Ensemble reaches the highest accuracy of 96.7% yet suffers from degraded recall 94.8% and significantly higher computational cost. Furthermore, ANN exhibits the lowest validation cost of 42, compared to 43 for SVM and 56 for Ensemble, reflecting greater efficiency and reduced sensitivity to feature tuning and class-boundary effects. While the Ensemble model offers competitive accuracy, its higher class-specific error rates and lack of end-to-end feature learning result in reduced generalization. The ANN's architecture effectively captures non-linear feature interactions, enabling reliable deployment in high-stakes, real-time applications, whereas the SVM's superior accuracy is offset by its computational overhead as shown in Table 6.7. Overall, the ANN achieves the best trade-off between accuracy, efficiency, and robustness, establishing state-of-the-art performance.

### 6.5.2 Confusion Matrix Analysis

Confusion matrix analysis shows that most models achieve class-wise accuracies above 90% except few classes such as 100, 63, and 38.5. For class 38.5, both ANN and SVM reach

Table 6.7 Computational performance metrics for classification and regression-based prediction.

| Model    | Classification    |                 |                          | Regression-based Prediction |                 |                          |
|----------|-------------------|-----------------|--------------------------|-----------------------------|-----------------|--------------------------|
|          | Training Time (s) | Model Size (kB) | Prediction Speed (obs/s) | Training Time (s)           | Model Size (kB) | Prediction Speed (obs/s) |
| ANN      | 700.12            | 29              | 23000                    | 220.4                       | 23              | 100000                   |
| Ensemble | 95.12             | 313             | 12000                    | 38.2                        | 60              | 90000                    |
| SVM      | 893.66            | 28              | 6000                     | 107.1                       | 37              | 130000                   |

88.9% accuracy as shown in Figure 6.8 and 6.9, with misclassifications distributed in class 25.

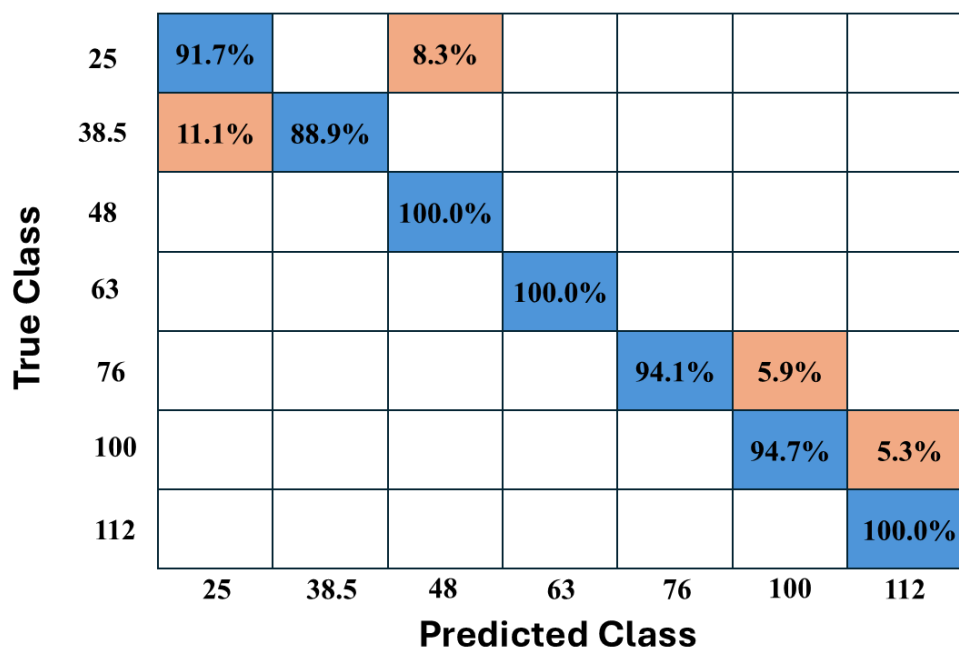


Fig. 6.8 Confusion matrix of test accuracy for classification of diameter by ANN.

For class 63, both the ensemble learner and SVM achieved an accuracy of 80%, with the ensemble model misclassifying samples as class 100 as shown in Figure 6.10, while the SVM misclassified them as class 76. In contrast, the ANN exhibited superior performance, attaining 100% accuracy for class 63 and misclassifying only 5.3% of samples in class 100, compared to 10.5% by the Ensemble model, reflecting its stronger ability to define clear decision boundaries and avoid local minima. Additionally, the SVM accuracy also decreases for class 112 to 83.3%, misclassifying some samples as class 100. This reduction is likely due to the SVM's reliance on maximizing class separation, which is challenging for small datasets, making it more prone to overfitting. In contrast, ANNs and Ensemble methods are more robust on limited data, as they can generalize through multi-layered architectures or by aggregating multiple diverse models to reduce individual errors. Overall, apart from these

| True Class      | 25     | 38.5  | 48     | 63    | 76    | 100   | 112   |
|-----------------|--------|-------|--------|-------|-------|-------|-------|
|                 | 100.0% |       |        |       |       |       |       |
|                 | 11.1%  | 88.9% |        |       |       |       |       |
|                 |        |       | 100.0% |       |       |       |       |
|                 |        |       |        | 80.0% | 20.0% |       |       |
|                 |        |       |        | 2.9%  | 97.1% |       |       |
|                 |        |       |        | 5.3%  |       | 94.7% |       |
|                 |        |       |        |       |       | 16.7% | 83.3% |
|                 | 25     | 38.5  | 48     | 63    | 76    | 100   | 112   |
| Predicted Class |        |       |        |       |       |       |       |

Fig. 6.9 Confusion matrix of test accuracy for the diameter classification for SVM.

exceptions, all models maintain high accuracies above 95%, confirming their robustness for diameter classification.

#### 6.5.2.1 Confusion Matrix of Optimized Features

The models were evaluated using the optimized feature parameters described in Section 6.3.3. Results confirm that these parameters enable accurate diameter classification with overall performance approaching 90% accuracy. Specifically, the ANN and SVM models achieved 94.2% accuracy, while the Ensemble reached 90.9%, as depicted in Table 6.8.

Although the SVM achieves comparable accuracy to the ANN, the ANN attains this performance at a substantially lower computational cost. Specifically, the ANN demonstrates superior efficiency with a prediction speed of approximately 48,000 observations per second (obs/s), compared to 18,000 obs/s for the SVM, establishing it as the most effective and computationally efficient model among those evaluated. Nonetheless, the full feature models deliver a higher accuracy of 95%, the models achieve approximately 94.2% accuracy with the optimized feature parameters. This reduction in accuracy is not very high and indicates that the optimized features possess sufficient classification capability while significantly reducing complexity, making it acceptable. The confusion matrix of ANN, as shown in Figure 6.11 reveal that the performance of optimized features is reduced for classes 63, 76, and 112 while improved for class 100. Similarly for the ensemble, classes 76 and 112 are misclassified as

| True Class      | 25   | 100.0% |       |        |       |        |       |        |
|-----------------|------|--------|-------|--------|-------|--------|-------|--------|
|                 | 38.5 | 5.6%   | 94.4% |        |       |        |       |        |
|                 | 48   |        |       | 100.0% |       |        |       |        |
|                 | 63   |        |       |        | 80.0% |        | 20.0% |        |
|                 | 76   |        |       |        |       | 100.0% |       |        |
|                 | 100  |        |       | 5.3%   |       | 5.3%   | 89.5% |        |
|                 | 112  |        |       |        |       |        |       | 100.0% |
|                 |      | 25     | 38.5  | 48     | 63    | 76     | 100   | 112    |
| Predicted Class |      |        |       |        |       |        |       |        |

Fig. 6.10 Confusion matrix of test accuracy for ensemble.

Table 6.8 Model performance on validation and test datasets with optimized parameters.

| Parameter           | Artificial Neural Network | Ensemble | Support Vector Machine |
|---------------------|---------------------------|----------|------------------------|
| <b>F1 Score</b>     |                           |          |                        |
| Test                | 94.3                      | 91.1     | 94.3                   |
| Validation          | 94.9                      | 94.2     | 94.7                   |
| <b>Recall Score</b> |                           |          |                        |
| Test                | 94.2                      | 90.9     | 94.2                   |
| Validation          | 94.9                      | 94.2     | 94.7                   |
| <b>Accuracy</b>     |                           |          |                        |
| Test                | 94.2                      | 90.9     | 94.2                   |
| Validation          | 94.9                      | 94.2     | 94.7                   |
| <b>Precision</b>    |                           |          |                        |
| Test                | 94.8                      | 91.4     | 94.7                   |
| Validation          | 94.9                      | 94.3     | 94.8                   |

illustrated in Figure 6.12 and improved for class 38.5. Moreover, the confusion matrix of the SVM, shown in Figure 6.13, indicates improvement in the classification of classes 38.5, 48, and 76, while the other classes indicates a close match with the full feature classification.

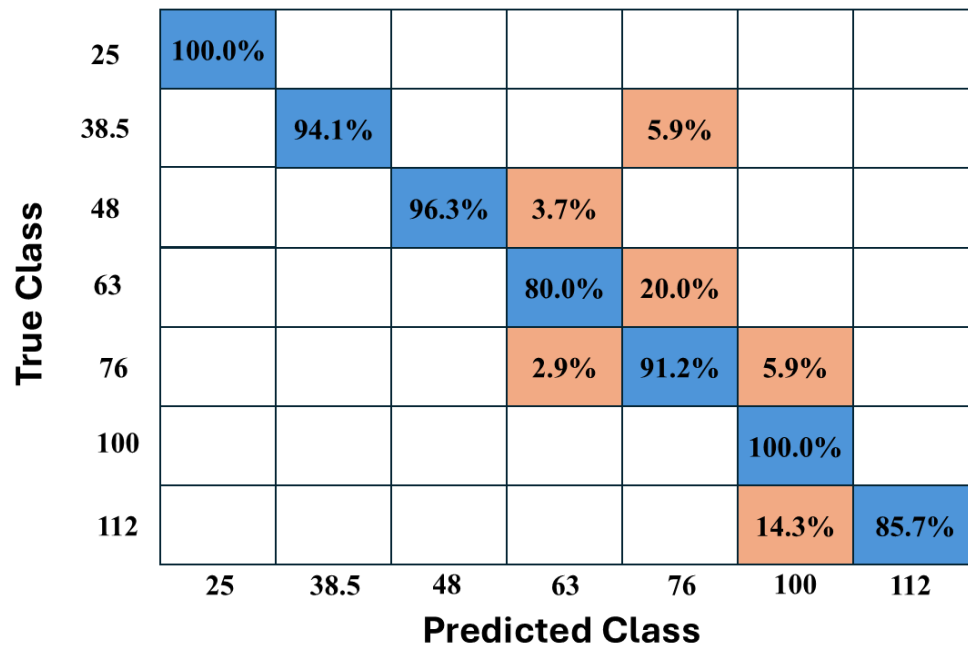


Fig. 6.11 Confusion matrix of test accuracy for the diameter classification with feature optimized ANN.

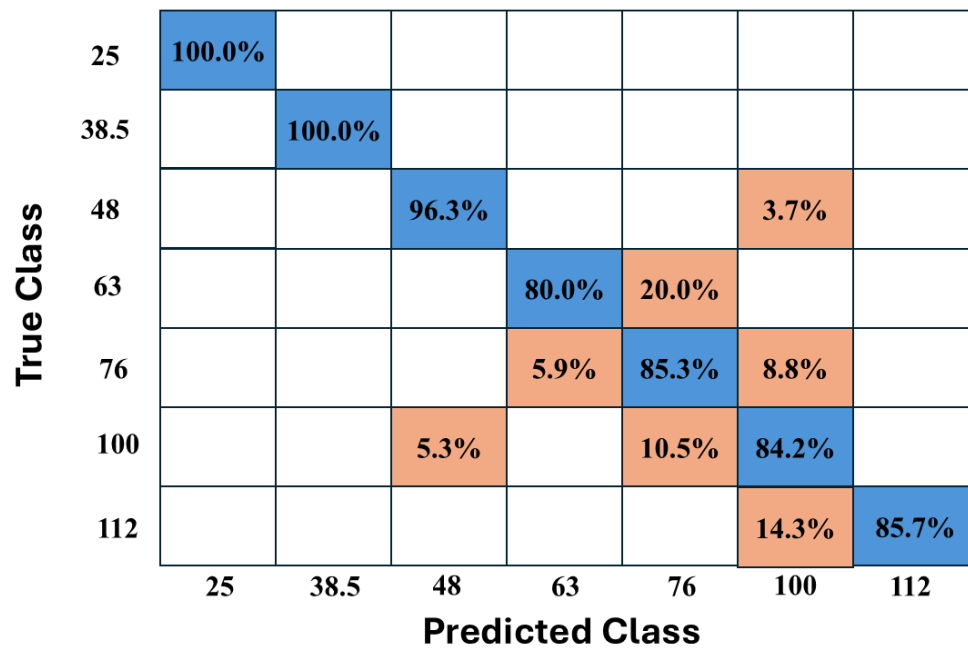


Fig. 6.12 Confusion matrix of test accuracy for the diameter classification with optimized features ensemble.

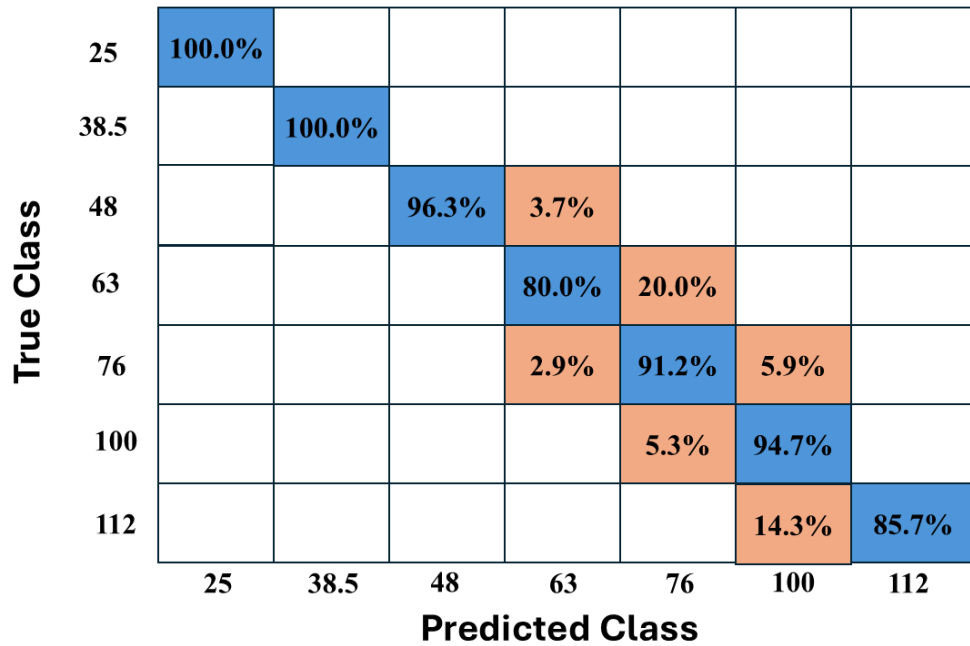


Fig. 6.13 Confusion matrix of test accuracy for the diameter classification with optimized features SVM.

### 6.5.3 Prediction of Chip Diameter

Regression analysis is a fundamental approach for predicting continuous process variables, enabling precise forecasting of critical parameters. In this study, the predictive performance of the three optimized ML models, ANN, Ensemble, and SVM, was evaluated for diameter prediction. Table 6.9 summarizes the performance metrics, highlighting that the Ensemble model achieved the highest accuracy with a minimum prediction error of 0.03. SVM yielded comparable accuracy but with a higher average error of 0.07 (2.3× that of Ensemble). In contrast, ANN demonstrated the worst performance, with  $R^2 = 0.76$  and an average error of 0.24 (8× higher than Ensemble). The ensemble and SVM models achieved  $R^2$  values of 0.97 and 0.93, respectively, which are considered acceptable for applications in the manufacturing industry.

Table 6.9 Comparative performance of optimized regression models for average current forecasting.

| Model                     | $R^2$ | Mean Squared Error (MSE) | Mean Absolute Error (MAE) | Mean Absolute Percentage Error (MAPE)(%) |
|---------------------------|-------|--------------------------|---------------------------|------------------------------------------|
| Optimized Ensemble        | 0.97  | 20.4                     | 1.7                       | 3.4                                      |
| Support Vector Machine    | 0.93  | 47.7                     | 4.8                       | 8.8                                      |
| Artificial Neural Network | 0.76  | 161.09                   | 9.78                      | 18.1                                     |

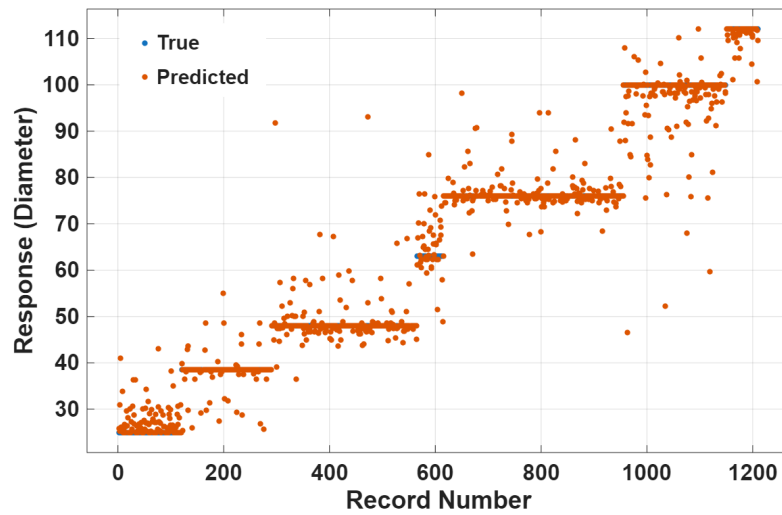


Fig. 6.14 Prediction accuracy of chip diameter using the ensemble model.

The deviations between actual and predicted diameters for Ensemble, SVM, and ANN are illustrated in Figures. 6.14, 6.15, and 6.16, respectively. The ANN model exhibits the largest discrepancies, in contrast to the closer alignment achieved by ensemble and SVM. This reduced performance is attributed to the limited dataset size, as ANN typically requires larger datasets to effectively learn complex patterns, resulting here in overfitting and degraded generalization. These findings establish the ensemble model as the most efficient and reliable predictor as detailed in Table 6.7, with predicted diameters closely matching the actual values. This capability enables manufacturers to develop devices precisely tailored to the requirements of their specific applications.

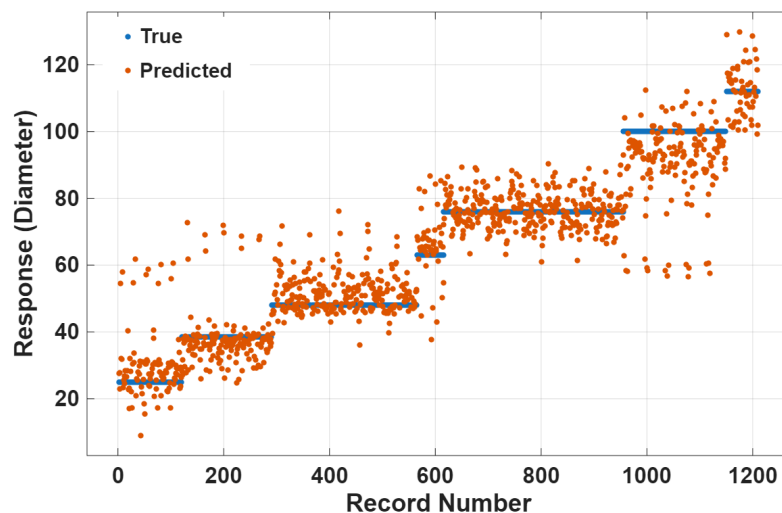


Fig. 6.15 Prediction accuracy of chip diameter using the Support Vector Machine (SVM) model.



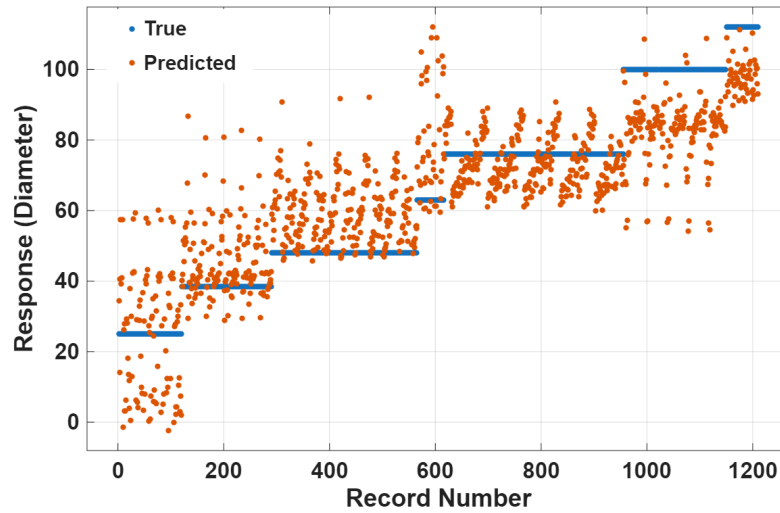


Fig. 6.16 Prediction accuracy of chip diameter using the Artificial Neural Network (ANN) model.

## 6.6 Limitations

In this chapter, a methodology is developed to predict the chip diameter based on the proposed framework. However, in semiconductor devices, the accurate prediction of the average current is also a critical parameter for device design and performance evaluation. The estimation of average current is not considered in this chapter and therefore represents a limitation of the present study. This aspect is addressed in the following chapter.

## 6.7 Conclusion

In this work, a comprehensive market survey was conducted to explore high-current thyristors, and a dataset was generated from leading manufacturers through the extraction of various electrical parameters. To increase the dataset size, data augmentation techniques were applied, and the device diameters were categorized into seven classes. Classification and prediction of diameter based on these parameters were performed using three ML algorithms: ANN, Ensemble, and SVM. Although the SVM achieved slightly higher accuracy, its computational cost was significantly greater, making the ANN the most efficient and reliable choice for diameter classification. However, in the regression-based prediction tasks, both the ensemble and SVM models demonstrated superior predictive performance compared to the ANN, indicating their enhanced capability in capturing the underlying nonlinear relationships within the dataset. Future work will focus on extending this methodology to predict and

classify current ratings, as well as implementing other advanced AI models and algorithms to further enhance performance and generalization.

**Publication Related to this Chapter**

This chapter reproduces material from the following publication:

**F. Ahmad**, L. Vaccaro, A. A. Nkembi, and F. Portesine, “*Classification and Prediction of Chip Diameter in High-Power Semiconductor Devices Through Electrical Parameters Using Machine Learning*,” **Technologies**, vol. 13, no. 12, p. 567, Dec. 2025. DOI: [10.3390/technologies13120567](https://doi.org/10.3390/technologies13120567)



# Chapter 7

## Machine Learning Framework for Average Current Classification and Prediction

This chapter outlines a ML framework utilized for the classification and prediction of average current in high-power devices. Section 7.2 states the methodology, which includes the preparation and structure of the dataset. Moreover, in Section 7.3, the feature extraction and selection process are detailed in depth. This reflects relevant electrical and thermal parameters to optimize and enhance model performance. Section 7.4 presents the implementation of various ML models, including ANN, ensemble learning methods, SVM, and gaussian process regression (GPR). In addition, in Section 7.5, the results and discussion are presented. This section introduces SHAP-based feature importance analysis and evaluates classification performance through the confusion matrix and related metrics. It also presents results of average current prediction and compares the performance of different models. Finally, Section 7.6 summarizes the key findings and conclude the chapter.

### 7.1 Overview and Research Motivation

The growing demand for high power density in advanced power electronics systems, including applications in HVDC [280, 305], data centers [306], and converters [4, 307], has significantly increased the development of devices that are capable of operating under higher current and voltage levels. Among these devices, high-power diodes and thyristors are still prominent choices in various applications due to their superior current and voltage ratings. However, with an increase in power levels, the reliability of the device becomes a critical

concern in both designing and manufacturing. In power conversion systems, the failure rate of power semiconductor devices has been reported to reach up to 31% of damaged devices, primarily due to excessive temperature rise [308, 309]. The junction temperature is a key reliability parameter influenced by several factors, most notably power dissipation. Since temperature rise is strongly correlated with average current, monitoring and controlling the device's average current is essential to maintain junction temperature within safe limits and to ensure the long-term reliability of high-power electronic systems.

Currently, conventional methods are used to calculate the average current of devices, including analytical models [310] and empirical methods. In practical industry applications, mostly manufacturers conduct experimental tests to employ analytical approaches for current ratings and evaluating the device performance, which are typically based on conduction loss analysis and thermal modeling-based estimation, as shown in Figure 7.1. The conduction loss method quantifies the power dissipated during forward conduction by relating the average current to both the power loss and the corresponding voltage drop across the device. In contrast, thermal modeling has been utilized for thermal characterization of the device, and the resulting thermal resistance and junction temperature rise has been used to estimate average current. Thus, devices with lower thermal resistance dissipate heat more efficiently, enabling higher current handling capability and vice versa. However, the experimental setups consist of substantial and costly equipment that requires complex procedures. Furthermore, performing tests with higher current may compromise the reliability of such devices, resulting in performance degradation and failure. Subsequently, simulation-based methods are employed to investigate the thermal and electrical behavior of the device using simulation program with integrated circuit emphasis (SPICE) modeling and finite element analysis (FEA). Circuit-level and thermal network simulations enable the estimation of average current from the power loss and thermal profiles. Furthermore, standard power ratings, which are typically provided by manufacturers in device datasheets, enable the application of empirical estimation methods for average current calculation. Such methods rely on interpolating the characteristic curves (e.g., I–V or V–I relationships) under specified operating conditions to estimate the average current while ensuring that the operating point remains within the safe operating area (SOA) of the device. However, these models usually fail to describe the actual behavior of the devices accurately. In recent years, data-driven approaches have been widely adopted for classification and prediction tasks across various domains, including semiconductors and power electronics, where they have been applied to lifetime estimation [96–98], condition monitoring and fault diagnostics [96, 99, 100], and performance prediction [101, 102, 277]. In [278], the remaining useful life of insulated gate bipolar transistors (IGBTs) was directly estimated using various ML models, followed by a comparative performance analysis. In

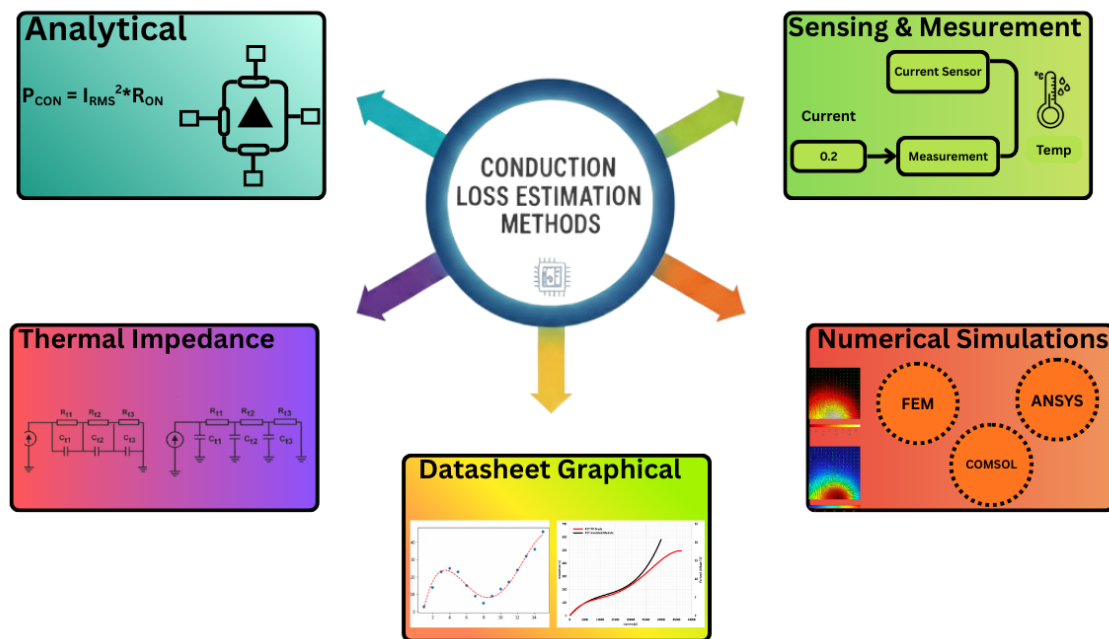


Fig. 7.1 Various techniques to estimate average current.

[99], a method is proposed for early degradation detection of bonding wires. An ensemble learning approach was employed for state classification of the extracted features. Moreover, to improve the accuracy of random forest model classification, cross-validation and particle swarm optimization were also used in this study. Furthermore, in [104], ML is integrated with finite element analysis to estimate the equivalent resistivity and thermal conductivity of semiconductor chips under various operating conditions with improved accuracy. The authors in [105] investigated chip-level thermal mapping and the prediction of temperature change rates using a ML-based neural network model. Similarly, [279] proposed a model for IGBTs that employs ML algorithms, including linear regression, SVM, and random forest, to estimate junction temperature by using collector-emitter voltage ( $V_{CE}$ ) and collector current ( $I_C$ ) as input features. While these advances demonstrate ML's growing role in semiconductor analysis, most existing studies focus on reliability assessment, failure classification, and thermal parameter prediction, often limited to IGBTs. In contrast, ML models for predicting and classifying critical design parameters, such as average current of high-power thyristors and diodes, remain largely unexplored, which employ nonlinear behavior and manufacturer-dependent design variations. To bridge this gap, this study presents a data-driven framework that enables devices to operate closer to their rated current limits without compromising their reliability while reducing device design time and improving the accuracy of prediction. The methodology can also be extended to estimate other critical parameters, such as thermal

resistance and reverse blocking voltage, and could be adapted to other high-power devices like IGBTs and diodes, offering a practical tool for device design and performance evaluation. The main contributions of this chapter are summarized as follows:

- SHAP analysis is performed to highlight the importance of crucial parameters and to identify the impact of each parameter on the output. The analysis provides interpretability by quantifying feature contributions.
- ML model is developed for both classification of average current into nine categories and continuous regression, enabling simultaneous discrete rating assessment and precise performance prediction.
- A comparative evaluation of multiple ML algorithms is conducted using standardized performance metrics, identifying optimal trade-offs between prediction accuracy, computational efficiency, and model robustness.

## 7.2 Methodology

The proposed ML modeling utilizes critical electrical and thermal parameters, extracted from datasheets of multiple semiconductor manufacturers, to evaluate the average current capability of the device. After data pre-processing, SHAP-based feature selection is employed to quantify and rank the importance of each parameter, generating both full-feature and reduced-feature sets. These feature sets are then used to train classification models when current classes are required and regression models when exact current values are needed. Various machine learning models, including SVM, ANN, GPR, and ensemble, are implemented, and their performance is compared. This workflow enables automatic estimation of the device's average current capability, enhancing reliability and reducing the need for manual interpretation. However, several input parameters (e.g.,  $R_{th}$ ,  $r_T$ , and device diameter) are associated with the average current of the manufacturer's design process; therefore, correlations with the target variable are expected. Importantly, the dataset includes devices from multiple manufacturers, which reduces the risk that the model merely reproduces a single manufacturer's design choices. The proposed model captures these design-driven dependencies as represented in practical device specifications and reflected in the dataset. The complete structure of the methodology is presented in Figure [7.2](#)

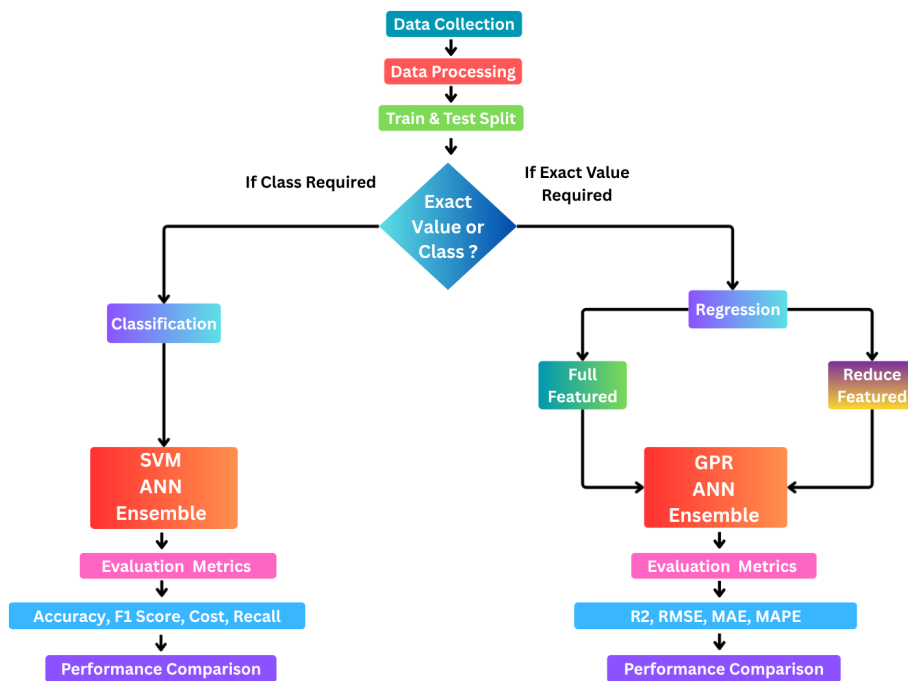


Fig. 7.2 Methodology for classification and prediction of average current.

### 7.2.1 Dataset

The employed dataset was developed as discussed in Section 6.3 from the device information provided in the technical data sheets of leading thyristor manufacturers, including ABB, Infineon, Dynex, and Posieco Power Electronics. Six key electrical and structural parameters that can influence the device behavior, including peak reverse repetitive voltage ( $V_{RRM}$ ), average current ( $I_{AV}$ ), threshold voltage ( $V_{th}$ ), thermal resistance ( $R_{th}$ ), slope resistance ( $rT$ ), and device diameter, were systematically extracted and standardized to ensure cross-manufacturer consistency. In this dataset, a total number of 250 industrial thyristor devices were included with diameters ranging from 19 mm to 115 mm,  $V_{RRM}$  ratings from 800 V to 8500 V, and average current ratings from 124 A up to 14 kA. In order to classify the devices, average current values were divided into 9 defined classes given as 350 A, 750 A, 1500 A, 2500 A, 3500 A, 4750 A, 6000 A, 7500 A, and 12500 A, enabling a structured representation suitable for supervised learning. To increase the dataset size, a controlled data augmentation strategy with a ratio of 1:5 was applied, resulting in a total sample size of 1,252. Class balance was preserved by normalizing each class relative to its original sample size, thereby ensuring proportional and effective representation of all classes after augmentation. Moreover, Table 7.1 shows the six input features that are considered in the proposed model for classifying and predicting the average current capability of the device. All features



Table 7.1 Dataset features used in the proposed model, including average current details.

| Diameter (mm) | $R_{th}$ | $V_{RRM}$ | $V_{th}$ | $r_T$ | Average Current |         |                |
|---------------|----------|-----------|----------|-------|-----------------|---------|----------------|
|               |          |           |          |       | $I_{AV}$        | Samples | Percentage (%) |
| 25            | 60       | 1400      | 0.96     | 0.6   | 350             | 90      | 7.19 %         |
| 25            | 50       | 1600      | 1.00     | 0.92  | 750             | 157     | 12.54 %        |
| 38.5          | 37       | 1800      | 0.81     | 0.24  | 1500            | 192     | 15.34 %        |
| 48            | 26       | 2600      | 0.80     | 0.165 | 2500            | 121     | 9.67 %         |
| 48            | 21       | 2600      | 0.80     | 0.11  | 3500            | 160     | 12.78 %        |
| 73            | 9.5      | 800       | 0.84     | 0.06  | 4750            | 207     | 16.53 %        |
| 100           | 7        | 2800      | 0.77     | 0.10  | 6000            | 100     | 7.99 %         |
| 100           | 6        | 1800      | 0.90     | 0.05  | 7500            | 145     | 11.58 %        |
| 100           | 6.5      | 2400      | 0.85     | 0.029 | 12500           | 80      | 6.39 %         |

are numerical and directly influence the electro-thermal behavior of the thyristor, thereby providing a robust basis for machine-learning-driven performance prediction, classification, and decision support in design.

### 7.3 Feature Extraction and Selection

In order to highlight the impact of the input parameters on the output, feature relevance analysis is first performed using the Minimum Redundancy Maximum Relevance (MRMR) algorithm to identify parameters that may influence  $I_{AV}$  prediction. MRMR optimizes feature ranking by maximizing mutual information with the target variable while minimizing redundancy among features. The MRMR ranking scores are presented in Figure 7.3. Subsequently, SHAP analysis is applied to the trained models for interpretability as discussed in Section 7.5.1.

### 7.4 Implementation of Machine Learning Models

This study focuses on estimating the average current of high-power semiconductor devices. Classification models (ANN, SVM, and ensemble learning) are used to categorize current ratings, while regression models (ANN, ensemble, and GPR) predict continuous current values. These models reduce the functional dependencies between device parameters and average current during training, subsequently enabling continuous predictions based on the learned relationships.

All classification and regression models were implemented in MATLAB® R2025b, using the Statistics and Machine Learning Toolbox. The corresponding model architectures and

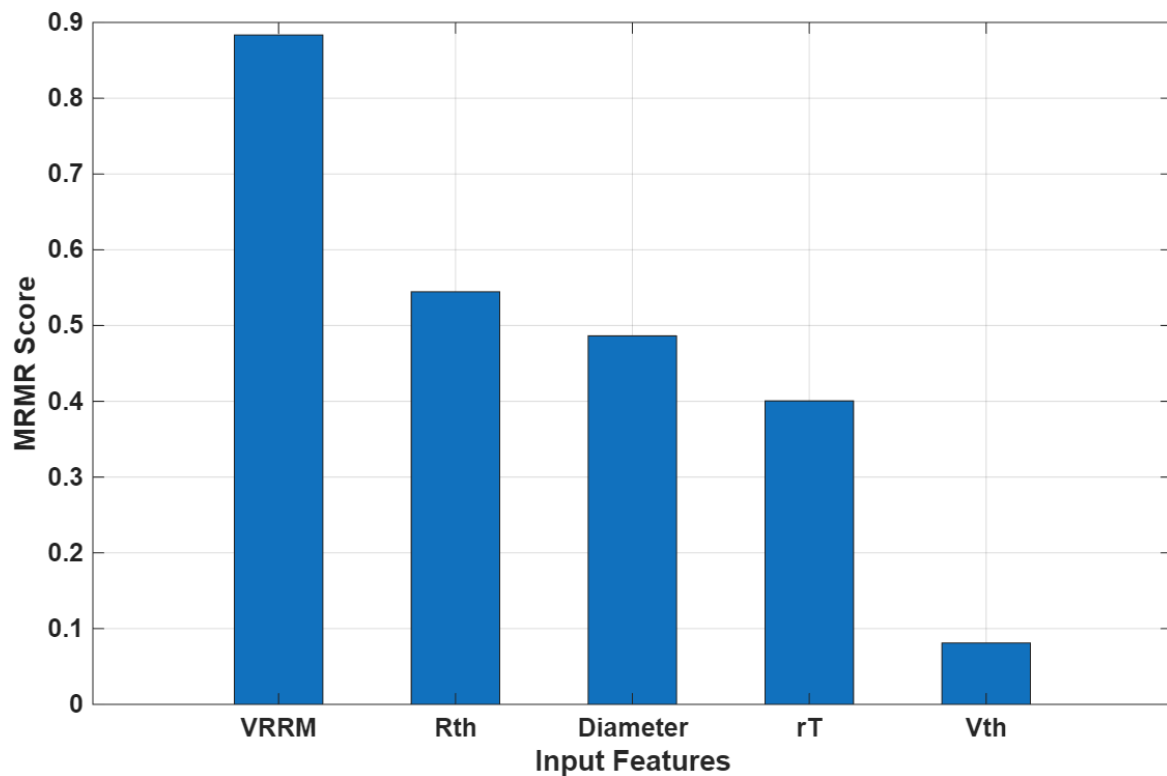


Fig. 7.3 MRMR-based feature ranking showing relevance scores of input features.

configuration parameters are provided in Tables 7.2 and 7.3. Furthermore, to ensure better comparison across these models, identical data partitions were used for all experiments: 90% of the samples were allocated for training and the remaining 10% for testing. Classification performance was evaluated using accuracy, F1-score, precision, and recall, whereas regression performance was assessed using the root-mean-square error (RMSE), mean absolute error (MAE), and the coefficient of determination ( $R^2$ ). Reported results represent the average of five-fold cross-validation to enhance statistical reliability. Hyperparameters for all models were optimized using Bayesian optimization to ensure near-optimal predictive performance.

#### 7.4.1 Artificial Neural Network

In this study, an ANN model is developed for both classification and regression. To classify the average current, a feedforward ANN model with one hidden layer, containing 246 neurons, was developed. To manage the possible nonlinearities in the dataset, a sigmoid activation function was employed to enhance the performance. Moreover, Bayesian optimization was used to select optimal hyperparameters, including the number of layers and neurons, thus ensuring stable convergence and strong generalization across the nine average current classes.

Table 7.2 Architecture of machine learning models for classification models.

| Model    | Property             | Architecture            |
|----------|----------------------|-------------------------|
| Ensemble | Method               | Bag                     |
|          | No. of Splits        | 1050                    |
|          | No. of Learners      | 499                     |
|          | Predictors to sample | 2                       |
| SVM      | Kernel function      | Cubic                   |
|          | Box constraint level | 1.8529                  |
|          | Multiclass coding    | one-vs-one              |
| ANN      | Hidden layers        | 1                       |
|          | Number of neurons    | 246                     |
|          | Activation function  | Sigmoid                 |
|          | Optimizer            | Bayesian optimization   |
|          | Learning rate        | $9.160 \times 10^{-07}$ |

However, to predict the continuous average current values, regression-based ANN models were developed using two architectural configurations: a full-feature model and a reduced-feature model, using a single hidden layer, with 289 neurons in the full-feature architecture and 300 neurons in the reduced-feature model. Moreover, the full-feature model employs a ReLU activation function to enhance nonlinear approximation, and the reduced-feature model uses a sigmoid activation function to improve performance under lower input dimensionality. Bayesian optimization was used to explore network architectures with one to three hidden layers, where each hidden layer contained between 1 and 300 neurons. The activation function was selected from ReLU, tanh, and sigmoid, while the learning rate was optimized over a wide range from  $8.96 \times 10^{-9}$  to 89.6 to accommodate different convergence behaviors. For classification tasks, validation accuracy was used as the optimization objective, whereas for regression tasks the objective was minimization of validation RMSE. Architectures with comparable performance were resolved in favor of simpler configurations to reduce model complexity and mitigate overfitting. The resulting ANN models demonstrated strong performance in both classification and regression, confirming their suitability for modeling the intricate relationships between electrical, thermal, and structural parameters that influence the average current of high-power semiconductor devices.

### 7.4.2 Ensemble Methods

Ensemble learning combines multiple weak learners to enhance predictive accuracy, robustness, and stability. Ensemble models are usually employed with two strategies, bagging and boosting. Bagging was selected for the classification task in this study due to its strong vari-

Table 7.3 Architecture of machine learning models for regression models.

| Model    | Property             | Full Feature Architecture | Reduced Feature           |
|----------|----------------------|---------------------------|---------------------------|
| GPR      | Basis function       | Zero                      | Zero                      |
|          | Kernel function      | Non-isotropic exponential | Non-isotropic exponential |
|          | Kernel scale         | 98.98                     | 975.48                    |
|          | Sigma                | 0.4335                    | 0.0001017                 |
|          | Optimizer            | Bayesian optimization     | Bayesian optimization     |
| Ensemble | Method               | LSBoost                   | Bag                       |
|          | leaf size            | 11                        | 1                         |
|          | Learners             | 170                       | 477                       |
|          | Predictors to sample | 5                         | 3                         |
| ANN      | Hidden layers        | 1                         | 1                         |
|          | No. of neurons       | 289                       | 300                       |
|          | Activation function  | ReLU                      | Sigmoid                   |
|          | Optimizer            | Bayesian optimization     | Bayesian optimization     |
|          | Learning rate        | 0.00025658                | 3.8e-7                    |

ance reduction capability and resilience to noisy data. Moreover, bagging models ensemble by training multiple learners, creating many different training datasets by randomly sampling from the original dataset and aggregating their predictions through majority voting. The ensemble model proposed for classification consists of 499 bagged decision trees, each with a maximum of 1050 splits and two predictors sampled at each node. while the full-featured regression model employs LSBoost with 170 learners and a leaf size of 11 and the reduced feature model with 477 learners and a leaf size. These architectures enhance the performance and stability of the model and mitigate overfitting in data across all classes. Bayesian optimization was applied to both classification and regression, including Bagging, AdaBoost, RUSBoost, and LSBoost methods. The search space included the number of learners ranging from 10 to 500, learning rates between 0.001 and 1, minimum leaf size from 1 to 558 (for regression), and the number of predictors sampled per split between 1 and 5.

### 7.4.3 Support Vector Machine

SVM aims to identify a hyperplane in a multidimensional feature space that maximizes the margin between classes by solving an optimization problem that balances margin maximization with a penalty for misclassifications. The boundary decisions among classes are defined by a specific subset of training instances, referred to as support vectors. In datasets

where nonlinear relationships exist, kernel transformations are used to map the input space into a higher-dimensional feature space, making linear separation possible. In the proposed SVM model for classification of average current, a cubic kernel function, a box constraint of 1.8529, and a one-vs-one multiclass coding scheme are employed, which enable effective separation among all the classes. Furthermore, Bayesian optimization was employed to select the optimal regularization strength and kernel function. The box constraint parameter varied between 0.001 and 1000 to balance margin maximization and misclassification tolerance. Kernel functions considered included gaussian, linear, quadratic, and cubic kernels.

#### 7.4.4 Gaussian Process Regression

Gaussian Process Regression is a nonparametric model based on the Bayesian learning technique and models the relationship between input features and continuous outputs using Gaussian Distribution (GD). GD is defined by a mean function and a covariance kernel. GPR offers two major advantages: (i) it provides smooth function approximations suitable for physical systems, and (ii) it yields uncertainty estimates associated with each prediction. The proposed GPR forecasts the continuous value of the average current based on the electrical and structural features of high-power semiconductor devices. Both the full-feature and reduced-feature configurations employed a zero basis function and a non-isotropic exponential kernel, with kernel scale and noise variance optimized via Bayesian optimization. The optimized kernel scale and sigma were 98.98 and 0.4335, respectively, whereas the reduced-feature configuration has a larger kernel scale (975.48) and a lower noise variance (0.0001017). These configurations enable GPR to capture nonlinear relationships while maintaining smoothness in the predicted output surface. Bayesian optimization was conducted over the noise variance parameter  $\sigma$ , which ranged from 0.0001 to approximately  $2.7 \times 10^4$ . Mean (basis) functions, including constant, zero, and linear forms, were evaluated. The kernel scale was optimized within the range of 0.001 to 1000, and both isotropic and non-isotropic kernel functions were considered, including matern (3/2 and 5/2), rational quadratic, exponential, and squared exponential kernels.

## 7.5 Results and Discussion

### 7.5.1 SHAP-Based Feature Importance and Interpretability

Global feature importance, quantified using SHAP analysis, is shown in Figure 7.4. For each input feature, the mean absolute SHAP value over the entire test dataset was computed to represent its average contribution to the model's predictions. This analysis shows that

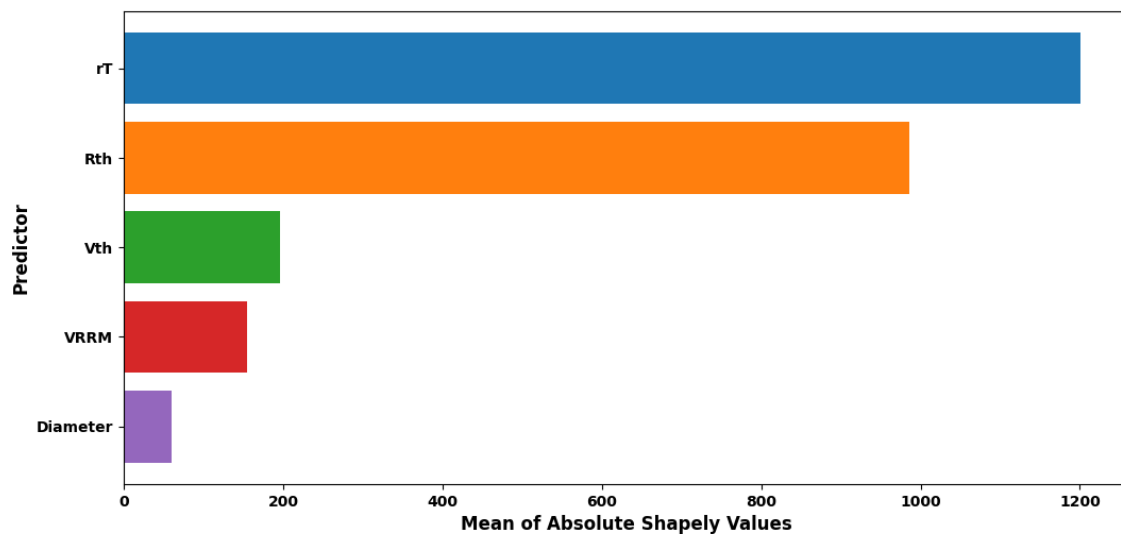


Fig. 7.4 Contribution of feature on output for average current prediction.

$rT$ ,  $R_{th}$ , and  $V_{th}$  exhibit the highest global relevance, consistent with the dominant role of thermal and electrical characteristics in governing current-conduction behavior. In addition, Figure 7.5 presents class-specific SHAP contributions, where mean absolute shapely values are computed separately across different current ranges. The segmented bars highlight how each predictor's influence varies with operating conditions. This class-dependent representation confirms that  $rT$  and  $R_{th}$  dominate consistently across all current classes, while the contributions of device diameter,  $V_{th}$ , and  $V_{RRM}$  fluctuate depending on the operating condition, demonstrating important local variations which are not captured by the global ranking.

### 7.5.2 Classification Performance Evaluation

The result of this study determined that ML algorithms can be used to accurately classify the average current of high-power thyristors. The ensemble model achieved an accuracy of 91.3%, while SVM and ANN classifiers achieved an accuracy of 88.7% and 87.1%, respectively. The performance of all algorithms is satisfactory in this study and achieved an accuracy of over 85% as listed in the Table 7.4. Among the implemented algorithms, the ensemble achieves the best overall performance, delivering 91.3% testing accuracy along with a stable F1-score and recall, i.e., 91.1% across both testing and validation, demonstrating robustness against overfitting. In comparison, the SVM model attains an accuracy of 88.7% with an F1-score and recall of 88.8% and 88.7% respectively, while the ANN reaches the lower accuracy of 87.1% yet suffers from degraded accuracy and F1-score and recall of

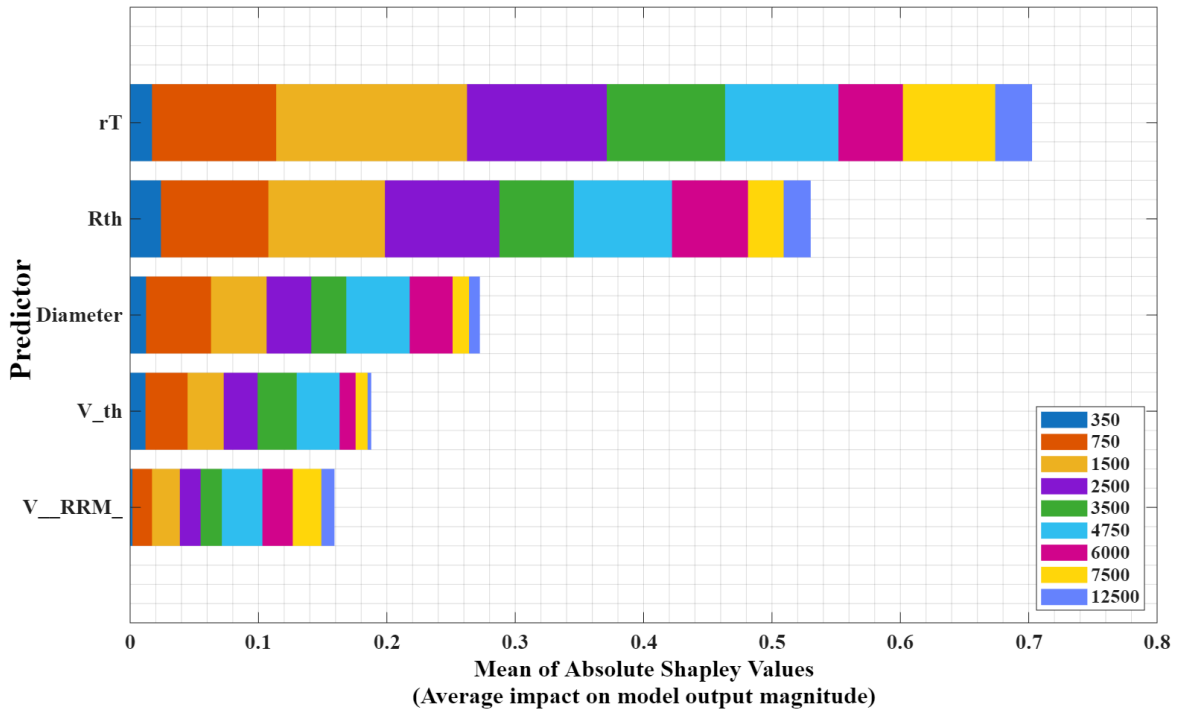


Fig. 7.5 Impact of input features on average current for each class.

87.83% and 87.1% respectively. However, the model is efficient computationally with lower training time and memory. Moreover, the ensemble model also exhibits the lowest validation cost of 11, compared to 14 for SVM and 16 for ANN, resulting in reduced sensitivity to feature tuning and class-boundary effects. While the ensemble model has competitive accuracy, its lower class-specific error rates and enhanced end-to-end feature learning result in increased generalization. The ensemble architecture effectively captures non-linear feature interactions, demonstrating improved generalization within the evaluated dataset, whereas the SVM's accuracy is offset by its computational overhead, as shown in Table 7.5. Overall, the ensemble achieves the best trade-off between accuracy and robustness.

### 7.5.2.1 Confusion Matrix and Metrics

The classification performance of the three models varies across the different average-current classes. The ensemble classifier demonstrates the most consistent behavior, achieving high accuracy for both low and high current classes while exhibiting moderate performance in the mid-range classes. As illustrated in Figure 7.6, the ensemble model attains over 94% accuracy for classes up to 2500 A and reaches 100% accuracy for the highest current classes. However, accuracy decreases to approximately 80% for the mid-range classes between 3500 A and 6000 A, indicating greater overlap in feature distributions within this range, with

Table 7.4 Model performance on validation and test datasets.

| Parameter        | Artificial Neural Network ANN | Ensemble | Support Vector Machines |
|------------------|-------------------------------|----------|-------------------------|
| <b>F1 Score</b>  |                               |          |                         |
| Test             | 87.3                          | 91.3     | 88.8                    |
| Validation       | 88.9                          | 91.1     | 90.7                    |
| <b>Recall</b>    |                               |          |                         |
| Test             | 87.1                          | 91.1     | 88.7                    |
| Validation       | 89.0                          | 91.1     | 90.8                    |
| <b>Accuracy</b>  |                               |          |                         |
| Test             | 87.1                          | 91.1     | 88.7                    |
| Validation       | 89.0                          | 91.1     | 90.8                    |
| <b>Precision</b> |                               |          |                         |
| Test             | 88.8                          | 91.8     | 89.3                    |
| Validation       | 89.0                          | 91.2     | 90.38                   |

Table 7.5 Computational performance metrics for classification.

| Model             | Full Featured Classification |                          |                          |
|-------------------|------------------------------|--------------------------|--------------------------|
|                   | Training Time (s)            | Model Size (kB)          | Prediction Speed (obs/s) |
| Training Time (s) | Model Size (kB)              | Prediction Speed (obs/s) |                          |
| ANN               | 583.43                       | 31                       | 25000                    |
| Ensemble          | 884.86                       | 15                       | 390                      |
| SVM               | 1216.6                       | 52                       | 14000                    |

misclassifications represented by the percentages shown in the green cells. The SVM model exhibits a similar trend but with slightly reduced accuracy at higher current levels. As shown in Figure 7.7, the SVM achieves over 90% accuracy for current classes up to 2500 A and approximately 80% for classes up to 6000 A. For the 12 500 A class, the accuracy decreases to 75%, whereas the ensemble classifier achieves perfect classification for this class. Nevertheless, SVM attains 100% accuracy for selected classes, including 350 A, 2500 A, and 12,500 A. The ANN model shows strong performance at lower current levels and achieves 100% accuracy for the high-current classes at 700 A and 12,500 A, as presented in Figure 7.8. However, its performance degrades for mid-range current levels, where accuracy drops to approximately 70%, indicating challenges in modeling the nonlinear characteristics within this region. Despite this, ANN maintains satisfactory accuracy in the lower-current classes.

Overall, the ensemble method delivers the most stable classification across all current levels, while SVM performs competitively with minor degradation at higher classes. The



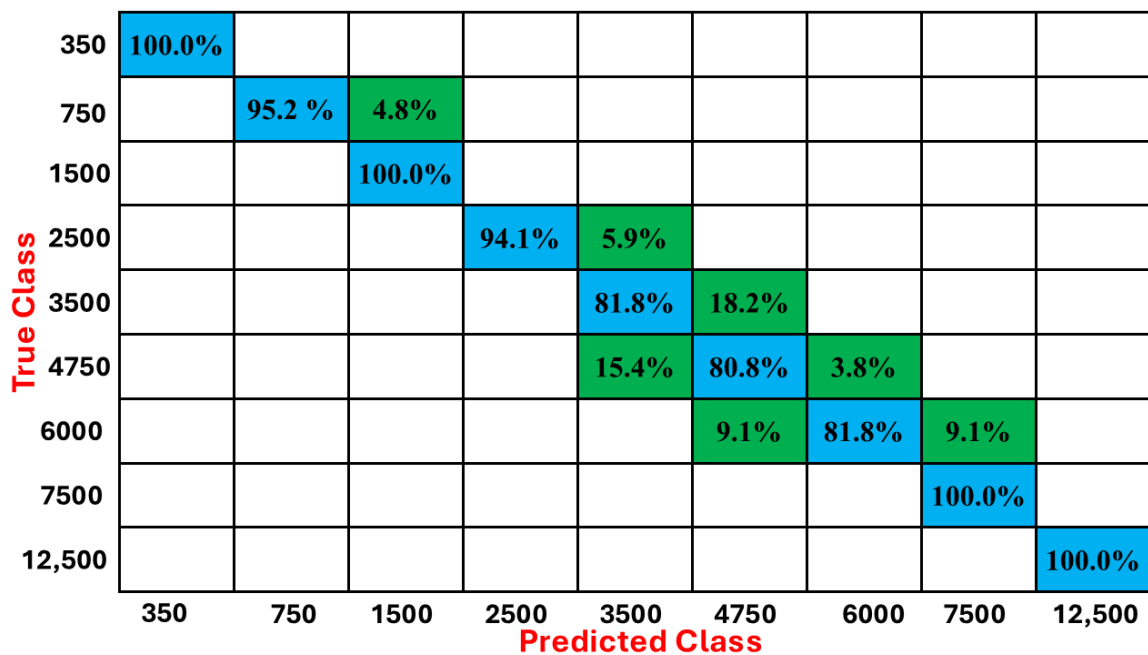


Fig. 7.6 Confusion matrix of average current classification on the test dataset using the ensemble model.

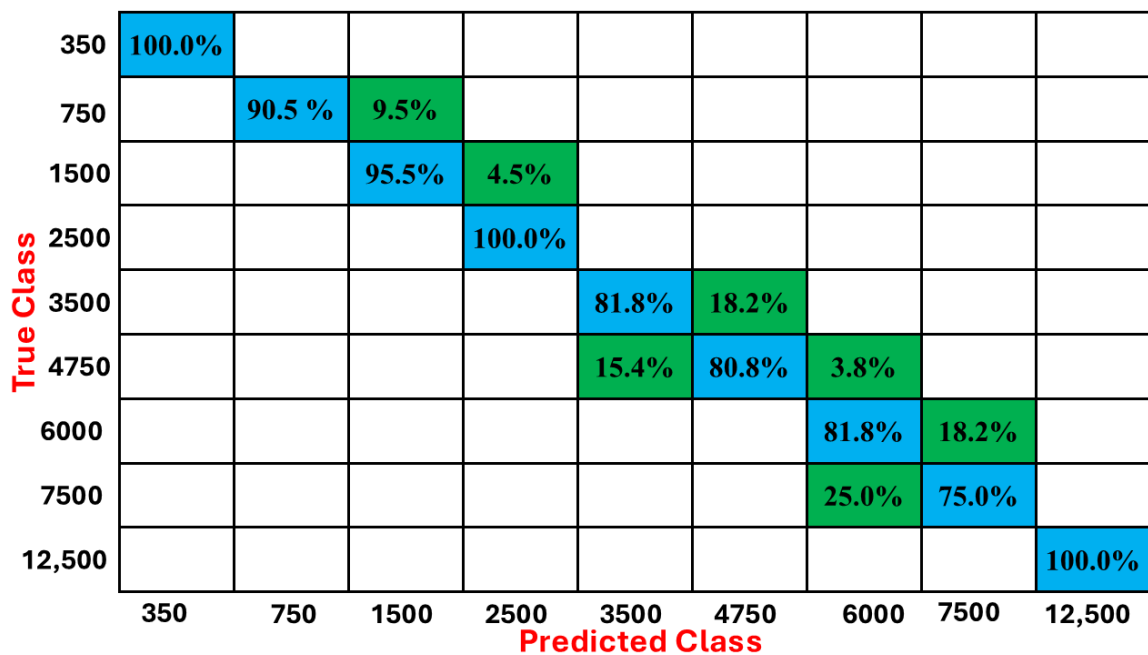


Fig. 7.7 Confusion matrix of average current classification on the test dataset using the SVM model.

ANN exhibits strong performance at the extremes but reduced reliability in the mid-range

classes, emphasizing the sensitivity of neural networks to feature distributions in transitional operating regions.

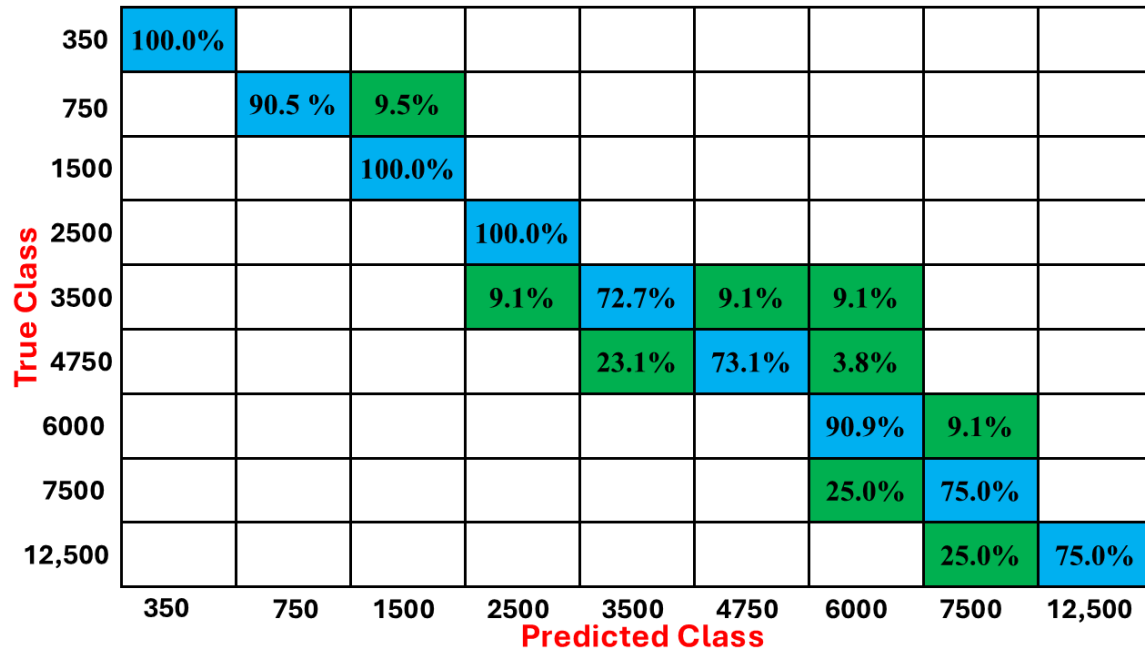


Fig. 7.8 Confusion matrix of average current classification on the test dataset using the ANN model.

### 7.5.3 Average Current Prediction Results

#### 7.5.3.1 Performance of the Artificial Neural Network

The performance of the ANN model was evaluated using both the full-feature and reduced-feature configurations. For the full-featured model, the ANN achieved coefficients of determination ( $R^2$ ) of 0.95 for training and 0.96 for testing, as shown in Table 7.6. The corresponding testing RMSE and MAE values were 501.26 and 353.86, respectively, highlighting good accuracy. The results show that predicted current values align with the overall trend of the true measurements across the full operating range as shown in Figure 7.9a. Moreover, the overlap between the two curves confirms that the ANN successfully captures the underlying nonlinear relationship between the inputs and the output current. This is further confirmed by the strong correlation noted in Figure 7.10a, although slight deviations are noted at higher current levels. The residual analysis in Figure 7.11a further evaluates the model performance; while the residuals remain centered around zero for low and mid-current ranges, the error spread increases substantially at higher current values (above 6000 A), indicating reduced

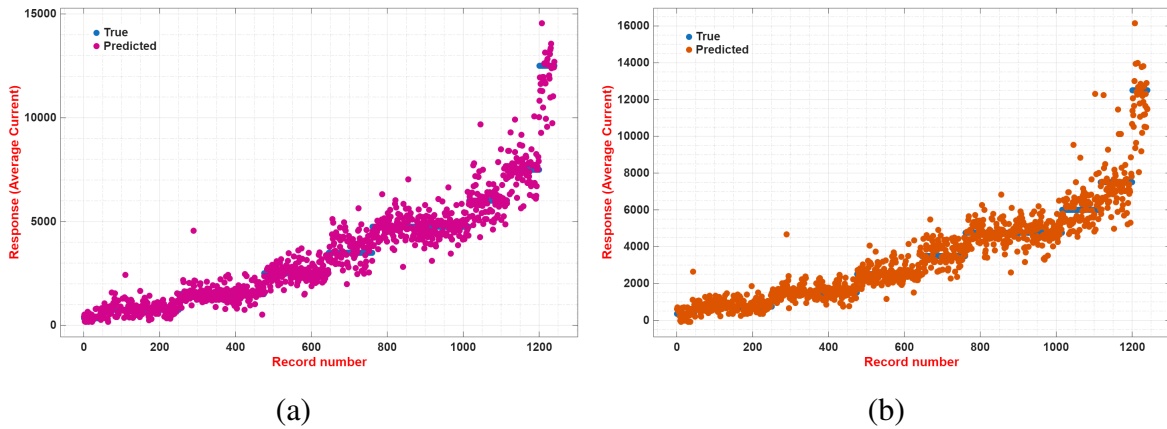


Fig. 7.9 Response plot of ANN (a) Full featured (b) Reduced featured.

accuracy. Furthermore, a small number of few large outliers are also present across some classes, suggesting that the ANN struggles to generalize for extreme operating conditions. Overall, the ANN demonstrates solid predictive capability but exhibits moderate error ampli-

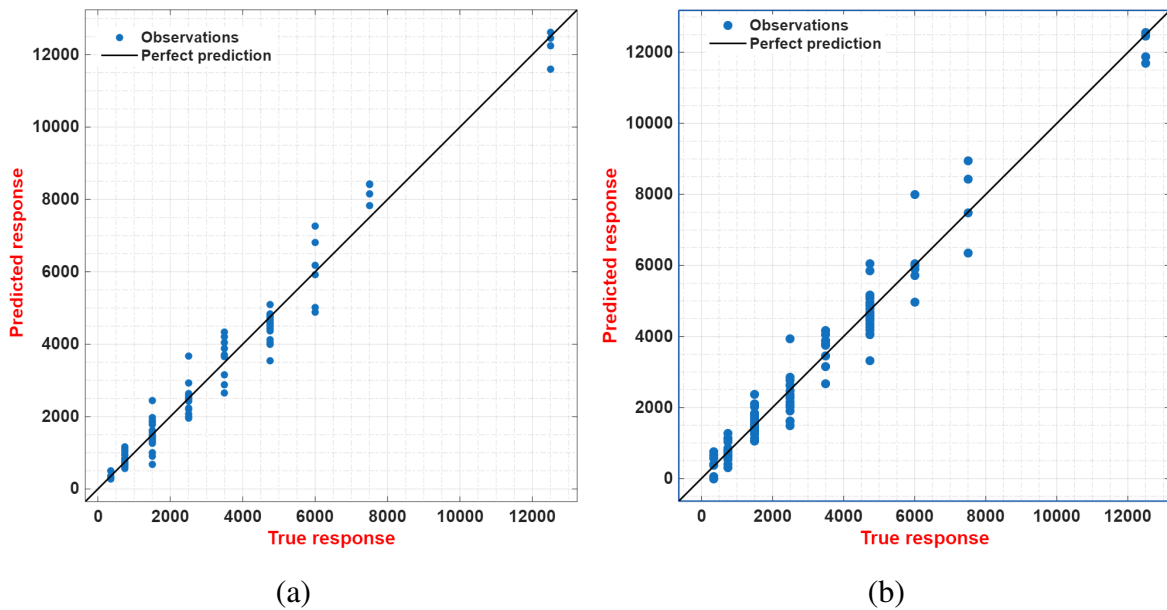


Fig. 7.10 Actual vs predicted of ANN (a) Full featured (b) Reduced featured.

fication as the current approaches the upper end of the range. In contrast, the reduced-feature model resulted in  $R^2$  values of 0.93 for training and 0.91 for testing, with testing MSE and RMSE values of 701.35 and 484.98, respectively, as shown in Table 7.7. Although a small reduction in accuracy was observed, the performance remained comparable to the full-feature configuration, as shown in Figure 7.9b, illustrating the robustness of the selected features. The reduced-feature ANN maintained a high predictive accuracy as presented in Figure

7.10b while achieving slightly improved computational efficiency as given in Table 7.8. The residual analysis in Figure 7.11b shows increased error variance at higher current values; however, the occurrence of large outliers is notably reduced compared with the full-feature configuration. These results establish the ANN as a reliable and high-performing predictor of average current in high-power thyristors. Its ability to extract nonlinear relationships between thermal and electrical characteristics demonstrates its suitability for integration into advanced semiconductor design and reliability assessment frameworks.

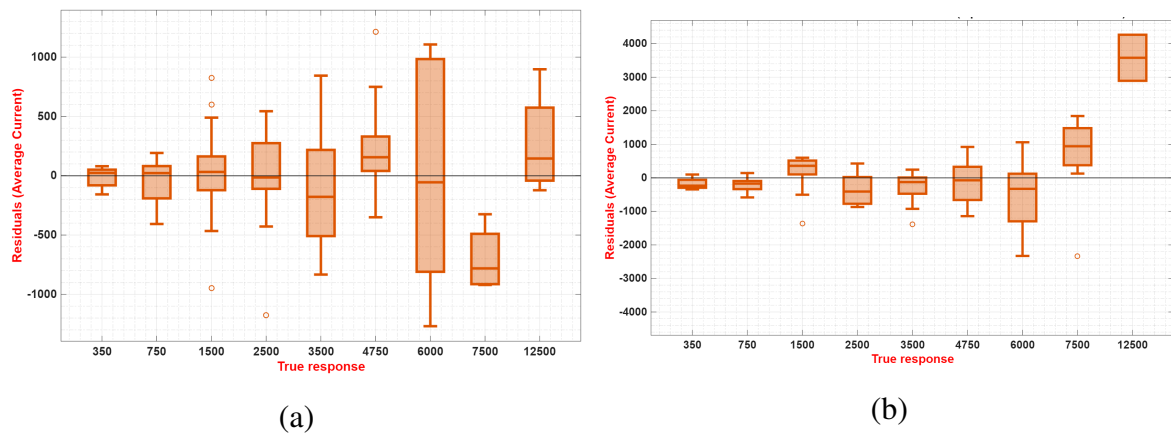


Fig. 7.11 Residual ANN (a) Full featured (b) Reduced featured.

Table 7.6 Comparison of testing and validation performance of regression models.

| Model                     | Data       | $R^2$ | RMSE   | MAE    | MAPE (%) |
|---------------------------|------------|-------|--------|--------|----------|
| GPR                       | Testing    | 0.99  | 296.38 | 164.57 | 6.6      |
|                           | Validation | 0.98  | 352.03 | 208.7  | 7.2      |
| Ensemble                  | Testing    | 0.98  | 400.33 | 259.56 | 9.8      |
|                           | Validation | 0.96  | 510.21 | 318.45 | 10.9     |
| Artificial Neural Network | Testing    | 0.96  | 501.26 | 353.86 | 18.5     |
|                           | Validation | 0.95  | 589.46 | 393.80 | 15.8     |

### 7.5.3.2 Performance of the Optimized Ensemble Model

The ensemble model demonstrated high predictive capability for estimating the average current of high-power thyristors using both the complete full feature set and the reduced feature subset. The full-featured model achieved  $R^2$  values of 0.98 for training and 0.96 for testing, respectively, with corresponding MSE and RMSE given in Tables 7.6 and 7.7. The regression plot given in Figure 7.12a shows tracking of predicted and actual values throughout the dataset, confirming the ability of the model to capture nonlinear dependencies

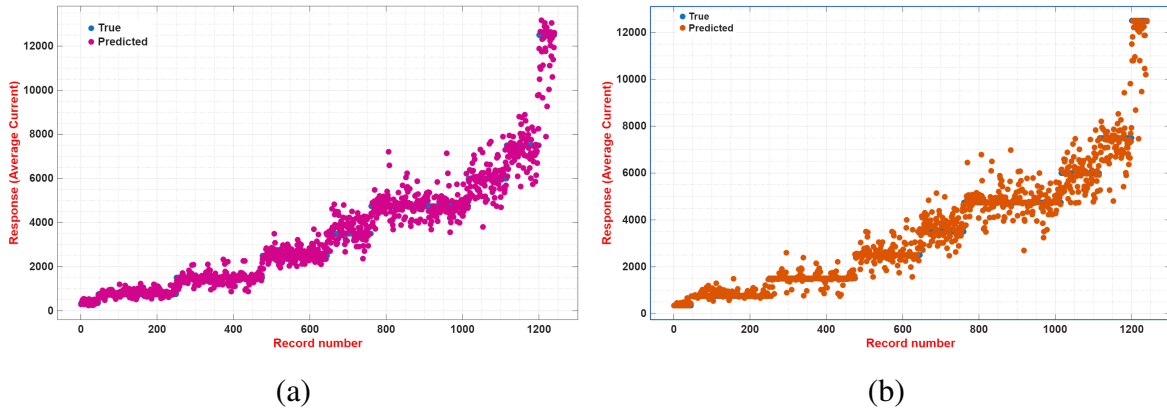


Fig. 7.12 Response plot of ensembles (a) Full featured (b) Reduced featured.

while mitigating overfitting through ensemble averaging. The ensemble model produces more stable residuals across most average current classes, as shown in Figure 7.13a, with fewer extreme deviations compared to ANN. However, it still exhibits a wider error band around 6000–7500 A, suggesting moderate sensitivity to higher current estimations but good accuracy throughout the prediction, as shown in Figure 7.14a. Moreover, the ensemble model has good computational efficiency, as shown in Table 7.8. Using the reduced feature

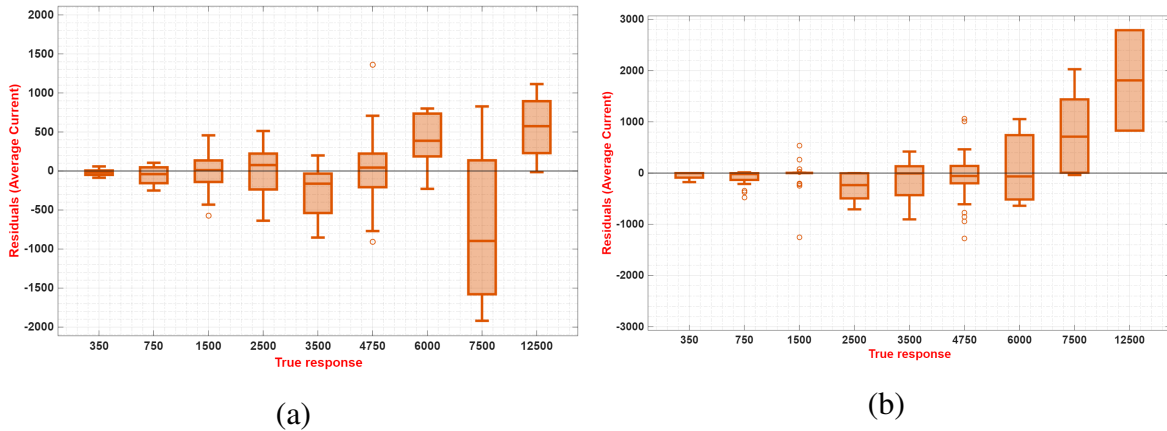


Fig. 7.13 Residual of ensemble (a) Full featured (b) Reduced featured.

configuration, the model maintained almost similar high accuracy as shown in Figure 7.12b with good alignment of predicted values and actual values, yielding  $R^2$  values of 0.96 (training) and 0.95 (testing). Although a slight increase in dispersion was observed at higher current levels as shown in Figure 7.13b by residual analysis. These results confirm that slope resistance ( $rT$ ), thermal resistance ( $R_{th}$ ), and threshold voltage  $V_{th}$  are the dominant predictors of thyristor current-handling capability as shown in Figure 7.14b, highlighting the

robustness and efficiency of the proposed model for modeling in high-power semiconductor devices.

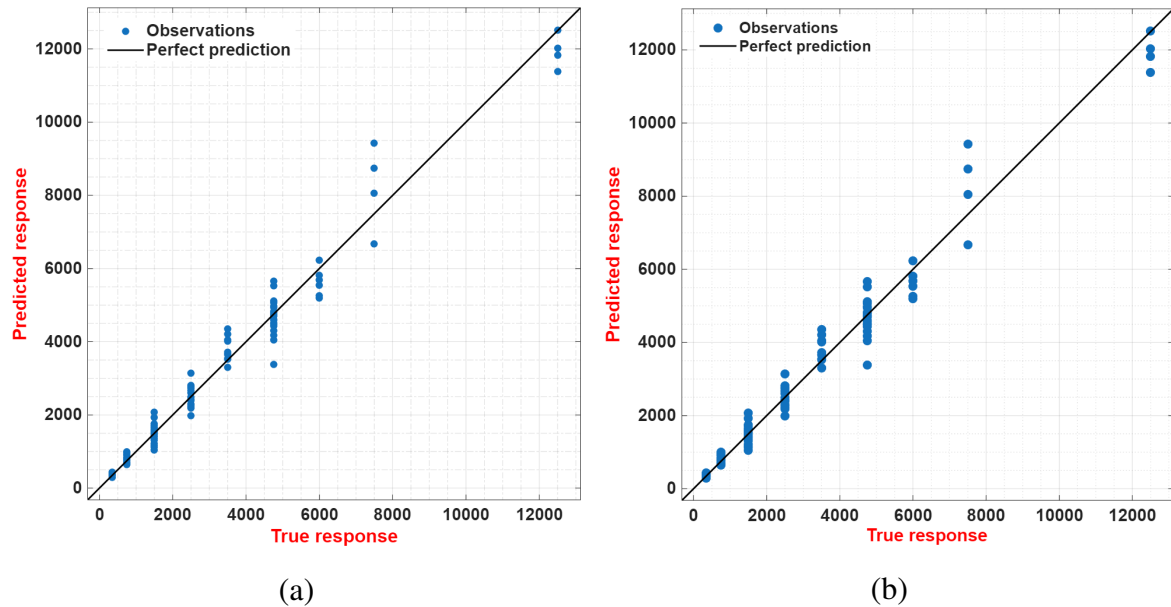


Fig. 7.14 Actual vs predicted of ensemble (a) Full featured (b) reduced featured.

Table 7.7 Comparative testing and validation performance of reduced-feature regression models for average current forecasting.

| Model                     | Data       | $R^2$ | RMSE   | MAE    | MAPE (%) |
|---------------------------|------------|-------|--------|--------|----------|
| GPR                       | Testing    | 0.96  | 446.75 | 244.73 | 7.9      |
|                           | Validation | 0.97  | 493.33 | 280.33 | 10.0     |
| Ensemble                  | Testing    | 0.95  | 540.11 | 305.03 | 9.5      |
|                           | Validation | 0.96  | 519.05 | 283.41 | 8.8      |
| Artificial Neural Network | Testing    | 0.91  | 701.35 | 484.98 | 20.1     |
|                           | Validation | 0.93  | 705.89 | 447.64 | 18.5     |

### 7.5.3.3 Gaussian Process Regression

The GPR model results in the highest predictive performance among all implemented ML models, outperforming both the ANN and ensemble models. Using the full feature set, the GPR achieved  $R^2$  of 0.98 for training and 0.99 for testing, highlighting outstanding accuracy of prediction and a closely matched correspondence between the actual and estimated current values. As shown in Figure 7.15a, the predicted current values perfectly follow the actual values through the entire dataset. The predicted values are obtained with minimal deviation

even in the high current region. Moreover, the response plot employs closer overlap and a lower number of abrupt fluctuations compared with the ANN and ensemble models, indicating a superior ability to capture the underlying nonlinear behavior. These results are

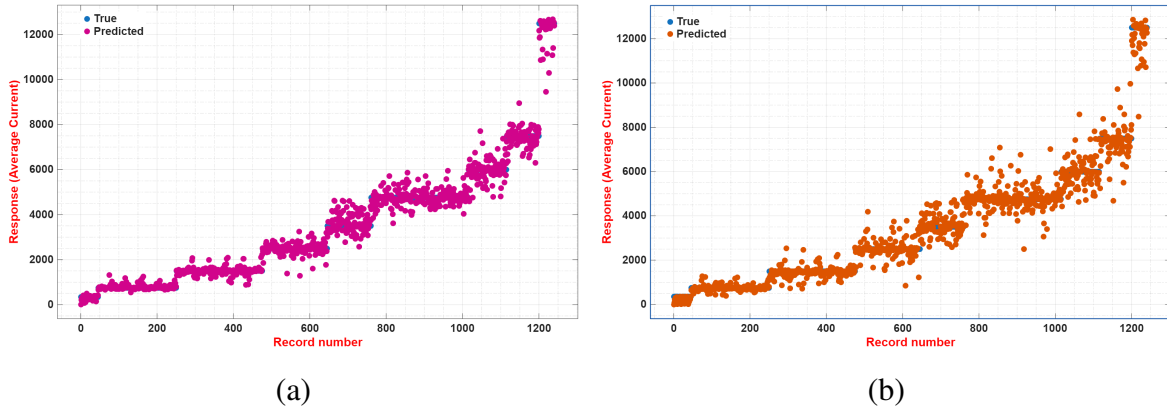


Fig. 7.15 Response plot of GPR (a) Full featured (b) Reduced featured.

further confirmed in Figure 7.16b, which shows that the GPR predictions are concentrated near the line representing exact agreement with the true response. The reduced vertical spread and absence of large misaligned points also highlight improved accuracy and stronger generalization capability. In contrast, the ANN model shows a biased behavior at higher current values, while the ensemble model demonstrates increased dispersion in the errors, particularly near the region of 6000 A, indicating less stable performance across the full operating range. The residual analysis in Figure 7.17a provides clear evidence of the GPR model's superiority. The residuals are smaller, more symmetrically distributed, and exhibit significantly fewer large outliers than those observed in both ANN configurations (5-feature and reduced 3-feature) and the ensemble model. Although a mild increase in error variance appears at higher current values, the overall magnitude and frequency of deviations remain substantially lower. Furthermore, the reduced feature model results in almost the same accuracy as the full feature as presented in Figures 7.15b, 7.16b, and 7.17b, achieving  $R^2$  values of 0.97 for training and 0.96 for testing as presented in Table 7.7. This shows that the average current of a device depends significantly on the reduced feature, and also the model keeps most of its predictive performance even with fewer significant input contributing parameters, which highlights its robustness and reduced sensitivity to feature dimensionality.

In summary, the proposed GPR model exhibits the best predictive capability among all implemented models, the most stable residual behavior, and the strongest alignment with true responses. Moreover, as shown in Figure 7.18, the 95% confidence intervals are well calibrated, achieving 95.2% coverage, with relative predictive uncertainty remaining below

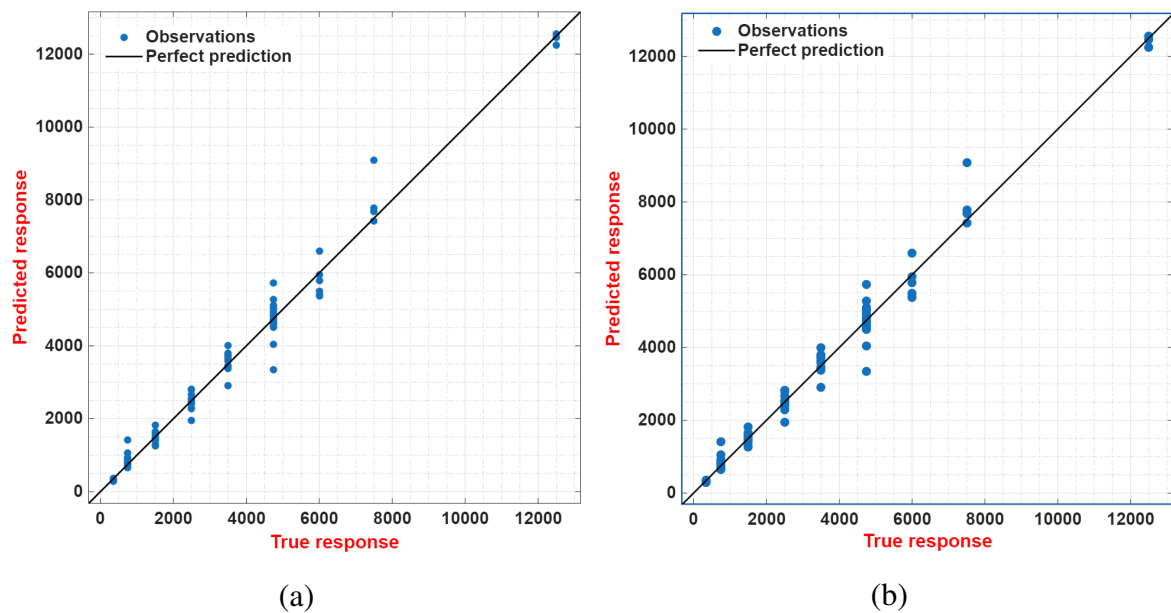


Fig. 7.16 Actual vs predicted of GPR (a) Full featured (b) reduced featured.

Table 7.8 Computational performance metrics for prediction: Full featured and reduced featured.

| Model    | Full Featured Prediction |                 |                          | Reduced Featured Prediction |                 |                          |
|----------|--------------------------|-----------------|--------------------------|-----------------------------|-----------------|--------------------------|
|          | Training Time (s)        | Model Size (kB) | Prediction Speed (obs/s) | Training Time (s)           | Model Size (kB) | Prediction Speed (obs/s) |
| GPR      | 1661.7                   | 55              | 24000                    | 1256                        | 38              | 39000                    |
| Ensemble | 47.9                     | 185             | 12000                    | 63.7                        | 40000           | 2900                     |
| ANN      | 656.22                   | 18              | 47000                    | 188.38                      | 13              | 47000                    |

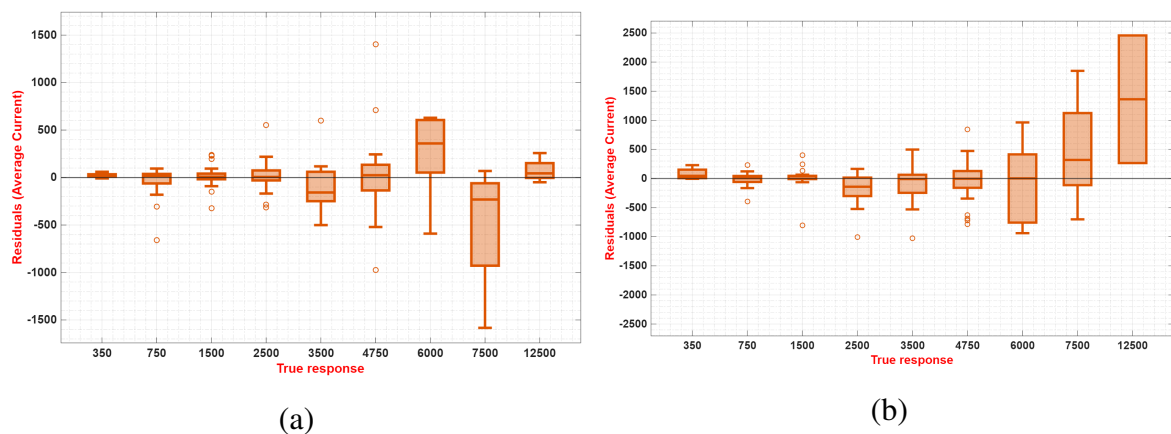


Fig. 7.17 Residual of GPR (a) Full featured (b) Reduced featured.

15%. Its strong performance under both full and reduced feature configurations confirms its suitability and effectiveness for accurate average current estimation, thus offering a useful tool for design and manufacturing.



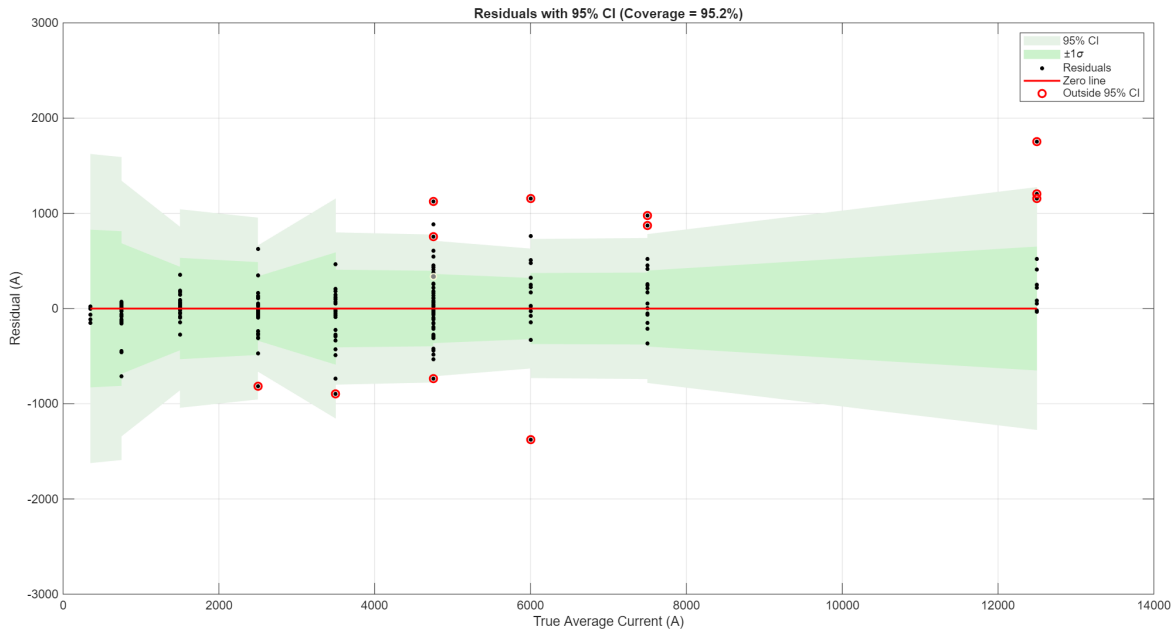


Fig. 7.18 Predicted responses with associated 95% confidence intervals from the GPR model.

## 7.6 Conclusion

This study applies ML techniques to classify and predict the average current in high-power semiconductor devices, including thyristors. The average current values were categorized into nine different classes. Moreover, multiple ML were implemented to perform both discrete classification and continuous prediction. In addition, SHAP-based interpretability analysis was also performed. Furthermore, the performance of all implemented models was evaluated and compared by using standard metrics. For the classification, the ensemble-based model demonstrates superior performance with the highest accuracy and F1-score over 91% as compared to other models, while for regression, the GPR model achieves high prediction accuracy. The GPR model attained an  $R^2$  of 0.99 with a test MAPE of 6.6% for the full-feature model and maintained strong performance under reduced-feature conditions ( $R^2 = 0.96$ ). Future work could include estimating the device's junction temperature at different current levels, which would further enhance device reliability and operational safety.

### Publication Related to this Chapter

This chapter reproduces material from the following publication:

**F. Ahmad**, L. Vaccaro, A. A. Nkembi, M. Marchesoni, and F. Portesine, “*Classification and Prediction of Average Current in High-Power Semiconductor Devices: A Machine Learning Framework*,” **Electronics**, vol. 15, no. 6, p. 1149, Mar. 2026. DOI: [10.3390/electronics15061149](https://doi.org/10.3390/electronics15061149)



# **Chapter 8**

## **Conclusions and Future Research Directions**

### **8.1 Overview**

This thesis investigates the electro-thermal behavior, surge current robustness, packaging influence, and data-driven design methodologies for high-power semiconductor devices. The work focus to combines physics-based electro-thermal modeling, experimental validation, comparative packaging analysis, and ML techniques to encounter key challenges associated with high-power semiconductor device design and reliability. The research progresses from analytical thermal modeling to surge current analysis and finally to data-driven design approaches. The main findings and contributions are summarized in the following sections.

### **8.2 Summary of Findings and Main Contributions**

This thesis has made substantial contributions in multiple areas, from thermal characterization of high power press pack diodes to innovative electrothermal modeling and surge reliability. Each of these contributions has been developed to address specific challenges in high-power diode, and are summarized below:

#### **8.2.1 Electro-Thermal Modeling of High-Power Devices**

- An electrothermal model is developed to accurately predict transient thermal impedance of high power press-pack diodes
- Cauer thermal network is implemented in PSIM to perform simulations.

- Cauer model is transformed to a Foster thermal network using MATLAB<sup>®</sup> curve fitting to extract thermal resistances and time constants from simulation results.
- Experimental setup was established, and measurements were performed to validate the model results.

### **8.2.2 Surge Current Analysis**

- An electro-thermal model was proposed to estimate forward voltage drop and predict junction temperature under high surge conditions
- Rated electrical parameters are integrated with thermal simulation data to develop the model.
- A series of experimental surge tests were conducted for proposed model validation.
- Simulations were performed in PSIM and ANSYS to estimate device temperature rise. The model enables understanding of surge current behavior and reliability limits of the device.

### **8.2.3 Packaging Technology Comparison**

- PCT press-pack diodes and PCT diode modules were tested under surge conditions to investigate the effect of packaging on thermal behavior and surge withstand capability.
- A surge wave generator producing a 10 ms half-sine waveform was developed to conduct experimental testing.
- The device failure behavior was investigated, and the forward voltage and current waveforms were recorded during surge events. The junction temperature was estimated using electro-thermal simulations.

### **8.2.4 Data-Driven Design Using Machine Learning**

- Dataset of high-current diodes and thyristors is generated from leading manufacturer datasheets.
- Data augmentation is applied to extend the dataset.

- Various ML models, including ANN, SVM, GPR, and ensemble, were implemented to classify and predict chip diameter.
- ML models were applied to classify and predict the average current of high-power semiconductor devices.
- SHAP analysis was employed for model interpretability.

### **8.3 Possible Improvements and Future Direction**

From the research carried out in this thesis, there exist possibilities to extend the work done and improve its applicability. Some of the further research directions which have been identified are summarized below:

#### **8.3.1 Extension to Wide-Bandgap and Multi-Chip Architectures**

Electro-thermal modeling framework can be extended to develop accurate models for next-generation power devices, including wide-bandgap materials such as SiC, improving the design and reliability assessment. Thermal behavior and performance can be investigated in multi-chip module architectures under different operating conditions.

#### **8.3.2 Statistical Surge Reliability Assessment**

Further studies on the development of statistical models may be conducted to predict device reliability under repeated surge events and inform design decisions. Systematic surge testing can be performed across multiple devices to study performance variability. Moreover, the variability in surge failure thresholds and potential weak areas exposed to failure can also be identified.

#### **8.3.3 Interface Effects and Aging Considerations**

Further research is required to investigate the thermal behavior of semiconductor devices occurring due to the influence of interface parameters, such as clamping force, surface conditions, and contact quality, on device thermal behavior. Apart from this, the impact of aging, performance degradation, and long-term operation on packaging materials is also critical and should be studied to improve predictive models for long-term reliability and lifetime assessment of high-power devices.

### **8.3.4 Extensions of Machine Learning Frameworks**

To enhance the training robustness of models, the dataset should be expanded by including additional device parameters and operating conditions. Moreover, advanced ML models can be employed to predict thermal behavior, junction temperature, and failure analysis of high power devices under high anomalous surge current. Integration of ML predictions with electro-thermal simulations for hybrid modeling approaches to enable intelligent design and optimization of semiconductor devices, reducing experimental iterations and improving reliability.

## **8.4 Final Remarks**

The results presented in this thesis considerably advance the understanding of electro thermal behavior and reliability of high-power semiconductor devices. Through the development of analytical and simulation-based modeling approaches, this work provides effective methods for estimating transient thermal impedance, junction temperature, and device performance under surge current conditions. The reliability of the proposed methodologies are further strengthen by experimental validation. Moreover, comparative study of different packaging technologies are conducted to analyze critical role of device structure, highlighting thermal performance and surge robustness. Furthermore, the applications of ML techniques was employed to classify and predict crucial parameters of device that enables optimized design and reliability. Overall, the contributions of this thesis offer practical tools and insights to enhance performance of high power semiconductor devices, such as thermal management, reliability assessment, and design. Future research can extend these approaches to new generation emerging semiconductor technologies, larger datasets, and advanced modeling frameworks to develop more efficient and reliable power electronic devices.

# References

- [1] L. Yu, L. Xu, J. Zhu, and R. Li, “Impedance modelling and stability analysis of diode-rectifier based hvdc connected offshore wind farms,” *IEEE Transactions on Power Delivery*, vol. 37, no. 1, pp. 591–602, 2022.
- [2] M. Marchesoni and L. Vaccaro, “Study of the circulating current in the modular multilevel converter for optimal operation mode in hvdc application,” in *EPE-ECCE 2015*, 2015, pp. 8–10.
- [3] A. Benevieri, L. Carbone, S. Cosso, K. Kumar, M. Marchesoni, M. Passalacqua, and L. Vaccaro, “Series architecture on hybrid electric vehicles: A review,” *Energies*, vol. 14, no. 22, p. 7672, 2021.
- [4] A. A. Nkembi, D. Santoro, F. Ahmad, I. Kortabarria, P. Cova, E. Sacchi, and N. Delmonte, “Novel droop-based techniques for dynamic performance improvement in a linear active disturbance rejection controlled-dual active bridge for fast battery charging of electric vehicles,” *Energies*, vol. 17, no. 20, p. 5171, 2024.
- [5] M. Wang, X. Yang, S. Li, Y. Zhu, W. Feng, and T. Q. Zheng, “High voltage dc auto-transformer traction power supply for braking energy utilization, rail potential, and stray current mitigation,” *IEEE Transactions on Transportation Electrification*, vol. 8, no. 3, pp. 3960–3976, 2022.
- [6] A. A. Khan, U. A. Khan, H. F. Ahmed, H. Cha, and S. Ahmed, “Improved npc inverters without short-circuit and dead-time issues,” *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 2180–2190, 2022.
- [7] M. A. Hosseinzadeh, M. Sarebanzadeh, C. F. Garcia, E. Babaei, J. Rodriguez, and R. Kennel, “Reduced multisource switched-capacitor multilevel inverter topologies,” *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 647–14 666, 2022.
- [8] I. Harbi, J. Rodriguez, A. Poorfakhraei, H. Vahedi, M. Guse, M. Trabelsi, M. Abdelrahman, M. Ahmed, M. Fahad, C.-H. Lin *et al.*, “Common dc-link multilevel converters: Topologies, control and industrial applications,” *IEEE Open Journal of Power Electronics*, vol. 4, pp. 512–538, 2023.
- [9] H. Gui, R. Chen, J. Niu, Z. Zhang, L. M. Tolbert, F. F. Wang, B. J. Blalock, D. Costinett, and B. B. Choi, “Review of power electronics components at cryogenic temperatures,” *IEEE transactions on power electronics*, vol. 35, no. 5, pp. 5144–5156, 2019.

- [10] F. Roccaforte, P. Fiorenza, G. Greco, R. L. Nigro, F. Giannazzo, F. Iucolano, and M. Saggio, "Emerging trends in wide band gap semiconductors (sic and gan) technology for power devices," *Microelectronic Engineering*, vol. 187, pp. 66–77, 2018.
- [11] S. A. Rizzo and N. Salerno, "Actual reasons involving turn-off losses improvement with increasing load and gate resistance in mosfets enhanced with kelvin source," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 1, pp. 369–379, 2023.
- [12] V. V. Obreja, "On the reliability of power silicon rectifier diodes above the maximum permissible operation junction temperature," in *2006 IEEE International Symposium on Industrial Electronics*, vol. 2, 2006, pp. 835–840.
- [13] A. Benmansour, S. Azzopardi, J.-C. Martin, and E. Woirgard, "Trench igbt failure mechanisms evolution with temperature and gate resistance under various short-circuit conditions," *Microelectronics Reliability*, vol. 47, no. 9-11, pp. 1730–1734, 2007.
- [14] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, "Condition monitoring: A decade of proposed techniques," *IEEE Industrial Electronics Magazine*, vol. 9, no. 4, pp. 22–36, 2015.
- [15] N. Dhameliya, "Power electronics innovations: Improving efficiency and sustainability in energy systems," *Asia Pacific Journal of Energy and Environment*, vol. 9, no. 2, pp. 71–80, 2022.
- [16] J. Hu, Y. Shan, K. W. Cheng, and S. Islam, "Overview of power converter control in microgrids—challenges, advances, and future trends," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9907–9922, 2022.
- [17] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 4212–4228, 2015.
- [18] A. Bindra, "Driven by density, efficiency at low cost, power integration reaches new heights: Psips and pwrsocs are growing faster than the traditional power supplies," *IEEE Power Electronics Magazine*, vol. 9, no. 1, pp. 14–19, 2022.
- [19] X. Liang and M. Abbasipour, "Hvdc transmission and its potential application in remote communities: Current practice and future trend," *IEEE Transactions on Industry Applications*, vol. 58, no. 2, pp. 1706–1719, 2022.
- [20] N. M. Manousakis, P. S. Karagiannopoulos, G. J. Tsekouras, and F. D. Kanellos, "Integration of renewable energy and electric vehicles in power systems: a review," *Processes*, vol. 11, no. 5, p. 1544, 2023.
- [21] A. Kochanek, T. Załona, I. Pietrucha, A. Petryk, U. Ziemiańczyk, Z. Basak, P. Guzdek, L. Akbulut, A. Atilgan, and A. D. Woźniak, "Renewable energy integration in sustainable transport: A review of emerging propulsion technologies and energy transition mechanisms," *Energies*, vol. 18, no. 24, p. 6610, 2025.
- [22] N. Wang, B. Li, Y. Wang, Y. Jiao, F. Deng, R. Li, and D. Xu, "A high-power mvac-lvdc rectifier empowering wide voltage range operation," *IEEE Transactions on Power Electronics*, vol. 40, no. 5, pp. 6963–6976, 2025.



- [23] S. Korotkov, Y. Aristov, A. Zhmodikov, and D. Korotkov, "High-voltage closing switches with nanosecond switching time based on shock ionization dynistors connected in series," *IEEE Transactions on Plasma Science*, vol. 51, no. 5, pp. 1320–1324, 2023.
- [24] Y. Baazizi, L. Ferreira, S. Meunier, T. Phulpin, and L. Quéval, "Experimental study of a three-phase diode rectifier operating at cryogenic temperature," *IEEE Transactions on Applied Superconductivity*, vol. 34, no. 3, pp. 1–5, 2024.
- [25] A. Nadermohammadi, P. Abolhassani, A. Seifi, M. Zarrinehbaban, P. Aghakhanlou, S. H. Hosseini, and M. Sabahi, "Cost-effective soft-switching ultra-high step-up dc–dc converter with high power density for dc microgrid application," *Scientific Reports*, vol. 14, no. 1, p. 20407, 2024.
- [26] A. Pragati, M. Mishra, P. K. Rout, D. A. Gadanayak, S. Hasan, and B. R. Prusty, "A comprehensive survey of hvdc protection system: fault analysis, methodology, issues, challenges, and future perspective," *Energies*, vol. 16, no. 11, p. 4413, 2023.
- [27] B. Zhang, Y. Zhong, P. Cui, Y. Cui, M. Xu, H. Linewih, and J. Han, "The surge current failure and thermal analysis of 4h-sic schottky barrier diode," *IEEE Transactions on Electron Devices*, vol. 71, no. 6, pp. 3805–3810, 2024.
- [28] F. Profumo, A. Tenconi, S. Facelli, and B. Passerini, "Instantaneous junction temperature evaluation of high-power diodes (thyristors) during current transients," *IEEE Transactions on Power electronics*, vol. 14, no. 2, pp. 292–299, 2002.
- [29] B. Zhao, Z. Wang, Q. Wang, Y. Wen, B. Gu, Z. Dongye, and L. Qi, "Experimental investigation of temperature distribution in igbt modules," in *IET Conference Proceedings CP964*, vol. 2025, no. 42. IET, 2025, pp. 35–39.
- [30] M. Akbari, A. S. Bahman, P. D. Reigosa, L. Ceccarelli, F. Iannuzzo, and M. Tavakoli, "Non-uniform temperature distribution implications on thermal analysis accuracy of si igbts and sic mosfets," in *2018 24rd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*. IEEE, 2018, pp. 1–6.
- [31] C. S. Thomas, "Transportation options in a carbon-constrained world: Hybrids, plug-in hybrids, biofuels, fuel cell electric vehicles, and battery electric vehicles," *International Journal of hydrogen energy*, vol. 34, no. 23, pp. 9279–9296, 2009.
- [32] C. Cunanan, M.-K. Tran, Y. Lee, S. Kwok, V. Leung, and M. Fowler, "A review of heavy-duty vehicle powertrain technologies: Diesel engine vehicles, battery electric vehicles, and hydrogen fuel cell electric vehicles," *Clean Technologies*, vol. 3, no. 2, pp. 474–489, 2021.
- [33] M. Elkelawy, H. Alm ElDin Mohamad, M. Samadony, A. M. Elbanna, and A. M. Safwat, "A comparative study on developing the hybrid-electric vehicle systems and its future expectation over the conventional engines cars," *Journal of Engineering Research*, vol. 6, no. 5, pp. 21–34, 2022.
- [34] E. Sangeetha and V. Ramachandran, "Different topologies of electrical machines, storage systems, and power electronic converters and their control for battery electric vehicles—a technical review," *Energies*, vol. 15, no. 23, p. 8959, 2022.

- [35] P. Dini, S. Saponara, and A. Colicelli, "Overview on battery charging systems for electric vehicles," *Electronics*, vol. 12, no. 20, p. 4295, 2023.
- [36] A. S. Veerendra, M. R. B. Mohamed, and F. P. García Márquez, "Energy management control strategies for energy storage systems of hybrid electric vehicle: A review," *Energy storage*, vol. 6, no. 1, p. e573, 2024.
- [37] S. Augustine, S. Brahma, J. E. Quiroz, and M. J. Reno, "Dc microgrid protection: Review and challenges," 2018.
- [38] M. Borecki and M. Ciuba, "Testing of selected surge protection devices in the context of the possibility of ensuring the reliability of power grids," *Energies*, vol. 16, no. 3, p. 1445, 2023.
- [39] S. Shaikh, D. Kumar, A. Hakeem, and A. M. Soomar, "Protection system design of induction motor for industries," *Modelling and simulation in engineering*, vol. 2022, no. 1, p. 7423018, 2022.
- [40] M. Buffolo, D. Favero, A. Marcuzzi, C. De Santi, G. Meneghesso, E. Zanoni, and M. Meneghini, "Review and outlook on gan and sic power devices: Industrial state-of-the-art, applications, and perspectives," *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1344–1355, 2024.
- [41] S. S. H. Rafin, R. Ahmed, M. A. Haque, M. K. Hossain, M. A. Haque, and O. A. Mohammed, "Power electronics revolutionized: A comprehensive analysis of emerging wide and ultrawide bandgap devices," *Micromachines*, vol. 14, no. 11, p. 2045, 2023.
- [42] S. K. Mazumder, L. F. Voss, K. M. Dowling, A. Conway, D. Hall, R. J. Kaplar, G. W. Pickrell, J. Flicker, A. T. Binder, S. Chowdhury *et al.*, "Overview of wide/ultrawide bandgap power semiconductor devices for distributed energy resources," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 4, pp. 3957–3982, 2023.
- [43] F. Carastro, J. Mari, T. Zoels, B. Rowden, P. Losee, and L. Stevanovic, "Investigation on diode surge forward current ruggedness of si and sic power modules," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*. IEEE, 2016, pp. 1–10.
- [44] S. I. Rahman, A. Moghassemi, A. Arsalan, L. Timilsina, P. K. Chamarthi, B. Papari, G. Ozkan, and C. S. Edrington, "Emerging trends and challenges in thermal management of power electronic converters: A state of the art review," *IEEE Access*, vol. 12, pp. 50 633–50 672, 2024.
- [45] X. Du, J. Zhang, G. Li, Y. Yu, C. Qian, and R. Du, "Thermal fatigue failure mechanism of igbt module," in *Thermal Reliability of Power Semiconductor Device in the Renewable Energy System*. Springer, 2022, pp. 17–33.
- [46] M. Ishiko, K. Hotta, S. Kawaji, T. Sugiyama, T. Shouji, and T. Fukami, "Investigation of igbt turn-on failure under high applied voltage operation," *Microelectronics and reliability*, vol. 44, no. 9-11, pp. 1431–1436, 2004.

- [47] U.-M. Choi, F. Blaabjerg, and S. Jørgensen, "Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, 2017.
- [48] D. C. Katsis and J. D. van Wyk, "Void-induced thermal impedance in power semiconductor modules: Some transient temperature effects," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1239–1246, 2003.
- [49] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE transactions on power electronics*, vol. 25, no. 11, pp. 2734–2752, 2010.
- [50] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for sic power converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7765–7794, 2019.
- [51] A. S. Bahman, K. Ma, and F. Blaabjerg, "Thermal impedance model of high power igt modules considering heat coupling effects," in *2014 International Power Electronics and Application Conference and Exposition*. IEEE, 2014, pp. 1382–1387.
- [52] B. Heinze, J. Lutz, M. Neumeister, R. Rupp, and M. Holz, "Surge current ruggedness of silicon carbide schottky-and merged-pin-schottky diodes," in *2008 20th International Symposium on Power Semiconductor Devices and IC's*. IEEE, 2008, pp. 245–248.
- [53] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, "Semiconductor power devices," *Physics, characteristics, reliability*, vol. 2, 2011.
- [54] Y. Lu, E. Xiang, Y. Jin, H. Luo, H. Yang, W. Li, and R. Zhao, "A 3-d temperature-dependent thermal model of igt modules for electric vehicle application considering various boundary conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 6, pp. 5463–5475, 2024.
- [55] B. Gao, F. Yang, M. Chen, L. Ran, I. Ullah, S. Xu, and P. Mawby, "A temperature gradient-based potential defects identification method for igt module," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2227–2242, 2016.
- [56] A. H. Okilly, P. N. Harmony, C. Kim, D.-W. Kim, and J. Baek, "Estimation of peak junction hotspot temperature in three-level tnp-igt modules for traction inverters through chip-level modeling and experimental validation," *Energies*, vol. 18, no. 14, p. 3829, 2025.
- [57] S. Zhao, X. Yang, X. Wu, Y. Zhang, and G. Liu, "Investigation on fatigue mechanism of solder layers in igt modules under high temperature gradients," *Microelectronics Reliability*, vol. 141, p. 114901, 2023.
- [58] Y. Kang, L. Dang, L. Yang, Z. Wang, Y. Meng, S. Li, Y. Sun, Y. Wang, and H. Dong, "Research progress in failure mechanism and health state evaluation index system of welded igt power modules," *Electronics*, vol. 12, no. 15, p. 3248, 2023.
- [59] S. Zhao, Y. Tong, C. Wang, and E. Yao, "Challenges and progress in packaging materials for power modules with high operation temperature," *Journal of Materials Science: Materials in Electronics*, vol. 35, no. 35, p. 2237, 2024.

- [60] Q. Li, Y.-B. Li, H.-D. Fu, C.-M. Tu, B. Xiao, F. Xiao, D.-Y. Zhai, and J.-W. Lu, "Review of the failure mechanism and methodologies of igbt bonding wire," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 13, no. 7, pp. 1045–1057, 2023.
- [61] T. Han, Y. Luo, B. Liu, H. Yuan, and Z. Shi, "Thermal balance-based evaluation method for safe operating areas and its degradation of igbt power module," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2025.
- [62] X. Jiang, T. Fan, Z. Qiu, D. Zheng, G. He, P. Ning, and X. Wen, "Lifetime prediction of high-current igbt modules considering bond wire degradation under non-constant stress," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2025.
- [63] Z. Xiang, T. Luo, W. Wang, B. Sun, B. Sun, Q. Zhang, G. Zhang, and J. Fan, "Package-level electro-thermal simulation with transient thermal resistance model for surge stress failure analysis of sic mosfet," *IEEE Transactions on Device and Materials Reliability*, 2026.
- [64] T. Basler, J. Lutz, R. Jakob, and T. Brückner, "Surge current capability of igbts," in *International Multi-Conference on Systems, Signals & Devices*. IEEE, 2012, pp. 1–6.
- [65] H. Guan, Y. Chang, P. Bai, L. Bian, Q. J. Zhang, and P. Liu, "Investigation of degradation mechanism in 1200-v sic mosfets under surge current stress of body diode using electro-thermal-mechanical analysis," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2026.
- [66] X. Wang, W. Chen, R. Sun, C. Liu, Y. Xia, Y. Xin, X. Xu, F. Wang, X. Chen, Y. Chen *et al.*, "Degradation behavior and mechanism of gan hemts with p-type gate in the third quadrant under repetitive surge current stress," *IEEE Transactions on Electron Devices*, vol. 69, no. 10, pp. 5733–5741, 2022.
- [67] J. McPherson, "Brief history of jedec qualification standards for silicon technology and their applicability (?) to wbg semiconductors," in *2018 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2018, pp. 3B–1.
- [68] S. Devices—Part, "Semiconductor devices—part 2: Discrete devices—rectifier diodes," IEC-60747-2, Tech. Rep., 2016.
- [69] A. Abuelnaga, M. Narimani, and A. S. Bahman, "A review on igbt module failure modes and lifetime testing," *IEEE access*, vol. 9, pp. 9643–9663, 2021.
- [70] R. Wu, F. Blaabjerg, H. Wang, and M. Liserre, "Overview of catastrophic failures of freewheeling diodes in power electronic circuits," *Microelectronics Reliability*, vol. 53, no. 9-11, pp. 1788–1792, 2013.
- [71] J. Zhang, E. Deng, Z. Zhao, J. Li, and Y. Huang, "Simulation on fatigue failure of single igbt chip module of press-pack igbts," *Transactions of China electrotechnical society*, vol. 33, no. 18, pp. 4277–4285, 2018.

- [72] T. Poller, T. Basler, M. Hernes, S. D'Arco, and J. Lutz, "Mechanical analysis of press-pack igbts," *Microelectronics Reliability*, vol. 52, no. 9, pp. 2397–2402, 2012, sPECIAL ISSUE 23rd EUROPEAN SYMPOSIUM ON THE RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0026271412002764>
- [73] W.-S. Loh, M. Corfield, H. Lu, S. Hogg, T. Tilford, and C. M. Johnson, "Wire bond reliability for power electronic modules-effect of bonding temperature," in *2007 International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems. EuroSime 2007*. IEEE, 2007, pp. 1–6.
- [74] C. Delepaut, S. Siconolfi, O. Mourra, and F. Tonicello, "Mosfet gate open failure analysis in power electronics," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2013, pp. 189–196.
- [75] T. Li, Y. Wang, Y. Zhang, J. Fan, X. Li, L. Qi, and X. Cui, "Impacts of the pressure distribution on dynamic avalanche in single press-pack igbt chip," *IEEE Transactions on Power Electronics*, vol. 39, no. 7, pp. 8187–8201, 2024.
- [76] Y. Jian, S. Peng, Z. Chen, Z. He, L. He, and X. Lv, "Influence of different vibration directions on the solder layer fatigue in igbt modules," *Microelectronics Reliability*, vol. 162, p. 115526, 2024.
- [77] K. Xiao, Z. Wang, X. Yan, W. Li, Y. Liu, and P. Liu, "Temperature distribution and mechanical stress analysis of press-pack igbt single chip under different operations," in *Frontier Academic Forum of Electrical Engineering*. Springer, 2025, pp. 789–796.
- [78] H. Li, R. Yao, W. Lai, H. Ren, and J. Li, "Modeling and analysis on overall fatigue failure evolution of press-pack igbt device," *IEEE Transactions on Electron Devices*, vol. 66, no. 3, pp. 1435–1443, 2019.
- [79] H. Fu, Y. Li, Q. Li, C. Tu, B. Xiao, F. Xiao, P. Liu, B. Gao, and J. Lu, "Failure mechanism analysis of bond wire of high power igbt under different load current," in *2022 IEEE 5th International Electrical and Energy Conference (CIEEC)*. IEEE, 2022, pp. 798–803.
- [80] Y. Zhang, C. Zhan, L. Zhu, L. Dou, W. Wang, S. Ji, Y. Jin, and X. Liu, "Condition deterioration mechanisms of high voltage press-pack igbt under power cycling test," in *2022 IEEE international conference on high voltage engineering and applications (ICHVE)*. IEEE, 2022, pp. 1–4.
- [81] L. Tinschert, A. R. Årdal, T. Poller, M. Bohlländer, M. Hernes, and J. Lutz, "Possible failure modes in press-pack igbts," *Microelectronics Reliability*, vol. 55, no. 6, pp. 903–911, 2015. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0026271415000451>
- [82] R. Liu, H. Li, R. Yao, X. Wang, H. Tan, W. Lai, Y. Yu, Z. Zhu, and B. Zhou, "Research on long-term reliability of silver sintered press-pack igbt modules," *Power Electronic Devices and Components*, vol. 3, p. 100012, 2022. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S2772370422000098>

- [83] Y. Peng, Y. Shen, and H. Wang, "A converter-level on-state voltage measurement method for power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1220–1224, 2020.
- [84] Y. Peng, S. Zhao, and H. Wang, "A digital twin based estimation method for health indicators of dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2105–2118, 2020.
- [85] L. Dupont, Y. Avenas, and P.-O. Jeannin, "Comparison of junction temperature evaluations in a power igbt module using an ir camera and three thermosensitive electrical parameters," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1599–1608, 2013.
- [86] H. Luo, W. Li, F. Iannuzzo, X. He, and F. Blaabjerg, "Enabling junction temperature estimation via collector-side thermo-sensitive electrical parameters through emitter stray inductance in high-power igbt modules," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4724–4738, 2017.
- [87] Z. Wang, B. Tian, W. Qiao, and L. Qu, "Real-time aging monitoring for igbt modules using case temperature," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1168–1178, 2015.
- [88] U. Scheuermann and R. Schmidt, "Impact of solder fatigue on module lifetime in power cycling tests," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*. IEEE, 2011, pp. 1–10.
- [89] U.-M. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen, and B. Rannestad, "Reliability improvement of power converters by means of condition monitoring of igbt modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7990–7997, 2016.
- [90] V. Smet, F. Forest, J.-J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of vce monitoring as a real-time method to estimate aging of bond wire-igbt modules stressed by power cycling," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2760–2770, 2012.
- [91] H. Huang and P. A. Mawby, "A lifetime estimation technique for voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 4113–4119, 2012.
- [92] F. Gonzalez-Hernando, J. San-Sebastian, A. Garcia-Bediaga, M. Arias, F. Iannuzzo, and F. Blaabjerg, "Wear-out condition monitoring of igbt and mosfet power modules in inverter operation," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6184–6192, 2019.
- [93] S. Tufail, H. Riggs, M. Tariq, and A. I. Sarwat, "Advancements and challenges in machine learning: A comprehensive review of models, libraries, applications, and algorithms," *Electronics*, vol. 12, no. 8, p. 1789, 2023.
- [94] M. Shafique, M. Naseer, T. Theocharides, C. Kyrkou, O. Mutlu, L. Orosa, and J. Choi, "Robust machine learning systems: Challenges, current trends, perspectives, and the road ahead," *IEEE Design & Test*, vol. 37, no. 2, pp. 30–57, 2020.

- [95] I. H. Sarker, "Machine learning: Algorithms, real-world applications and research directions," *SN computer science*, vol. 2, no. 3, pp. 1–21, 2021.
- [96] S. Zhao, T. An, and F. Qin, "Research on machine learning-assisted numerical simulation methods for igbt module bonded interface fatigue damage," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 3, pp. 3259–3272, 2025.
- [97] A. Ismail, L. Saidi, M. Sayadi, and M. Benbouzid, "Power igbt remaining useful life estimation using neural networks based feature reduction," in *2020 6th IEEE International Energy Conference (ENERGYCon)*. IEEE, 2020, pp. 137–142.
- [98] M. Moniruzzaman, A. H. Okilly, S. Choi, J. Baek, T. I. Mannan, and Z. Islam, "A comprehensive study of machine learning algorithms for gpu based real-time monitoring and lifetime prediction of igbts," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2024, pp. 2678–2684.
- [99] X. Shen, X. Zhang, H. Shen, Z. Dongye, B. Gu, and L. Qi, "Identification of igbt bonding wire degradation based on feature extraction and state classification," *IEEE Transactions on Power Electronics*, vol. 40, no. 10, pp. 15 371–15 380, 2025.
- [100] X. Yang, Y. Zhang, X. Wu, and G. Liu, "Failure mode classification of igbt modules under power cycling tests based on data-driven machine learning framework," *IEEE Transactions on Power Electronics*, vol. 38, no. 12, pp. 16 130–16 141, 2023.
- [101] L. Li, J. Liu, M.-L. Tseng, and M. K. Lim, "Accuracy of igbt junction temperature prediction: An improved sailfish algorithm to optimize support vector machine," *IEEE Transactions on Power Electronics*, vol. 39, no. 6, pp. 6864–6876, 2024.
- [102] V. Y. Konda, J.-H. Jung, and M. Liserre, "Intelligent junction temperature estimation of an igbt using machine learning and  $v_{ce}$  measurement," in *2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. IEEE, 2024, pp. 1–6.
- [103] F. Al-Turjman and I. Baali, "Machine learning for wearable iot-based applications: A survey," *Transactions on Emerging Telecommunications Technologies*, vol. 33, no. 8, p. e3635, 2022.
- [104] N.-Y. Choi and S.-U. Zhang, "Digital design for high-performance igbt devices using machine learning and multi-physics simulation," in *PCIM Conference 2025; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2025, pp. 90–96.
- [105] M. Rapp, O. Elfatairy, M. Wolf, J. Henkel, and H. Amrouch, "Towards nn-based online estimation of the full-chip temperature and the rate of temperature change," in *Proceedings of the 2020 ACM/IEEE Workshop on Machine Learning for CAD*, 2020, pp. 95–100.
- [106] Y. Dai, J. Chen, Q. Yao, J. Yao, Z. Hu, Y. Xu, M. Zhang, J. Zhang, and Y. Guo, "Device-package-level electrothermal performance prediction of power mosfets using data generation-based artificial neural networks," *IEEE Transactions on Electron Devices*, vol. 73, no. 1, pp. 508–516, 2026.

- [107] O. Solomakha, V. Afanasenko, and I. Kallfass, "Online junction temperature estimation of power semiconductor devices using neural network and model-based design," in *IEEE EUROCON 2023-20th International Conference on Smart Technologies*. IEEE, 2023, pp. 187–192.
- [108] Z. Xu, H. Wang, X. Ge, Y. Zhang, D. Xie, B. Yao, L. Zhang, Y. Wang, and X. Feng, "Junction temperature monitoring of power devices using convolutional neural networks," *IEEE Transactions on Industry Applications*, 2025.
- [109] M. M. Zaben, M. Y. Worku, M. A. Hassan, and M. A. Abido, "Machine learning methods for fault diagnosis in ac microgrids: A systematic review," *IEEE access*, vol. 12, pp. 20 260–20 298, 2024.
- [110] K. Sarita, S. Kumar, and R. Saket, "Oc fault diagnosis of multilevel inverter using svm technique and detection algorithm," *Computers & Electrical Engineering*, vol. 96, p. 107481, 2021.
- [111] S. U. Jagade, M. S. Muthuvalu, A. C. Ribeiro, and M. Sambath, "Prediction of igt peak junction temperature using hybrid voting-based ensemble model," in *2025 IEEE Industrial Electronics and Applications Conference (IEACon)*. IEEE, 2025, pp. 176–181.
- [112] O. Yatskiv and B. Koman, "Assessing the potential of artificial intelligence and machine learning for thermal management in electronic devices," *Technology audit and production reserves*, vol. 1, no. 1/81, pp. 58–74, 2025.
- [113] R. Rodrigues, Y. Zhang, T. Jiang, E. Aeloiza, and P. Cairolì, "Surge current capability of sic mosfets in ac distribution systems," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 331–337.
- [114] S. Palanisamy, G. V. Yoganath, G. Zeng, J. Lutz, J. Kowalsky, and T. Basler, "Temperature determination of sic mps diodes during surge current event with measurement and simulation," in *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*. IEEE, 2019, pp. P–1.
- [115] D. Nehmer, T. Ringelmann, and M.-M. Bakran, "Modelling and evalaution of the bidirectional surge current robustness of si(-igt and -diode), sic(-mosfets and -jfet) and gan(-hemts) devices," *Energies*, vol. 17, no. 17, 2024. [Online]. Available: <https://www.mdpi.com/1996-1073/17/17/4362>
- [116] T. B. Soeiro, E. Mengotti, E. Bianda, and G. Ortiz, "Performance evaluation of the body-diode of sic mosfets under repetitive surge current operation," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 5154–5159.
- [117] J. Wu, N. Ren, and K. Sheng, "Electrothermal coupling model with distributed heat sources for junction temperature calculation during surges," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 11 887–11 895, 2022.
- [118] F. Zheng, X. Cui, X. Li, Z. Zhao, and L. Qi, "Temperature evaluation and failure analysis of wire-bonded frd chips in surge conditions," *IEEE Transactions on Power Electronics*, vol. 39, no. 12, pp. 16 103–16 115, 2024.



- [119] M. Shahjalal, T. Shams, S. B. Hossain, M. R. Ahmed, M. Ahsan, J. Haider, R. Goswami, S. B. Alam, and A. Iqbal, "Thermal analysis of si-igbt based power electronic modules in 50kw traction inverter application," *e-Prime-Advances in Electrical Engineering, Electronics and Energy*, vol. 3, p. 100112, 2023.
- [120] Y. Tang, C. Zhan, L. Zhu, W. Wang, Y. Gou, and S. Ji, "Efficient junction temperature estimation of sic power modules based on temperature-dependent lumped thermal model," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 3, pp. 2799–2810, 2024.
- [121] Y. Yang, Y. Wu, X. Ding, and P. Zhang, "A novel thermal management method for enhancing the consistency of igbt heat stress in converter," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 10, pp. 10 628–10 638, 2022.
- [122] H.-C. Cheng, J.-Y. Syu, H.-H. Wang, Y.-C. Liu, K.-S. Kao, and T.-C. Chang, "Power cycling modeling and lifetime evaluation of sic power mosfet module using a modified physical lifetime model," *IEEE Transactions on Device and Materials Reliability*, vol. 24, no. 1, pp. 142–153, 2024.
- [123] S. Rahimpour, H. Tarzamni, N. V. Kurdkandi, O. Husev, D. Vinnikov, and F. Tahami, "An overview of lifetime management of power electronic converters," *Ieee Access*, vol. 10, pp. 109 688–109 711, 2022.
- [124] P. Dini, S. Saponara, S. Chakraborty, F. Hosseinabadi, and O. Hegazy, "Experimental characterization and electro-thermal modeling of double side cooled sic mosfets for accurate and rapid power converter simulations," *IEEE Access*, vol. 11, pp. 79 120–79 143, 2023.
- [125] L. ZHOU, D. WANG, S. JONES-JACKSON, C. LIU, M. ABDALMAGID, and A. EMADI, "Overview of thermal modeling and monitoring for sic multi-chip power modules," *IEEE Open Journal of Power Electronics*, 2026.
- [126] Y. Shi, J. Liu, Y. Ai, S. Chen, and Y. Bai, "Dynamic igbt three-dimensional thermal network model considering base solder degradation and thermal coupling between igbt chips," *IEEE Transactions on Transportation Electrification*, vol. 9, no. 2, pp. 2994–3011, 2022.
- [127] J. Zhang, H. Shen, H. Sun, and Z. Wang, "Review on the thermal models applications in the reliability of power semiconductor device," *IET Power Electronics*, vol. 18, no. 1, p. e70065, 2025.
- [128] Y. Huo, J. Song, W. Li, J. Zhang, Y. Zhang, Y. Fu, W. Yuan, X. Chen, S. Liu, M. Jiang *et al.*, "Emerging advanced electronic packaging materials for thermal management in power electronics," *Advanced Science*, p. e24348, 2026.
- [129] M. Singh, J. F. Sargent Jr, and K. M. Sutter, "Semiconductors and the semiconductor industry." *Congressional Research Service (CRS) Reports and Issue Briefs*, pp. R47 508–R47 508, 2023.
- [130] Market.us, "Semiconductor materials market report," <https://market.us/report/semiconductor-materials-market/>, accessed: 2025-08-05.

- [131] S. Gujar and S. Ugale, “Semiconductor foundry market size, share, forecast 2025–2034,” <https://www.gminsights.com/industry-analysis/semiconductor-foundry-market>, Feb. 2025, published: February 2025.
- [132] SNS Insider pvt ltd, “Power semiconductor market size to hit usd 75.13 billion by 2032,” Press release on GlobeNewswire, Feb. 04 2025, austin, TX – February 04, 2025. [Online]. Available: <https://www.globenewswire.com/news-release/2025/02/04/3020410/0/en/Power-Semiconductor-Market-Size-to-Hit-USD-75-13-Billion-by-2032-SNS-Insider.html>
- [133] PW Consulting Information & Electronics Research Center, “Power semiconductor chips market,” Website, February 25 2025, “Power Semiconductor Chips Market” report. Accessed 2025-08-07, URL: <https://pmarketresearch.com/it/power-semiconductor-chips-market/>.
- [134] Mordor Intelligence, “Power semiconductor market– share, companies& industry size,” <https://www.mordorintelligence.com/industry-reports/semiconductor-industry-landscape>, 2025, accessed: 2025-08-05.
- [135] M. A. Rahman, “A review on semiconductors including applications and temperature effects in semiconductors,” *American Scientific Research Journal for Engineering, Technology, and Sciences (ASRJETS)*, vol. 7, no. 1, pp. 50–70, 2014.
- [136] M. D. McCluskey and E. E. Haller, *Dopants and defects in semiconductors*. CRC press, 2018.
- [137] Y. Rozanov, *Power electronics basics: operating principles, design, formulas, and applications*. CRC press, 2015.
- [138] A. I. Maswood, “The power diode,” in *Power Electronics Handbook*. Elsevier, 2011, pp. 17–27.
- [139] C. Qian, A. M. Gheitaghy, J. Fan, H. Tang, B. Sun, H. Ye, and G. Zhang, “Thermal management on igbt power electronic devices and modules,” *Ieee Access*, vol. 6, pp. 12 868–12 884, 2018.
- [140] T. Kimoto and H. Watanabe, “Defect engineering in sic technology for high-voltage power devices,” *Applied Physics Express*, vol. 13, no. 12, p. 120101, 2020.
- [141] P. L. Hower and V. K. Reddi, “Avalanche injection and second breakdown in transistors,” *IEEE Transactions on Electron Devices*, vol. 17, no. 4, pp. 320–335, 1970.
- [142] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, “Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review,” *IEEE Transactions on power electronics*, vol. 30, no. 5, pp. 2413–2426, 2014.
- [143] X. Ge, K. Chen, H. Wang, Z. Xu, and Z. Fu, “Failure mechanism investigations of bond wires lifting-off and die-attach solder aging considering the thermal coupling effects,” *IEEE Transactions on Power Electronics*, vol. 40, no. 1, pp. 2042–2056, 2025.

- [144] U.-M. Choi, F. Blaabjerg, and S. Jørgensen, "Study on effect of junction temperature swing duration on lifetime of transfer molded power igbt modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6434–6443, 2017.
- [145] J. Zhou, L. Zhong, X. Feng, W. Zhang, X. Liu, H. Zhou, Z. Liu, Y. Hao, and J. Zhang, "Recent advances in device-level thermal management technologies for wide bandgap semiconductor: A review," *IEEE Transactions on Electron Devices*, 2025.
- [146] Q. Zhang and P. Zhang, "A junction temperature and package aging decoupling evaluating method for sic mosfets based on the turn-on drain-source current overshoot," *IEEE Transactions on Power Electronics*, vol. 38, no. 11, pp. 14 537–14 546, 2023.
- [147] W. Miller, C. Smith, D. Mackenzie, and K. Evans, "Negative thermal expansion: a review," *Journal of materials science*, vol. 44, pp. 5441–5451, 2009.
- [148] J. Chen, L. Hu, J. Deng, and X. Xing, "Negative thermal expansion in functional materials: controllable thermal expansion by chemical modifications," *Chemical Society Reviews*, vol. 44, no. 11, pp. 3522–3567, 2015.
- [149] S. Chen, Y. Zhu, and G. Konstantinou, "Dependencies of temperature sensitive electrical parameters and influence of degradation in silicon carbide mosfets: A review," in *2024 IEEE 34th Australasian Universities Power Engineering Conference (AUPEC)*. IEEE, 2024, pp. 1–6.
- [150] Z. Zhang, L. Liang, L. Wang, Z. Zhang, K. Wen, and L. Tu, "Maximum chip temperature direct monitoring for press-pack igbt integrating temperature sensors," *IEEE Transactions on Power Electronics*, vol. 40, no. 6, pp. 8049–8061, 2025.
- [151] R. Anandanatarajan, U. Mangalanathan, and U. Gandhi, "Deep neural network-based linearization and cold junction compensation of thermocouple," *IEEE Transactions on Instrumentation and Measurement*, vol. 72, pp. 1–9, 2023.
- [152] L. Zhang, Z. Zheng, and X. Lou, "A review of wbg and si devices hybrid applications," *Chinese Journal of Electrical Engineering*, vol. 7, no. 2, pp. 1–20, 2021.
- [153] J. G. Jeon, H. J. Kim, G. Shin, Y. Han, J. H. Kim, J. H. Lee, J. Lee, H. Lim, S. Ha, M. Bae *et al.*, "High-precision ionic thermocouples fabricated using potassium ferri/ferrocyanide and iron perchlorate," *Advanced Electronic Materials*, vol. 8, no. 5, p. 2100693, 2022.
- [154] I. Fedosov and A. Shestakov, "Synthetic data generation for thermocouples. an original approach to simulation modelling of a measurement function," in *2023 XXXIII International Scientific Symposium Metrology and Metrology Assurance (MMA)*. IEEE, 2023, pp. 1–5.
- [155] K. Ding, R. Jiang, M. Tao, and R. Xie, "A simple single channel type k thermocouple temperature measurement design," in *2025 5th International Conference on Consumer Electronics and Computer Engineering (ICCECE)*, 2025, pp. 447–450.
- [156] M. P. R. Sofia, M. Jeyakumar, A. R. L. S. K., and P. RS, "Design of mems thermocouple with chromel and alumel (cr-al)," in *2024 International Conference on System, Computation, Automation and Networking (ICSCAN)*, 2024, pp. 1–5.

- [157] A. Noerpamoengkas, A. Y. Ismail, and M. F. Mahamudin, “Effect of surface imperfections on the thermocouple performance,” *Journal of Advanced Research in Applied Mechanics*, vol. 34, no. 1, pp. 10–14, 2017.
- [158] Y. Abdelaziz, M. Hammam, F. Megahed, and E. R. Qamar, “Characterizing drift behavior in type k and n thermocouples after high temperature thermal exposures,” *Journal of Advanced Research in Fluid Mechanics and Thermal Sciences*, vol. 97, no. 1, pp. 62–74, 2022.
- [159] M. Faraday, *On a new law of electric conduction; On conducting power generally*. Royal Society, 1833.
- [160] T. J. Bajzek, “Thermocouples: A sensor for measuring temperature,” *IEEE Instrumentation & Measurement Magazine*, vol. 8, no. 1, pp. 35–40, 2005.
- [161] L. Yang, Y. Zhao, C. Feng, and H. Zhou, “The influence of size effect on sensitivity of cu/cuni thin-film thermocouple,” *Physics Procedia*, vol. 22, pp. 95–100, 2011.
- [162] X. Perpiñà, J.-F. Serviere, J. Saiz, D. Barlini, M. Mermet-Guyennet, and J. Millan, “Temperature measurement on series resistance and devices in power packs based on on-state voltage drop monitoring at high current,” *Microelectronics Reliability*, vol. 46, no. 9-11, pp. 1834–1839, 2006.
- [163] D. L. Blackburn, “Temperature measurements of semiconductor devices-a review,” in *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (IEEE Cat. No. 04CH37545)*. IEEE, 2004, pp. 70–80.
- [164] G. Romano, M. Riccio, G. De Falco, L. Maresca, A. Irace, and G. Breglio, “An ultrafast ir thermography system for transient temperature detection on electronic devices,” in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*. IEEE, 2014, pp. 80–84.
- [165] W. Zhou, X. Zhong, and K. Sheng, “High temperature stability and the performance degradation of sic mosfets,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2329–2337, 2013.
- [166] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, “Ir camera validation of igbt junction temperature measurement via peak gate current,” *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3099–3111, 2016.
- [167] W. Zhou, X. Zhong, and K. Sheng, “High temperature stability evaluation of sic mosfets,” in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*. IEEE, 2014, pp. 305–308.
- [168] R. Isa, J. Mirza, S. Ghafoor, M. Z. Mustafa Khan, and K. K. Qureshi, “Junction temperature optical sensing techniques for power switching semiconductors: A review,” *Micromachines*, vol. 14, no. 8, p. 1636, 2023.
- [169] X. Xiao, X. Ge, Q. Ke, L. Yong, Y. Liao, H. Wang, and Y. Zhang, “An adaptive temperature observer for electrothermal analysis of igbt based on temperature characteristics,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 2, pp. 2246–2258, 2022.

- [170] M. Ventimiglia, A. Scuto, G. Sorrentino, G. Belverde, F. Iannuzzo, and S. A. Rizzo, "On-state voltage measurement circuit for condition monitoring of mosfets in resonant converters," *Electronics*, vol. 13, no. 19, p. 3902, 2024.
- [171] H. Tan, W. Song, J. Chen, P. Xu, K. Yang, and T. Tang, "An online junction temperature estimation method of igbts based on the improved on-state voltage measuring circuit," *IEEE Transactions on Instrumentation and Measurement*, vol. 73, pp. 1–11, 2024.
- [172] A. Griffo, J. Wang, K. Colombage, and T. Kamel, "Real-time measurement of temperature sensitive electrical parameters in sic power mosfets," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2663–2671, 2017.
- [173] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Industrial Electronics Magazine*, vol. 8, no. 3, pp. 17–27, 2014.
- [174] F. Stella, G. Pellegrino, E. Armando, and D. Daprà, "On-line temperature estimation of sic power mosfet modules through on-state resistance mapping," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2017, pp. 5907–5914.
- [175] F. Stella, G. Pellegrino, E. Armando, and D. Dapra, "Online junction temperature estimation of sic power mosfets through on-state voltage mapping," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3453–3462, 2018.
- [176] Y. Yang, Q. Zhang, and P. Zhang, "A fast igbt junction temperature estimation approach based on on-state voltage drop," *IEEE Transactions on Industry Applications*, vol. 57, no. 1, pp. 685–693, 2020.
- [177] A. Arya, P. Kumar, and S. Anand, "Methodology of an accurate static i–v characterization of power semiconductor devices," *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 10, pp. 7703–7715, 2020.
- [178] P. Wang and Z. Zhao, "A gate oxide degradation and junction temperature evaluation method for sic mosfets based on an on-state resistance model," *Electronics*, vol. 14, no. 11, p. 2278, 2025.
- [179] G. Lee and S. Chae, "Online estimation method for on-state resistance imbalance among mosfets in the dab converter," in *2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE)*. IEEE, 2025, pp. 1–5.
- [180] E. Panciroli, A. Musetti, and A. Soldati, "Revisiting on-state resistance as tsep for discrete sic mosfets: steps towards the in-circuit approach," *IEEE Open Journal of Power Electronics*, 2025.
- [181] J. Shin, J.-W. Shin, and W. Kim, "Noise-robust online measurement of the on-state resistance of the power semiconductor devices in pwm converters," *IEEE Access*, vol. 12, pp. 63 669–63 682, 2024.
- [182] M. Asoodar, M. Nahalparvari, H.-P. Nee, and I. Shafikhani, "A time-skew resilient online condition monitoring technique for power mosfets based on on-state resistance estimation," in *2024 IEEE 9th Southern Power Electronics Conference (SPEC)*. IEEE, 2024, pp. 1–6.

- [183] J. Shin and J.-W. Shin, "Testbed of power mosfet aging including the measurement of on-state resistance," *The Transactions of the Korean Institute of Power Electronics*, vol. 27, no. 3, pp. 206–213, 2022.
- [184] J. Yang, Y. Che, L. Ran, M. Du, H. Jiang, and M. Xiao, "Monitoring initial solder layer degradation in a multichip igbt module via combined tseps," *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 1, pp. 26–35, 2021.
- [185] Y. Peng, L. Zhou, P. Sun, C. Gong, and X. Du, "Study of igbt junction temperature estimation based on turn-on miller platform voltage," *Proceedings of the CSEE*, vol. 37, no. 11, pp. 3254–3262, 2017.
- [186] H. Luo, F. Iannuzzo, and M. Turnaturi, "Role of threshold voltage shift in highly accelerated power cycling tests for sic mosfet modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1657–1667, 2019.
- [187] M. A. Eleffendi and C. M. Johnson, "Evaluation of on-state voltage  $v_{ce(on)}$  and threshold voltage  $v_{th}$  for real-time health monitoring of igbt power modules," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*. IEEE, 2015, pp. 1–10.
- [188] X. Jiang, J. Wang, H. Yu, J. Chen, Z. Zeng, X. Yang, and Z. J. Shen, "Online junction temperature measurement for sic mosfet based on dynamic threshold voltage extraction," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3757–3768, 2020.
- [189] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on sic mosfets high-voltage device reliability focusing on threshold voltage instability," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4604–4616, 2019.
- [190] T. Tang, W. Song, K. Yang, and J. Chen, "A junction temperature online monitoring method for igbts based on turn-off delay time," *IEEE Transactions on Industry Applications*, vol. 59, no. 5, pp. 6399–6411, 2023.
- [191] Z. Zhang, J. Dyer, X. Wu, F. Wang, D. Costinett, L. M. Tolbert, and B. J. Blalock, "Online junction temperature monitoring using intelligent gate drive for sic power devices," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7922–7932, 2018.
- [192] F. Yang, S. Pu, C. Xu, and B. Akin, "Turn-on delay based real-time junction temperature measurement for sic mosfets with aging compensation," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1280–1294, 2020.
- [193] Z. Lu and F. Iannuzzo, "Online junction temperature extraction for cascode gan devices based on turn-on delay," *IEEE Transactions on Power Electronics*, vol. 39, no. 8, pp. 10 250–10 260, 2024.
- [194] X. Lu and L. Wang, "A novel method for real-time junction temperature monitoring of sic mosfet through sensitivity amplification of turn-off delay time," *IEEE Transactions on Power Electronics*, 2025.

- [195] M. Gleissner, D. Nehmer, and M.-M. Bakran, "Junction temperature measurement based on the internal gate resistance for a wide range of power semiconductors," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 293–305, 2023.
- [196] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "Igbt junction temperature measurement via peak gate current," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3784–3793, 2015.
- [197] Q. Zhang and P. Zhang, "An online junction temperature monitoring method for sic mosfets based on a novel gate conduction model," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 087–11 096, 2021.
- [198] M. Iachello, V. De Luca, G. Petrone, N. Testa, L. Fortuna, G. Cammarata, S. Graziani, and M. Frasca, "Lumped parameter modeling for thermal characterization of high-power modules," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 10, pp. 1613–1623, 2014.
- [199] M. Musallam and C. M. Johnson, "Real-time compact thermal models for health management of power electronics," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1416–1425, 2010.
- [200] A. S. Bahman, K. Ma, and F. Blaabjerg, "A novel 3d thermal impedance model for high power modules considering multi-layer thermal coupling and different heating/cooling conditions," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2015, pp. 1209–1215.
- [201] Y. Yu, T.-Y. T. Lee, and V. A. Chiriac, "Compact thermal resistor-capacitor-network approach to predicting transient junction temperatures of a power amplifier module," *IEEE Transactions on components, packaging and manufacturing technology*, vol. 2, no. 7, pp. 1172–1181, 2012.
- [202] Y. C. Gerstenmaier, W. Kiffe, and G. Wachutka, "Combination of thermal subsystems modeled by rapid circuit transformation," in *2007 13th International Workshop on Thermal Investigation of ICs and Systems (THERMINIC)*. IEEE, 2007, pp. 115–120.
- [203] Y. Yang, R. Master, G. Refai-Ahmed, and M. Touzelbaev, "Transient frequency-domain thermal measurements with applications to electronic packaging," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 3, pp. 448–456, 2012.
- [204] T. K. Gachovska, B. Tian, J. L. Hudgins, W. Qiao, and J. F. Donlon, "A real-time thermal model for monitoring of power semiconductor devices," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3361–3367, 2015.
- [205] C. Batard, N. Ginot, and J. Antonios, "Lumped dynamic electrothermal model of igbt module of inverters," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 3, pp. 355–364, 2015.
- [206] M. Chen, A. Hu, and X. Yang, "Predicting igbt junction temperature with thermal network component model," in *2011 Asia-Pacific Power and Energy Engineering Conference*. IEEE, 2011, pp. 1–4.

- [207] Y. Tang and H. Ma, "Dynamic electrothermal model of paralleled igbt modules with unbalanced stray parameters," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1385–1399, 2016.
- [208] W. Guo, M. Ma, H. Wang, N. Xiang, H. Wang, Z. Chen, and W. Chen, "Real-time average junction temperature estimation for multichip igbt modules with low computational cost," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 4, pp. 4175–4185, 2022.
- [209] Z. Wang and W. Qiao, "A physics-based improved cauer-type thermal equivalent circuit for igbt modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 6781–6786, 2016.
- [210] Q. Li, S. Cheng, Y. Chen, J. Ye, X. Cui, and P. Li, "Study on cauer thermal network model considering bidirectional heat transfer," *IEEE Access*, vol. 12, pp. 90 525–90 534, 2024.
- [211] M. Chen, H. Wang, D. Pan, X. Wang, and F. Blaabjerg, "Thermal characterization of silicon carbide mosfet module suitable for high-temperature computationally efficient thermal-profile prediction," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 3947–3958, 2020.
- [212] C. Zhan, L. Zhu, W. Wang, Q. Jiao, Y. Zhang, and S. Ji, "A large-scale identification approach for thermal parameters of multichips igbt modules based on llso-sqp algorithm," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2554–2564, 2022.
- [213] Y. Kishor and R. Patel, "Thermal modelling and reliability analysis of recently introduced high gain converters for pv application," *Cleaner Energy Systems*, vol. 3, p. 100016, 2022.
- [214] K. Heng, X. Yang, X. Wu, and J. Ye, "A 3-d thermal network model for monitoring of igbt modules," *IEEE Transactions on Electron Devices*, vol. 70, no. 2, pp. 653–661, 2022.
- [215] H. Wang, Z. Zhou, Z. Xu, X. Ge, Y. Yang, Y. Zhang, B. Yao, and D. Xie, "A thermal network model for multichip power modules enabling to characterize the thermal coupling effects," *IEEE Transactions on Power Electronics*, vol. 39, no. 5, pp. 6225–6245, 2024.
- [216] K. Heng, X. Yang, X. Wu, and J. Ye, "A 3-d thermal network model for monitoring of igbt modules," *IEEE Transactions on Electron Devices*, vol. 70, no. 2, pp. 653–661, 2023.
- [217] X. Yang, S. Xu, K. Heng, and X. Wu, "Distributed thermal modeling for power devices and modules with equivalent heat flow path extraction," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 6, pp. 5863–5876, 2023.
- [218] Y. Lu, E. Xiang, Y. Jin, H. Luo, H. Yang, W. Li, and R. Zhao, "A 3-d temperature-dependent thermal model of igbt modules for electric vehicle application considering various boundary conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 6, pp. 5463–5475, 2024.



- [219] K. Heng, X. Yang, X. Wu, J. Ye, and G. Liu, "A temperature-dependent physical thermal network model including thermal boundary conditions for sic mosfet module," *IEEE Transactions on Electron Devices*, vol. 69, no. 8, pp. 4444–4452, 2022.
- [220] Y. Tian, B. Liu, K. Bu, C. Li, S. Ye, W. Li, H. Luo, and X. He, "A robust power loss observer for thermal model method-based igbt junction temperature monitoring," *Protection and Control of Modern Power Systems*, vol. 10, no. 2, pp. 102–119, 2025.
- [221] X. Yang, S. Xu, K. Heng, and X. Wu, "Distributed thermal modeling for power devices and modules with equivalent heat flow path extraction," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 6, pp. 5863–5876, 2023.
- [222] H. Wang, Z. Zhou, Z. Xu, X. Ge, Y. Yang, Y. Zhang, B. Yao, and D. Xie, "A thermal network model for multichip power modules enabling to characterize the thermal coupling effects," *IEEE Transactions on Power Electronics*, vol. 39, no. 5, pp. 6225–6245, 2024.
- [223] M. Giesselmann, K. Rodriguez, and J. Mayes, "Thermal models for power igbts in pulsed power applications," in *2024 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*. IEEE, 2024, pp. 1–4.
- [224] R. Wu, H. Wang, K. B. Pedersen, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A temperature-dependent thermal model of igbt modules suitable for circuit-level simulations," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3306–3314, 2016.
- [225] L. Ceccarelli, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "A fast electro-thermal co-simulation modeling approach for sic power mosfets," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2017, pp. 966–973.
- [226] M. Xu, K. Ma, B. Liu, and X. Cai, "Modeling and correlation of two thermal paths in frequency-domain thermal impedance model of power module," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 3971–3981, 2020.
- [227] K. Ma, M. Xu, and B. Liu, "Modeling and characterization of frequency-domain thermal impedance for igbt module through heat flow information," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1330–1340, 2020.
- [228] H. Wang, R. Zhu, H. Wang, M. Liserre, and F. Blaabjerg, "A thermal modeling method considering ambient temperature dynamics," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 6–9, 2019.
- [229] A. S. Bahman, F. Blaabjerg, A. Dutta, and A. Mantooth, "Electrical parasitics and thermal modeling for optimized layout design of high power sic modules," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2016, pp. 3012–3019.
- [230] A. S. Bahman, K. Ma, and F. Blaabjerg, "A lumped thermal model including thermal coupling and thermal boundary conditions for high-power igbt modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2518–2530, 2018.

- [231] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7183–7193, 2015.
- [232] M. Shahjalal, M. R. Ahmed, H. Lu, C. Bailey, and A. J. Forsyth, "An analysis of the thermal interaction between components in power converter applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9082–9094, 2020.
- [233] M. Xu, K. Ma, X. Cai, G. Cao, and Y. Zhang, "Lumped thermal coupling model of multichip power module enabling case temperature as reference node," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 11 502–11 506, 2022.
- [234] L. Ceccarelli, R. M. Kotecha, A. S. Bahman, F. Iannuzzo, and H. A. Mantooth, "Mission-profile-based lifetime prediction for a sic mosfet power module using a multi-step condition-mapping simulation strategy," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9698–9708, 2019.
- [235] F. Iannuzzo and G. Busatto, "Physical cad model for high-voltage igbts based on lumped-charge approach," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 885–893, 2004.
- [236] A. R. HEFNER JR, *Characterization and modeling of the power insulated gate bipolar transistor*. University of Maryland, College Park, 1987.
- [237] B. Du, J. L. Hudgins, E. Santi, A. T. Bryant, P. R. Palmer, and H. A. Mantooth, "Transient electrothermal simulation of power semiconductor devices," *IEEE Transactions on power electronics*, vol. 25, no. 1, pp. 237–248, 2009.
- [238] F. Ahmad, F. Portesine, M. Ashero, M. Marchesoni, and L. Vaccaro, "Transient thermal impedance characterization of new high power press pack diodes," in *2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2024, pp. 81–86.
- [239] M. A. Besserour, S. Eloued, J. B. H. Slama, F. Fouquet, and M. Kadi, "Thermal modelling for an electrothermal model of gan devices," in *2021 12th International Renewable Energy Congress (IREC)*. IEEE, 2021, pp. 1–6.
- [240] Y. Shen, X. Fan, and D. Tang, "Electrothermal simulation analysis on power loss and junction temperature of gan hemt in boost dc-dc converter," in *2022 7th International Conference on Power and Renewable Energy (ICPRE)*. IEEE, 2022, pp. 138–143.
- [241] A. Empeyrou, M. Ouhab, and N. Degrenne, "3d fine electrothermal modeling of igbt power device for reliability applications," in *2025 26th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*. IEEE, 2025, pp. 1–9.
- [242] J. Wang, W. Chen, Y. Wu, J. Zhang, L. Wang, and J. Liu, "Chip-level electrothermal stress calculation method of high-power igbt modules in system-level simulation," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 546–10 561, 2022.

- [243] M. Baghdadi, E. Elwarraki, I. Ait Ayad, and N. Mijlad, "Behavioral electrothermal modeling of mosfet for energy conversion circuits simulation using matlab/simulink," *Microelectronics Reliability*, vol. 154, p. 115340, 2024.
- [244] R. Al Mdanat, R. Georgious, S. Saeed, and J. Garcia, "Power loss modeling and impact of current measurement on the switching characterization in enhancement-mode gan transistors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2024.
- [245] X. Long, Z. Jun, B. Zhang, D. Chen, and W. Liang, "A unified electrothermal behavior modeling method for both sic mosfet and gan hemt," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9366–9375, 2020.
- [246] J. G. Berger, C. A. Rojas, A. H. Wilson-Veas, R. A. Bugueno, A. Peralta, J. Mar, H. Young, L. Callegaro *et al.*, "On the experimental verification of electrothermal modeling of gan-hemt-based dc-dc converters," *IEEE Transactions on Power Electronics*, 2024.
- [247] P. Górecki, "Electrothermal averaged model of a diode–igbt switch for a fast analysis of dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 11, pp. 13 003–13 013, 2022.
- [248] E. Deng, Z. Zhao, Z. Lin, R. Han, and Y. Huang, "Influence of temperature on the pressure distribution within press pack igbts," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6048–6059, 2017.
- [249] M. Guo, Y. Sha, L. Wei, and X. Jiang, "Electrothermal simulation of igbt module based on simulink," in *International Conference on Electrical and Information Technologies for Rail Transportation*. Springer, 2021, pp. 52–60.
- [250] W. Kwon, C. Yoo, and J. Jeon, "Electrothermal modeling of multi-nanosheet fets with various layouts," *IEEE Transactions on Electron Devices*, vol. 71, no. 4, pp. 2592–2597, 2024.
- [251] K. Górecki and P. Górecki, "Spice-aided nonlinear electrothermal modeling of an igbt module," *Electronics*, vol. 12, no. 22, p. 4588, 2023.
- [252] W. Hanini and M. Ayadi, "Electrothermal modeling of the insulated gate bipolar transistor (igbt) using pspice: application to dc–dc converter," *Journal of Control, Automation and Electrical Systems*, vol. 32, no. 2, pp. 507–521, 2021.
- [253] Y. Lu, E. Xiang, A. Zhu, H. Gao, H. Luo, H. Yang, and R. Zhao, "Physics-based electrothermal stress evaluation approach of igbt modules combined with artificial neural network model," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 740–751, 2023.
- [254] X. Lan and N. Zhao, "Development of a steady state electrothermal cosimulation model of sic power modules," *International Journal of Heat and Mass Transfer*, vol. 226, p. 125460, 2024.

- [255] Y. Jia, F. Xiao, Y. Duan, Y. Luo, B. Liu, and Y. Huang, "Pspice-comsol-based 3-d electrothermal-mechanical modeling of igbt power module," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 4173–4185, 2020.
- [256] Y. Tian, T. An, F. Qin, Y. Gong, and C. Liang, "A thermal network model for thermal analysis in automotive igbt modules," in *2021 22nd International Conference on Electronic Packaging Technology (ICEPT)*. IEEE, 2021, pp. 1–5.
- [257] S. Race, T. Ziemann, S. Tiwari, I. Kovacevic-Badstuebner, and U. Grossner, "Accuracy of thermal analysis for sic power devices," in *2021 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2021, pp. 1–5.
- [258] Q. Wang, J. Zhang, F. Iannuzzo, A. S. Bahman, W. Zhang, and F. He, "Improved temperature monitoring and protection method of three-level npc application based on half-bridge igbt modules," *IEEE Access*, vol. 10, pp. 35 605–35 619, 2022.
- [259] Y. Shi, J. Liu, Y. Ai, S. Chen, and Y. Bai, "Dynamic igbt three-dimensional thermal network model considering base solder degradation and thermal coupling between igbt chips," *IEEE Transactions on Transportation Electrification*, vol. 9, no. 2, pp. 2994–3011, 2023.
- [260] N. Dornic, Z. Khatir, S. H. Tran, A. Ibrahim, R. Lallemand, J.-P. Ousten, J. Ewanchuk, and S. V. Mollov, "Stress-based model for lifetime estimation of bond wire contacts using power cycling tests and finite-element modeling," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1659–1667, 2019.
- [261] B. Wang, L. Wang, F. Yang, W. Mu, M. Qin, F. Zhang, D. Ma, J. Wang, and J. Liu, "Air-cooling system optimization for igbt modules in mmc using embedded o-shaped heat pipes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 3992–4003, 2021.
- [262] T. Wu, Z. Wang, B. Ozpineci, M. Chinthavali, and S. Campbell, "Automated heatsink optimization for air-cooled power semiconductor modules," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5027–5031, 2019.
- [263] J. Li, A. Castellazzi, M. A. Eleffendi, E. Gurpinar, C. M. Johnson, and L. Mills, "A physical rc network model for electrothermal analysis of a multichip sic power module," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2494–2508, 2017.
- [264] Y. Chen, Q. Wu, C. Li, H. Luo, Y. Xia, Q. Yin, W. Li, and X. He, "Thermal mitigation and optimization via multitier bond wire layout for igbt modules considering multicellular electro-thermal effect," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 7299–7314, 2022.
- [265] H. Cui, M. Zhou, C. Yang, J. Li, and C. Wang, "Influence mechanism of solder aging and thermal network model optimization of multi-chip igbt modules," *Microelectronics Reliability*, vol. 139, p. 114827, 2022.

- [266] J. Cai, L. Zhou, P. Sun, T. Zhou, and Q. Li, "Effect of tim deterioration on monitoring of igbt module thermal resistance and its compensation strategy," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 12, no. 5, pp. 789–797, 2022.
- [267] Q. Li, F. Zhang, L. Guan, X. Zhang, X. Hu, Y. Chen, J. Zhai, P. Zeng, B. Yang, S. Cheng *et al.*, "An improved thermal coupling network model considering thermal interface material aging of igbt modules," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2025.
- [268] A. S. Bahman, K. Ma, and F. Blaabjerg, "A lumped thermal model including thermal coupling and thermal boundary conditions for high-power igbt modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2518–2530, 2017.
- [269] Y.-L. Chen, S. Sacchi, B. Dey, V. Blanco, S. Halder, P. Leray, and S. D. Gendt, "Exploring machine learning for semiconductor process optimization: A systematic review," *IEEE Transactions on Artificial Intelligence*, vol. 5, no. 12, pp. 5969–5989, 2024.
- [270] R. Ghoshhajra, K. Biswas, and A. Sarkar, "A review on machine learning approaches for predicting the effect of device parameters on performance of nanoscale mosfets," in *2021 Devices for Integrated Circuit (DevIC)*, 2021, pp. 489–493.
- [271] Z. Wang, L. Li, R. C. C. Leon, J. Yang, J. Shi, T. van der Laan, and M. Usman, "Improving semiconductor device modeling for electronic design automation by machine learning techniques," *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 263–271, 2024.
- [272] S. Zhao, T. An, and F. Qin, "Research on machine learning-assisted numerical simulation methods for igbt module bonded interface fatigue damage," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2025.
- [273] T. Thekemuriyil, J. D. Rohner, and R. A. Minamisawa, "Machine learning-based prediction of on-state voltage for real-time health monitoring of igbt," *Power Electronic Devices and Components*, vol. 6, p. 100049, 2023. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S2772370423000172>
- [274] X. Yang, Y. Zhang, X. Wu, and G. Liu, "Failure mode classification of igbt modules under power cycling tests based on data-driven machine learning framework," *IEEE Transactions on Power Electronics*, vol. 38, no. 12, pp. 16 130–16 141, 2023.
- [275] Q. Yao, J. Chen, Y. Dai, J. Yao, J. Zhang, M. Zhang, J. Liu, W. Tang, J. Zhang, B. Zhang, and Y. Guo, "A novel prediction technology of output characteristics for igbt based on compact model and artificial neural networks," *IEEE Transactions on Electron Devices*, vol. 70, no. 9, pp. 4885–4891, 2023.
- [276] L. Liu, G. Zhang, C. Zhao, C. Lin, J. Liu, and Y. Zhang, "Study on fault diagnosis of power electronic devices in power conversion system based on machine learning," in *Proceedings of the 1st Electrical Artificial Intelligence Conference, Volume 2*, R. Qu, Z. Song, Z. Ding, G. Mu, R. Xiong, and L. Han, Eds. Singapore: Springer Nature Singapore, 2025, pp. 52–61.

- [277] T. Thekemuriyil, J. D. Rohner, and R. A. Minamisawa, "Machine learning-based prediction of on-state voltage for real-time health monitoring of igbt," *Power Electronic Devices and Components*, vol. 6, p. 100049, 2023.
- [278] R. Prathiba, M. Saravanan, P. W. David, and H. Thangaraj, "Machine learning-based direct estimation of remaining useful life (rul) of igbt using multi-precursor prognostics," *Electrical Engineering*, vol. 107, no. 3, pp. 3435–3449, 2025.
- [279] V. Y. Konda, J.-H. Jung, and M. Liserre, "Intelligent junction temperature estimation of an igbt using machine learning and  $v_{ce}$  measurement," in *2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2024, pp. 1–6.
- [280] S. Farnesi, M. Marchesoni, and L. Vaccaro, "Reliability improvement of modular multilevel converter in hvdc systems," in *2016 Power Systems Computation Conference (PSCC)*. IEEE, 2016, pp. 1–7.
- [281] S. Rivera, J. Rojas, S. Kouro, P. W. Lehn, R. Lizana, H. Renaudineau, and T. Dragičević, "Partial-power converter topology of type ii for efficient electric vehicle fast charging," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7839–7848, 2022.
- [282] M. R. Khalid, M. S. Alam, M. Krishnamurthy, E. A. Al-Ammar, H. Alrajhi, and M. S. J. Asghar, "A multiphase ac–dc converter with improved power quality for ev charging station," *IEEE Transactions on Transportation Electrification*, vol. 8, no. 1, pp. 909–924, 2022.
- [283] G. Krishnan and A. Jain, "Heat transfer in a multi-layered semiconductor device with spatially-varying thermal contact resistance between layers," *International Communications in Heat and Mass Transfer*, vol. 140, p. 106482, 2023.
- [284] E. Deng, Z. Zhao, P. Zhang, X. Luo, J. Li, and Y. Huang, "Study on the method to measure thermal contact resistance within press pack igbts," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1509–1517, 2018.
- [285] J. Ortiz Gonzalez, O. Alatise, A. M. Aliyu, P. Rajaguru, A. Castellazzi, L. Ran, P. A. Mawby, and C. Bailey, "Evaluation of sic schottky diodes using pressure contacts," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8213–8223, 2017.
- [286] A. Hasmasan, C. Busca, R. Teodorescu, L. Helle, and F. Blaabjerg, "Electro-thermo-mechanical analysis of high-power press-pack insulated gate bipolar transistors under various mechanical clamping conditions," *IEEJ Journal of Industry Applications*, vol. 3, no. 3, pp. 192 – 197, 2014.
- [287] P. Siddappa and A. Tariq, "Contact area and thermal conductance estimation based on the actual surface roughness measurement," *Tribology International*, vol. 148, p. 106358, 2020.
- [288] M. Lambert and L. Fletcher, "Thermal contact conductance of spherical rough metals," 1997.

- [289] Y. Li, C. Madhusudana, and E. Leonardi, "On the enhancement of the thermal contact conductance: effect of loading history," *J. Heat transfer*, vol. 122, no. 1, pp. 46–49, 2000.
- [290] Y. Mei, T. Wang, X. Cao, G. Chen, G.-Q. Lu, and X. Chen, "Transient thermal impedance measurements on low-temperature-sintered nanoscale silver joints," *Journal of electronic materials*, vol. 41, pp. 3152–3160, 2012.
- [291] S. Bhadoria, F. Dijkhuizen, R. Raj, X. Wang, Q. Xu, E. Matioli, K. Kostov, and H.-P. Nee, "Enablers for overcurrent capability of silicon-carbide-based power converters: An overview," *IEEE transactions on power electronics*, vol. 38, no. 3, pp. 3569–3589, 2022.
- [292] X. Wu and W. Liu, "An engineering roadmap for the thermoelectric interface materials," *Journal of Materiomics*, vol. 10, no. 3, pp. 748–750, 2024. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S2352847823002265>
- [293] F. Asadi and K. Eguchi, *Power electronics circuit analysis with PSIM®*. Walter de Gruyter GmbH & Co KG, 2021.
- [294] L. Carbone, M. Marchesoni, M. Passalacqua, L. Vaccaro, and A. Formentini, "H2-lmi-based high performance control for matrix converter," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 9, pp. 10 029–10 038, 2024.
- [295] A. Benevieri, M. Marchesoni, M. Passalacqua, P. Pozzobon, and L. Vaccaro, "Synchronous dtc for torque sub-harmonic reduction in low switching frequency induction motor drives," *Control Engineering Practice*, vol. 154, p. 106133, 2025. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0967066124002922>
- [296] G. Wang, H. Wen, W. Liu, and F. Li, "Physical structure, characteristics, and applications of monolithic bidirectional switches: A comprehensive review," *IEEE Transactions on Power Electronics*, 2025.
- [297] Z. Wang, P. Wang, K. Liu, P. Wang, Y. Fu, C.-T. Lu, C. C. Aggarwal, J. Pei, and Y. Zhou, "A comprehensive survey on data augmentation," *IEEE Transactions on Knowledge and Data Engineering*, pp. 1–20, 2025.
- [298] J. Jung, D. P. Apsari, and D.-C. Lee, "Robust open-switch fault diagnosis of three-level npc inverters based on data augmentation with white noise injection," *IEEE Transactions on Power Electronics*, vol. 40, no. 2, pp. 3553–3565, 2025.
- [299] J. Ge, Z. Yao, M. Wu, J. H. S. Almeida Jr, Y. Jin, and D. Sun, "Tackling data scarcity in machine learning-based cfrp drilling performance prediction through a broad learning system with virtual sample generation (bls-vsg)," *Composites Part B: Engineering*, p. 112701, 2025.
- [300] K. Kavitha, R. A. Kumar *et al.*, "A maximum relevance minimum redundancy and random forest based feature selection and classification of gene expression data," in *2024 5th International Conference for Emerging Technology (INCET)*. IEEE, 2024, pp. 1–5.

- [301] Y. Wang, X. Li, and R. Ruiz, "Feature selection with maximal relevance and minimal supervised redundancy," *IEEE Transactions on Cybernetics*, vol. 53, no. 2, pp. 707–717, 2023.
- [302] F. E. Bezerra, G. C. d. Oliveira Neto, G. M. Cervi, R. Francesconi Mazetto, A. M. d. Faria, M. Vido, G. A. Lima, S. A. d. Araújo, M. Sampaio, and M. Amorim, "Impacts of feature selection on predicting machine failures by machine learning algorithms," *Applied Sciences*, vol. 14, no. 8, p. 3337, 2024.
- [303] M. Wu, Z. Yao, M. Verbeke, P. Karsmakers, B. Gorissen, and D. Reynaerts, "Data-driven models with physical interpretability for real-time cavity profile prediction in electrochemical machining processes," *Engineering Applications of Artificial Intelligence*, vol. 160, p. 111807, 2025.
- [304] S. Choi and J. Hur, "An ensemble learner-based bagging model using past output data for photovoltaic forecasting," *Energies*, vol. 13, no. 6, p. 1438, 2020.
- [305] J. Araneda, L. Morán, L. Vaccaro *et al.*, "Reactive power compensation system for the chilean hvdc transmission line," in *2025 AEIT HVDC International Conference (AEIT HVDC)*. IEEE, 2025, pp. 1–6.
- [306] Y. Chen, K. Shi, M. Chen, and D. Xu, "Data center power supply systems: From grid edge to point-of-load," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2441–2456, 2022.
- [307] A. Benevieri, S. Cosso, A. Formentini, M. Marchesoni, M. Passalacqua, and L. Vaccaro, "Advances and perspectives in multilevel converters: A comprehensive review," *Electronics*, vol. 13, no. 23, 2024. [Online]. Available: <https://www.mdpi.com/2079-9292/13/23/4736>
- [308] X. Jiang, J. Wang, H. Yu, J. Chen, Z. Zeng, X. Yang, and Z. J. Shen, "Online junction temperature measurement for sic mosfet based on dynamic threshold voltage extraction," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3757–3768, 2021.
- [309] B. A. M. Alizadeh, M. Khederzadeh, and R. Razzaghi, "Fault detection during power swing in thyristor-controlled series capacitor-compensated transmission lines," *Electric Power Systems Research*, vol. 187, p. 106481, 2020. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0378779620302844>
- [310] M. Joo, "Losses of thyristor on modified bridge type high-temperature superconducting fault current limiter," *IEEE transactions on applied superconductivity*, vol. 14, no. 2, pp. 835–838, 2004.