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Optimal modulation for AC-DC matrix converters

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Abstract

This thesis investigates modulation methods and switching pattern selection for three-phase AC–DC matrix converters, with the goal of minimizing output current ripple while considering switching losses. Existing research either focuses on a limited set of predefined patterns or optimizes individual patterns, but does not provide a comprehensive evaluation of all feasible switching patterns. One challenge addressed in this work is the extremely large number of possible patterns satisfying operational constraints, particularly for patterns with four or more switching states per half cycle, where manual optimization becomes impractical.

An automated procedure is proposed for systematic pattern generation and optimization, evaluating all feasible patterns to identify those that achieve the optimal trade-off between output current ripple and switching losses. Analytical optimization for the selected patterns enables real-time implementation, and experimental validation confirms close agreement with theoretical predictions.

Further ripple reduction is achieved by selecting an optimal set of one, two, or three patterns to be applied within a single input voltage period, with maps developed to determine the appropriate pattern based on input voltage angle and modulation index. The resulting optimized modulation strategies are compared to standard methods, demonstrating superior performance across different power factors.

Finally, a modulation approach based on discontinuous conduction mode (DCM) is introduced to improve efficiency and reduce input current distortion at low output currents. A current-control-based modulator and an output-inductance estimation method are developed, providing robust and experimentally validated steady-state and transient performance.

Abbreviations

AC	Alternating Current
CCM	Continuous conduction mode
CE	Common-emitter
CC	Common-collector
DC	Direct Current
DC-SVM	Duty Cycle Space-Vector Modulation
DCM	Disontinuous conduction mode
IGBT	Insulated Gate Bipolar Transistor
PFC	Power Factor Correction
PSU	Power supply unit
SVM	Space-Vector Modulation
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

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Chapter 1:

Introduction

Three-phase AC–DC converters have played a significant role in modern energy systems owing to the widespread utilization of the three-phase AC grid worldwide. Their ability to provide efficient, high-power conversion has made them indispensable in industrial, commercial, and utility-scale applications. In recent years, the rapid development of renewable energy systems, DC microgrids, and electric transportation has further expanded the range of applications for these converters. In particular, the growing deployment of battery energy storage systems and the increasing demand for high-speed charging infrastructure have created new opportunities and requirements for advanced three-phase AC–DC converter technologies [1].

1.1 Existing Three Phase AC-DC Converter Topologies

In the subsequent sections, existing topologies for three-phase AC–DC converters are reviewed. Several factors must be considered when evaluating converter performance. The first is the number of stages required for the conversion process. Single-stage converters are typically more efficient due to the reduced number of semiconductor devices involved in power transfer. In contrast to multi-stage converters, they do not require an intermediate DC-link capacitor, which can lead to a reduction in both weight and volume.

Another important consideration is bidirectional power transfer capability, which is essential for a wide range of applications. Input power quality and power factor correction capabilities are also critical, particularly in light of stringent regulatory requirements [2–4]. Furthermore, the output voltage regulation range must be taken into account when selecting a suitable topology.

The following subsections present representative examples of both uni- and bidirectional three-phase AC–DC converter topologies, along with an analysis of their respective

operational characteristics and performance capabilities. A more detailed review of AC–DC converter topologies is provided in [5–10].

1.1.1 Unidirectional converter topologies

The simplest form of a three-phase AC–DC converter is the passive rectifier (see Fig. 1.1(a)). Although structurally simple, this topology suffers from highly distorted input currents, an inability to regulate the output voltage, and unidirectional power flow. Power quality can be improved through the use of passive filters, active filters (see Fig. 1.1(c)), or current-controlled injection methods [5, 11–15].

Passive shunt filters are connected in parallel between the grid and the converter neutral point, providing a low-impedance path for higher-order harmonics. As a result, these harmonics flow through the filter to the neutral rather than into the grid [5]. However, such filters can interact with the system impedance, potentially leading to resonances [11]. Active filters mitigate disturbances by injecting current or voltage harmonics with equal amplitude and opposite phase [12].

Active current injection methods employ additional converters or networks (see Fig. 1.1(b)) to supply auxiliary AC-side currents, thereby reducing input current harmonics. Although the inclusion of auxiliary converters reduces overall efficiency, the power processed by the auxiliary network is typically only a fraction of the main rectifier power, which can still result in an overall efficiency improvement [13–15]. A notable subset of these topologies is the third-harmonic current injection rectifier, in which a controlled current component is injected into the AC side. AC-side injection in these systems can be implemented using

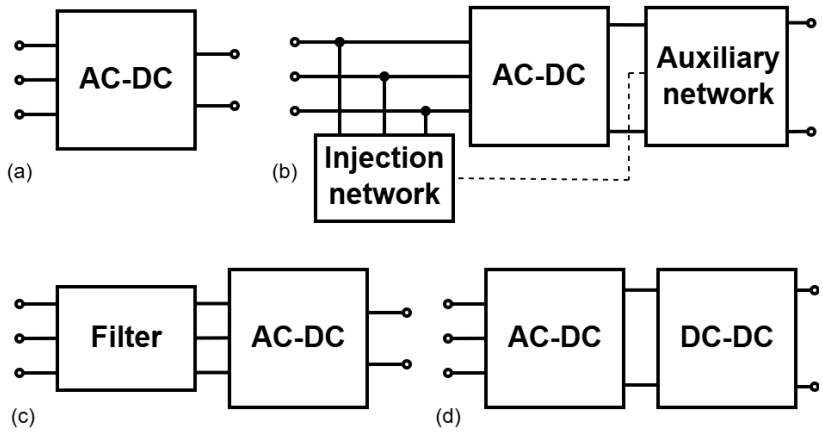

Figure 1.1: Three phase AC-DC converter topologies

bidirectional switches [15, 16] or passive injection networks [17].

Multipulse rectifiers can be used to improve input current quality and power factor. They usually consist of several standard three-phase rectifiers (6-pulse rectifiers) arranged in a specific configuration using transformers and tapped inductors [18, 19]. Due to their simplicity and high reliability, these converters are currently applied in aerospace systems [20, 21].

Thus far, the discussion has focused on enhancing input power quality, specifically by reducing higher-order harmonics in the input current, without considering output voltage regulation. The following topologies provide output voltage regulation in addition to improved input power quality.

The simplest solution for output voltage control is the introduction of a second DC–DC stage connected to a rectifier with power factor correction capability, as shown in Fig. 1.1(d). Depending on the application requirements, a buck [22, 23], boost [16, 17, 24], or buck–boost [25] converter can be used as the second stage.

The Δ-switch rectifier and the Vienna rectifier are step-up topologies that allow the formation of a phase displacement between the voltage and the fundamental component of the current [26, 27]. The three-phase buck-type PFC rectifier is a buck-derived topology that offers a wide operating range with respect to current and voltage displacement. An alternative is the active three-switch buck-type PFC rectifier, which provides a narrower displacement angle range [8]. The Swiss rectifier is a converter based on third-harmonic current injection combined with an additional buck converter [28]. This topology can operate only at unity power factor.

1.1.2 Bidirectional converter topologies

The most common approach for rectifying AC voltage while achieving high input current quality and a wide voltage–current displacement angle is the use of an active front-end (AFE) converter. The term active front end refers to a family of boost-type converters that enable bidirectional power flow with minimal current distortion and a variable power factor [29].

The most common representative of this family is the VSI-bridge-based bidirectional boost converter [30]. A unidirectional version of this topology can be obtained by replac-

ing three switches with diodes [8]. Numerous variations of the VSI-based topology exist, including four-switch configurations for cost reduction and four-wire topologies aimed at improving voltage ripple, balancing supply currents, and enabling operation under unbalanced supply voltage conditions [31, 32].

The three-level neutral-point-clamped (NPC) converter provides performance comparable to that of the VSI-based AFE while requiring a smaller input filter inductance and enabling higher switching frequencies. Its main drawback is the increased number of components [29]. The three-level T-type converter is a bidirectional variant of the Vienna rectifier. It is similar to the NPC converter but exhibits slightly lower switching losses [33, 34].

One representative of buck-type converters is the bidirectional Swiss rectifier. Compared to its unidirectional version, all diodes are replaced with active switches [35, 36]. The displacement between the input voltage and current must remain within the range $-\pi/6 \leq \varphi \leq \pi/6$ to avoid input current distortion.

The buck–boost Y-rectifier is a bidirectional quasi-single-stage converter. Although it consists of two stages, namely buck and boost, only one stage is required to operate at high switching frequency to achieve the desired output voltage [37, 38].

The AC–DC matrix converter is a single-stage bidirectional buck converter [39]. It is derived from the AC–AC matrix converter by removing one leg. Power factor variation can be achieved at the cost of a reduced maximum output voltage. A comparison of the AC–DC matrix converter with a two-stage converter for plug-in electric vehicle charging, presented in [40], demonstrates the superior power density of the matrix converter.

For converters with a limited output voltage range, a second DC–DC stage can be added to achieve full-range operation. A comprehensive review of bidirectional DC–DC converters is provided in [41].

A notable DC–DC topology that represents a strong candidate for the second stage is the dual-active-bridge (DAB) converter. It is an isolated, highly efficient buck–boost converter [42, 43]. Since the DAB consists of two H-bridges connected by a high-frequency transformer, alternative converter topologies can be integrated in place of the primary H-bridge to form three-phase AC–DC buck–boost isolated converters, such as the AC–DC matrix DAB converter [44–46] and the Swiss DAB [47].

As a single-stage AC–DC converter with sinusoidal input currents and power factor control capability, the AC–DC matrix converter represents a suitable candidate for systems requiring step-down voltage regulation. The following section examines the state of research on AC–DC matrix converters in greater detail.

1.2 Literature review on AC-DC Matrix converters

In 1981, the first modulation method for AC–AC matrix converters was presented in [48]. The proposed solution exhibited a limited output voltage ratio. This limitation was addressed in 1989 by the same researchers [49]. In the same year, the first space vector modulation (SVM) approach for matrix converters was introduced [50]. This modulation treated the matrix converter as a two-stage converter, leading to the development of indirect SVM. Two years later, the direct SVM method was proposed [51]. In 1992, results developed for AC–AC matrix converters were adapted for AC–DC matrix converters [39].

Several modulation strategies for AC–DC matrix converters have been reported in the literature. In general, a modulation strategy is required to fulfill the following objectives:

- Correct output voltage regulation;
- Sinusoidal input currents;
- Accurate power factor control.

A comparison of modulation strategies is presented in [52]. The authors distinguish between pulse-width modulation (PWM), where the duty cycle for the connection of each input–output terminal is determined separately, and SVM [53–57], where the duty cycles for applying specific line-to-line voltages to the output terminals are calculated based on the input current reference angle. The main advantages of SVM include straightforward implementation and inherently simple power factor control.

Model predictive control (MPC) based on SVM is proposed in [57], where the inclusion of virtual space vectors in the cost function leads to improved current ripple reduction and enhanced dynamic response. Finite control set MPC is investigated in [58], where the authors also introduce an observer for input voltage estimation.

An improved SVM scheme that reduces common-mode voltage and accounts for the narrow pulse problem is proposed in [59]. To address significant harmonic distortion at low modulation indices, [60] proposes switching sequences that incorporate additional zero states.

During duty cycle calculation, several degrees of freedom exist that can influence converter performance. In each PWM cycle, the required output voltage and input current can be achieved by connecting the output to two out of the three available line-to-line voltages. The selection of applied voltages, the connection phase of the zero state, and the switching pattern can significantly affect switching losses, output current ripple, input current distortion, and the maximum achievable output voltage.

The problem of modulation strategy selection has been addressed in several studies on matrix converters [61–64]. A genetic algorithm is employed in [65] to optimize the distribution and sequencing of passive duty cycles. The performance of Z-source ultra-sparse matrix converters, including input current and output voltage THD as well as switching losses, is analyzed for various patterns with and without zero states in [66]. A modulation scheme for isolated AC–DC matrix converters is introduced in [67], combining vector sequence allocation and duty cycle adjustment to reduce both DC-side current ripple and AC-side current distortion at high modulation indices.

Switching pattern selection for minimizing switching losses is discussed in [68–70]. For high modulation indices, it is proposed to eliminate zero states and control the converter using only active duty cycles. At low modulation indices, active duty cycles corresponding to lower line-to-line voltages are preferred. A similar pattern selection strategy is proposed in [71] to reduce current ripple, along with a method to compensate for the displacement between input voltage and current caused by the input filter. In [55], output current ripple is reduced through an improved SVM approach, where optimal placement of passive duty cycles also enhances input current total harmonic distortion (THD). A similar methodology is presented in [56], which additionally examines the influence of power factor on input current ripple and harmonic content. The impact of the number and type of passive duty cycles on converter efficiency is investigated in [72], concluding that certain patterns improve input current THD, while others enhance converter efficiency.

Efficiency improvement has been extensively studied for isolated matrix-based AC–DC converters [46, 73–75]. Zero-current switching is achieved by equalizing the volt-seconds in the primary and secondary windings during one switching cycle and aligning the rising or falling edges of the primary and secondary voltages. As a result, the same current flows at the beginning and end of the cycle. In [73], a voltage commutation compensation method is proposed to eliminate current offsets between cycles caused by commutation delays.

Despite the significant body of work on switching pattern selection and modulation strategies for AC-DC matrix converters, there are limitations in the existing literature. Most studies focus either on a limited subset of switching patterns or on the optimization of predefined modulation schemes, typically demonstrating improved performance with respect to a specific objective such as switching losses, output current ripple, or input current distortion. However, these approaches are generally constrained by the initial selection of candidate patterns and therefore do not provide a comprehensive assessment of the full solution space. As a result, the reported improvements are often relative to conventional or baseline methods rather than indicative of globally optimal performance.

Consequently, there remains a need for a more comprehensive and systematic investigation that considers a global set of feasible switching patterns and evaluates their performance across various operating conditions.

1.3 Thesis structure

This thesis consists of five chapters. The content of each chapter is summarized as follows:

- Chapter 2 provides a summary of the operating principles of AC–DC matrix converters. The main converter components are described, and commutation techniques required for proper operation are presented.
- Chapter 3 focuses on modulation techniques for AC–DC matrix converters. Existing methods, including duty-cycle modulation, space vector modulation (SVM), and duty-cycle–SVM approaches, are reviewed and compared.

- Chapter 4 addresses the problem of switching pattern selection and optimization. Patterns that achieve the best trade-off between output current ripple and switching losses are identified for different operating conditions. Further optimization within a single input voltage period is also performed to reduce output current ripple even more. Selected patterns are validated experimentally and compared with approaches reported in the literature.

- Chapter 5 presents a modulation strategy designed to improve converter performance under low output current conditions. The method targets reductions in input current THD, output current ripple, and switching losses. A discontinuous conduction mode (DCM) modulation algorithm is developed, implemented, and experimentally tested. The results are compared with standard modulation techniques to demonstrate performance improvements.

- Conclusions summarize the main findings of the thesis, highlighting the contributions in modulation optimization, switching pattern selection, and DCM-based performance enhancement.

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Chapter 2:

Basics of AC-DC Matrix Converters

The AC–DC matrix converter is a single-stage converter that enables direct conversion from three-phase AC voltage to DC voltage. It is a buck-type converter, meaning that the output voltage cannot exceed the maximum input line-to-line voltage. The converter can enforce sinusoidal input currents with a variable power factor. The converter topology is shown in Fig. 2.1 and consists of an input filter, six bidirectional switches, an output inductor and capacitor, and the load.

2.1 Principle of operation

The principle of operation of the converter is as follows: at any instant, two output terminals of the converter can be connected to any input phase. Simultaneous connection of an output terminal to multiple input phases is not allowed, as it would create a short circuit. Let the instantaneous input phase voltages be $V_{in1}, V_{in2}, V_{in3}$:

$$\begin{aligned} V_{in1} &= V_{mag} sin(\theta), \\ V_{in2} &= V_{mag} sin\left(\theta - \frac{2\pi}{3}\right), \\ V_{in3} &= V_{mag} sin\left(\theta + \frac{2\pi}{3}\right), \end{aligned} \tag{2.1}$$

where V_{mag} is the phase voltage magnitude and θ is the input voltage angle.

The corresponding line-to-line voltages are given by:

$$\begin{aligned} V_{l-l1} &= V_{in1} - V_{in2}, \\ V_{l-l2} &= V_{in2} - V_{in3}, \\ V_{l-l3} &= V_{in3} - V_{in1}. \end{aligned} \tag{2.2}$$

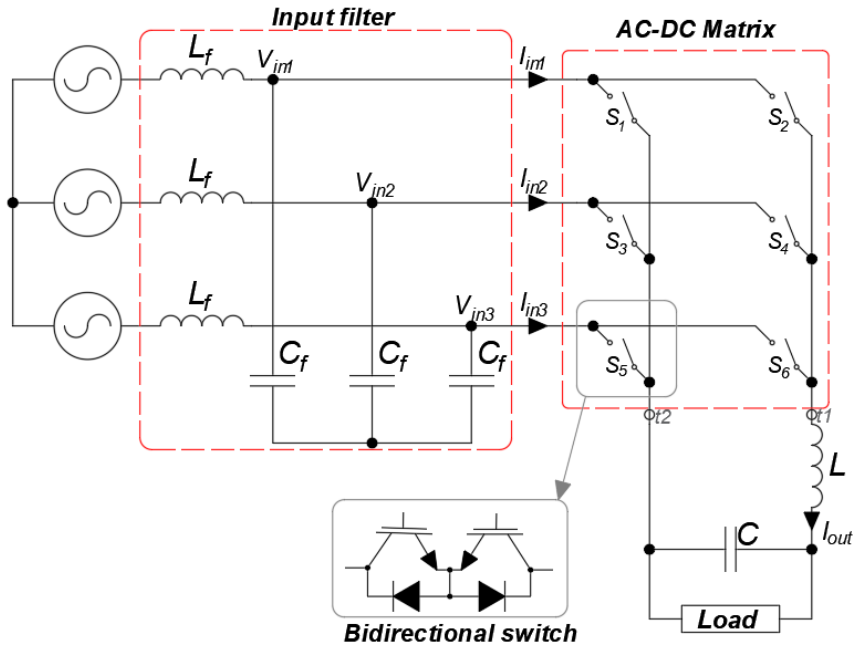

Figure 2.1: AC-DC matrix converter scheme

Since each output terminal can be connected to any input phase, there are seven possible states that can be formed at the output terminals:

$$V_{out} \in [-V_{l-l3}, -V_{l-l2}, -V_{l-l1}, 0, V_{l-l1}, V_{l-l2}, V_{l-l3}]. \tag{2.3}$$

A zero output voltage occurs when both output terminals are connected to the same input phase. For future reference, an output voltage of zero is referred to as a passive state, while any nonzero output voltage corresponds to an active state.

Assuming a fixed switching cycle, the duty cycle for a state x is defined as:

$$d_x = \frac{T_x}{T_s}, \tag{2.4}$$

where T_s is the switching period and T_x is the duration for which state x is applied to the output terminals. Similarly, the duty cycle during which the converter is in a passive state is called the passive duty cycle, while that for an active state is called the active duty cycle.

When an output terminal is connected to a specific input phase, the output current I_{out} flows through that phase. The direction of the current depends on which terminal the input phase is connected to. For instance, if phase 1 is connected to terminal $t1$, then

$I_{in1} = I_{out}$; if connected to terminal $t2$, then $I_{in1} = -I_{out}$; and if not connected to any terminal, $I_{in1} = 0$.

The input currents $I_{in1}, I_{in2}, I_{in3}$ have a pulse-like waveform, which is smoothed by the input filter.

In general, during each switching cycle, the control objectives are:

- Control the average output voltage V_{out}.
- Ensure sinusoidal input currents.
- Maintain the reference input power factor.

Considering that the input voltages are continuously varying, the following notations are introduced for future reference: $V_h \geq V_m \geq V_l$ represent the positive-sorted input line-to-line voltages, with corresponding duty cycles d_h, d_m, d_l for their application. For the application of negative voltages, duty cycles with a negative sign are used. According to (2.4), the following condition must be satisfied in every switching cycle:

$$|d_h| + |d_m| + |d_l| + |d_0| = 1, \tag{2.5}$$

where d_0 is the passive duty cycle - duty cycle in which both output terminals are connected to the same phase.

The input voltages are sinusoidal signals (see Fig. 2.2). Table 2.1 shows the input voltages that need to be applied to the output terminals in order to achieve a specific output voltage V_{out}. Assuming that input angle and indexes of input phases are determined as shown in (2.1), V_h, V_m and V_l are composed from the phase voltages with the indexes shown in the table depending on the angle value.

Active and passive duty cycle selection is performed to ensure the fulfillment of the control objectives described above. Modulation techniques are discussed in greater detail in the following chapter.

Once the duty cycles are calculated, the corresponding voltages must be applied to the output terminals in the next switching cycle T_s. Typically, the calculated duty cycles are compared to a carrier signal according to a specific order, referred to as the switching pattern. Carrier signals can have either a symmetric triangular or a sawtooth

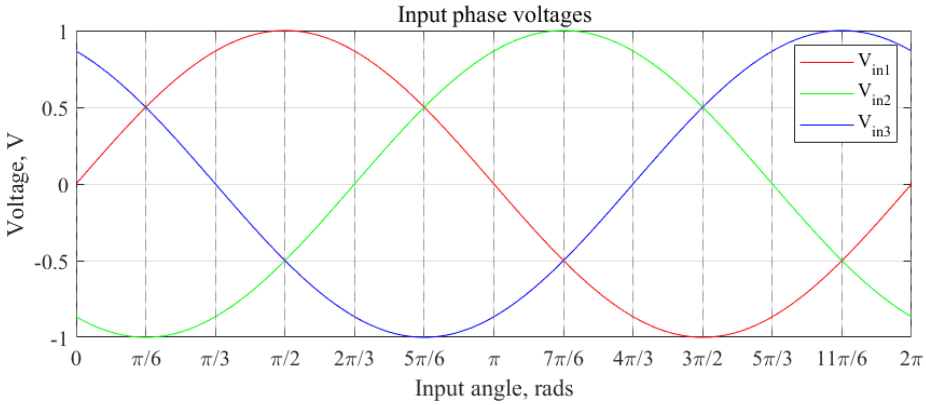

Figure 2.2: Input phase voltages

waveform (Fig. 2.3). The symmetric triangular form provides the benefit of a symmetric output current waveform. In steady state, the average output current over one switching cycle equals the instantaneous current at the start, middle, and end of the cycle. This allows the average current to be measured at a single fixed moment within the cycle. When using a sawtooth carrier, more advanced methods are required to estimate the average output current if the output current ripple is non-negligible. Switching pattern determines the order in which duty cycles are compared to the carrier. In the figure, d_h is compared to the carrier first, d_m is the second and d_0 is the third. When the carrier value is in the range of the duty cycle ([0,d_h] for d_h, (d_h, $d_h + d_m$] for d_m, etc.), the corresponding voltage is applied to the output.

Fig. 2.3 also illustrates which input voltages are connected to the output terminals for an input angle of $\theta = 0$ rad, according to Table 2.1. A zero output voltage occurs when both output terminals are connected to the same input phase. The converter performs one commutation each time the input phase connected to any terminal changes. The losses per commutation depend on both the current and voltage, as will be discussed in the following sections.

The selection of the input phase for generating zero output voltage should minimize the total number of commutations. In the pattern shown in Fig. 2.3 with a symmetric carrier wave, either phase 1 or phase 2 can be chosen, resulting in one commutation before and after the zero state. In contrast, choosing phase 3 for the zero state would result in four commutations.

Table 2.1: Correspondence between input phase numbers and line-to-line voltages

Input angle range	Number of input phases to connect to terminals $t1$ and $t2$		
	V_h	V_m	V_l
$[0, \frac{\pi}{6})$	$[3, 2]$	$[1, 2]$	$[3, 1]$
$[\frac{\pi}{6}, \frac{\pi}{3})$	$[1, 2]$	$[3, 2]$	$[1, 3]$
$[\frac{\pi}{3}, \frac{\pi}{2})$	$[1, 2]$	$[1, 3]$	$[3, 2]$
$[\frac{\pi}{2}, \frac{2\pi}{3})$	$[1, 3]$	$[1, 2]$	$[2, 3]$
$[\frac{2\pi}{3}, \frac{5\pi}{6})$	$[1, 3]$	$[2, 3]$	$[1, 2]$
$[\frac{5\pi}{6}, \pi)$	$[2, 3]$	$[1, 3]$	$[2, 1]$
$[\pi, \frac{7\pi}{6})$	$[2, 3]$	$[2, 1]$	$[1, 3]$
$[\frac{7\pi}{6}, \frac{4\pi}{3})$	$[2, 1]$	$[2, 3]$	$[3, 1]$
$[\frac{4\pi}{3}, \frac{3\pi}{2})$	$[2, 1]$	$[3, 1]$	$[2, 3]$
$[\frac{3\pi}{2}, \frac{5\pi}{3})$	$[3, 1]$	$[2, 1]$	$[3, 2]$
$[\frac{5\pi}{3}, \frac{11\pi}{6})$	$[3, 1]$	$[3, 2]$	$[2, 1]$
$[\frac{11\pi}{6}, 2\pi)$	$[3, 2]$	$[3, 1]$	$[1, 2]$

2.2 Bidirectional switches

The bidirectional switch shown in Fig. 2.4 consists of two IGBTs with antiparallel diodes connected together. Depending on the connection point, two variations of bidirectional switches exist: the common-collector (CC) and the common-emitter (CE) configurations.

Each configuration has its advantages and disadvantages. The CC topology requires fewer power supply units (PSUs) compared to CE; however, each PSU must be larger to supply three IGBTs instead of two. This can limit available options, especially for high-power converters. In contrast, the CE topology uses floating PSUs for each IGBT pair, which allows more predictable behavior in terms of electrical noise. In the CC topology, three PSUs are floating while three follow the grid.

From a PCB layout perspective, the CE topology is simpler and more efficient, as the IGBTs of the same bidirectional switch are physically located close to each other. Based on these considerations, the CC topology is generally more suitable for low-power converters, the CE topology for medium-power converters, and in high-power converters, each IGBT typically has a separate PSU, making the difference between topologies negligible.

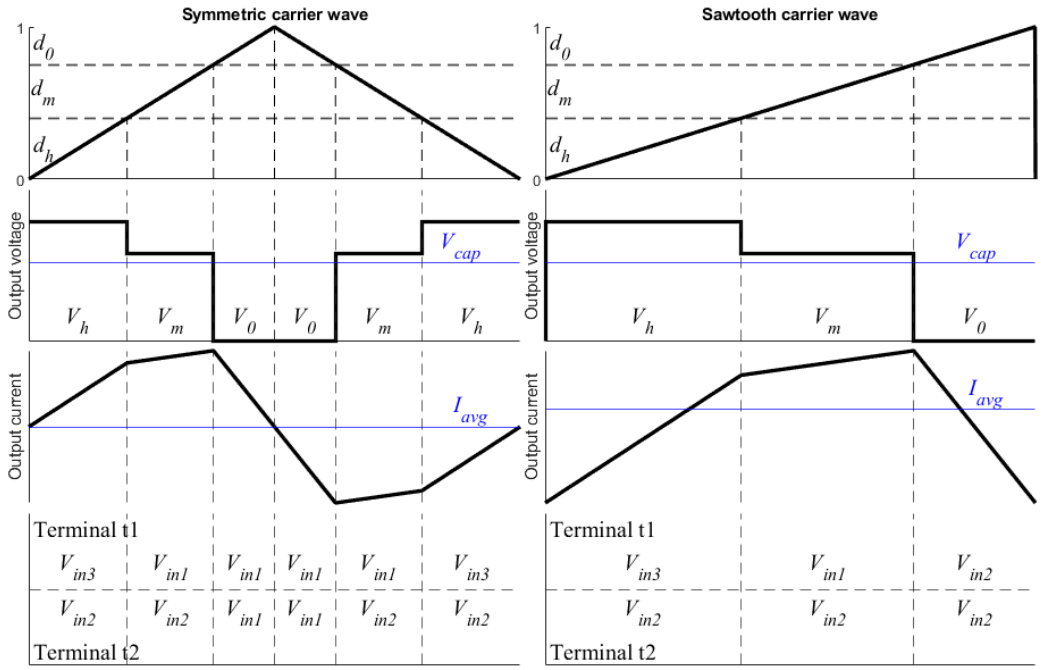

Figure 2.3: Comparison of symmetric and sawtooth carrier waves. The pattern follows the order V_h, V_m, V_0. Terminal connections for input angle $\theta = 0$ rad are shown.

In this thesis, a common-emitter bidirectional switch is used for both simulations and experimental implementations.

2.3 Commutation strategy

During converter operation, each output terminal can be connected to only one input phase; otherwise, a short circuit between input phases will occur. As the output terminal switches between input phases, ensuring safe commutation becomes critical. Several commutation methods have been proposed in the literature [1, 2]. The most common approach is the so-called four-step commutation [3]. As the name implies, the

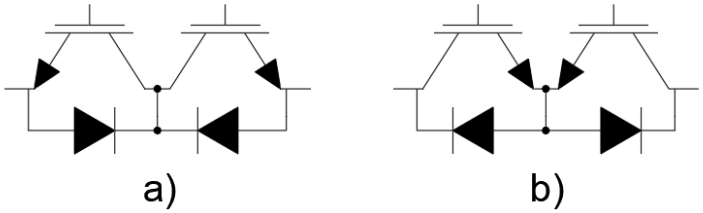

Figure 2.4: Bidirectional switch topologies: a) Common-collector (CC), b) Common-emitter (CE).

procedure consists of four steps. Fig. 2.5 illustrates the commutation process between two bidirectional switches.

Initially, the output terminal `Out` is connected to input phase `In1`, with both IGBTs S_1 and S_2 turned on. Depending on the current direction, only one of the IGBTs conducts the current. For example, if the current flows from the input to the output, S_1 and diode D_2 conduct the current.

The four steps of the commutation procedure are as follows:

1. Turn off switch S_2. The current continues to flow in the same direction through phase `In1`.
2. Turn on the IGBT of phase `In2` that will conduct the current. Based on the current direction, this is S_3.
3. Turn off the IGBT that was previously conducting current. In this case, it is S_1.
4. Turn on the remaining IGBT of phase `In2`, which is S_4.

Depending on the voltages of the input phases and the direction of the output current, the conduction state may change after the second or third step of the commutation procedure. If S_3 begins to conduct immediately after it is turned on, a soft commutation occurs. If S_1 continues to conduct even after S_3 is turned on, and the conduction state changes only after S_1 is turned off, a hard commutation occurs. Table 2.2 summarizes the conditions that lead to soft and hard commutations.

A time delay, commonly referred to as the dead time, is introduced between commutation steps to ensure that each IGBT is fully turned on or off before the next step. Dead time has a negative effect on converter performance because the actual control outputs applied to the converter differ from the reference values.

Table 2.2: Commutation type depending on input phase voltage relation and output current direction

Current direction	Voltage relation	
	$V_{in1} > V_{in2}$	$V_{in1} \leq V_{in2}$
Input $\rightarrow$ Output	"hard"	"soft"
Output $\rightarrow$ Input	"soft"	"hard"

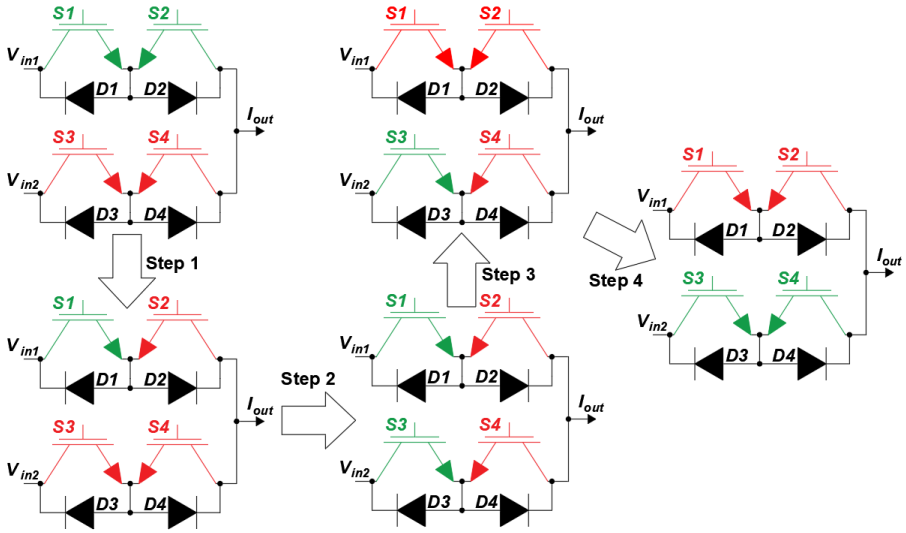

Figure 2.5: 4-step commutation diagram

Table 2.3: Commutation cases for different carrier waves

N	Voltage difference	Current direction	Commutation type
Symmetric carrier wave			
1a	$V_{in3} \rightarrow V_{in1}$	Input → Output	"hard"
2a	$V_{in2} \rightarrow V_{in1}$	Output → Input	"hard"
3a	$V_{in1} \rightarrow V_{in2}$	Output → Input	"soft"
4a	$V_{in1} \rightarrow V_{in3}$	Input → Output	"soft"
Sawtooth carrier wave			
1b	$V_{in3} \rightarrow V_{in1}$	Input → Output	"hard"
2b	$V_{in1} \rightarrow V_{in2}$	Input → Output	"hard"
3b	$V_{in2} \rightarrow V_{in3}$	Input → Output	"soft"

2.3.1 Switching losses

Switching losses occur in IGBTs and diodes when an output terminal switches between input phases. The source of the losses depends on the type of commutation. During soft commutation, turn-on losses of the IGBT that begins to conduct (e.g., S_3 in Fig. 2.5) and turn-off losses of the diode (D_2) occur. In contrast, during hard commutation, turn-off losses of the IGBT that was previously conducting (e.g., S_1) occur.

Fig. 2.6 shows the switching losses of the IGBT and diode for the Infineon IGBT with antiparallel diode (IKY50N120CH7) used in simulations and experiments. The losses are approximately linearly proportional to the current magnitude and the voltage difference

before and after the commutation. Therefore, the selection of the switching pattern has a direct influence on the total switching losses during operation.

In Fig. 2.3, patterns with symmetric and sawtooth carrier waves are compared for an input angle of $\theta = 0$ rad. Table 2.3 provides a comparison of the commutation types for both patterns. The symmetric carrier wave pattern results in four commutations per cycle, while the sawtooth carrier pattern results in three commutations (including the inter-cycle commutation). Despite this apparent advantage, the voltage difference in commutation 3b ($V_{in3} - V_{in2}$) equals the sum of the voltage differences in commutations 3a ($V_{in3} - V_{in1}$) and 4a ($V_{in1} - V_{in2}$), leading to very similar power losses for both patterns when taking the curves in Fig. 2.6 into account. This analysis can be extended to other patterns and input voltage angles.

Considering the analysis above and the benefit of achieving a symmetric output current waveform, this thesis focuses on the study of switching patterns with a symmetric carrier wave.

Half of the commutations are always "soft" and half - "hard" for the symmetrical carrier due to its structure. Power losses per one cycle for symmetrical carrier wave are

$$\begin{aligned} P_{sw-loss} = \sum_{t=1}^{2} \Big(& \sum_{s=1}^{n-1} e_{igbt-on}(i_{out}, v_{diff}(t,s), T_j) \\ & + \sum_{s=1}^{n-1} e_{igbt-off}(i_{out}, v_{diff}(t,s), T_j) \\ & + \sum_{s=1}^{n-1} e_{diode-off}(i_{out}, v_{diff}(t,s), T_j) \Big) f_{pwm} \end{aligned} \tag{2.6}$$

where n is a number of states per half cycle; $v_{diff}(t,s)$ is a difference between output voltage in two adjacent states $v_{diff}(t,s) = v_{out}(t,s+1) - v_{out}(t,s)$; t is a terminal number; T_j is a junction temperature; $e_{igbt-on}$, $e_{igbt-off}$ are turn-on and turn-off losses in IGBT; $e_{diode-off}$ - turn-off losses in diode.

2.4 Input filter

The input filter of the AC-DC matrix converter serves the purpose of reducing the harmonic content of the input currents. The most common filter type is a single-stage

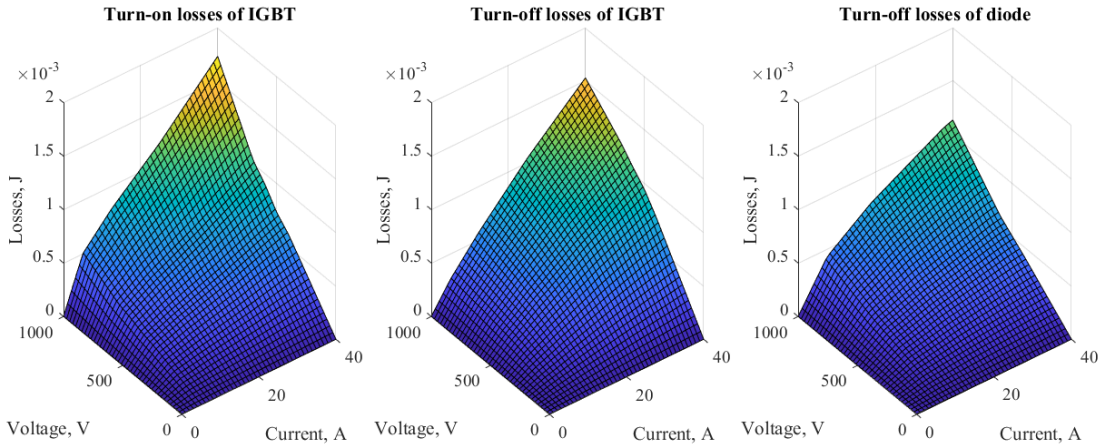

Figure 2.6: Switching losses of IGBT and diode for IKY50N120CH7. Junction temperature $T_j = 20°C$

LC filter [4] (see Fig. 2.1).

When selecting elements for the filter, several considerations have to be taken into account [5–7]:

- Input current and voltage displacement at low power should be minimal. Depending on power quality requirements, exact values can differ. In [5], the input filter is chosen so that the input power factor is greater than 0.8 at 30% of rated power. The following formula is used for the calculation of the input filter capacitor C_f:

$$C_f \leq \frac{PF_{min}P_{min}}{\omega_{grid}v_{l-l}^2} \tag{2.7}$$

  where P_{min} is the minimum power at which the power factor requirement applies, PF_{min} is the minimum allowed power factor at P_{min}, ω_{grid} is the grid angular velocity, and u_{l-l} is the line-to-line voltage.

- The voltage drop across the inductance should be minimal so as not to limit the maximum output voltage of the converter. The maximum voltage drop Δu at full load for a given inductance is

$$\frac{\Delta u}{u_p} = 1 - \sqrt{1 - (\omega_{grid}L_f)^2 \left(\frac{i_n}{u_n}\right)^2} \tag{2.8}$$

  where i_n and u_n are the rated input phase current and voltage, respectively.

- One of the benefits of the converter is its reduced size compared to two-stage

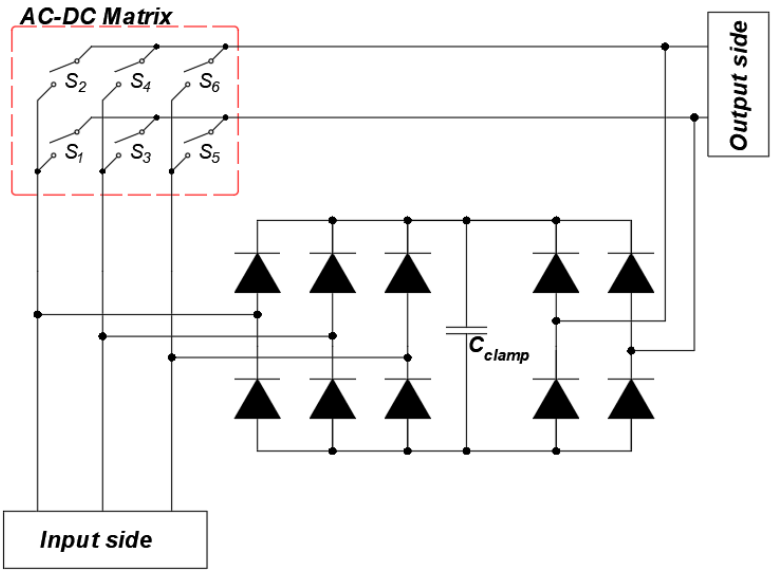

Figure 2.7: Clamp circuit

converters; therefore, input filter elements should be chosen to keep the filter as compact as possible.

- The resonance frequency of the filter has to be lower than the switching frequency of the converter but higher than the grid frequency. The input filter inductance is calculated as

$$L_f = \frac{1}{\omega_r^2 C_f} \tag{2.9}$$

2.5 Clamp circuit

The clamp circuit is designed to protect the converter from overvoltages on both the input and output sides, particularly during fault conditions [8]. The traditional clamp circuit is shown in Fig. 2.7. It consists of two high-speed bridge diodes connected to a capacitor. When a fault occurs, or when operation stops while there is residual inductive current in the load and the bidirectional switches are turned off, all energy stored in the load is dissipated in the capacitor C_{clamp}. Without the clamp module, overvoltage may occur, potentially causing damage to the switches, since the converter has no freewheeling paths.

2.6 Chapter Summary

This chapter presented the fundamental principles and operation of the AC-DC matrix converter, a single-stage topology that directly converts three-phase AC input voltages into a controllable DC output without intermediate energy storage. Owing to its buck-type characteristic, the output voltage is limited by the input line-to-line voltages. The converter, however, enables sinusoidal input currents and controllable power factor operation.

The conversion process relies on appropriate switching of bidirectional devices to connect the output to the input phases, thereby synthesizing the desired output voltage from discrete line-to-line voltage levels. The modulation strategy, based on controlling the duty cycles of selected switching states, is essential for achieving a smooth output voltage while maintaining desirable input current characteristics.

The chapter also discussed key auxiliary components. An input filter is required to attenuate switching harmonics and ensure compliance with grid requirements, with its design involving a trade-off between performance and resonance constraints. Additionally, a clamp circuit is necessary to protect the converter against overvoltages caused by the lack of natural freewheeling paths.

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Chapter 3:

Modulation methods of AC-DC matrix converters

Several modulation methods exist for calculating duty cycles in AC-DC matrix converters. In the first section, a comparison of the existing modulation methods for AC-DC matrix converters is presented. This is followed by an assessment of power factor variation for the converter.

3.1 Review of modulation methods

This section presents the main modulation techniques: duty-cycle modulation, space-vector modulation, and duty-cycle space-vector modulation. Under identical operating conditions, each modulation method can achieve the same output results. However, there are several degrees of freedom when calculating duty cycles, and the way these degrees of freedom are managed differs among the methods. This makes the choice of a particular modulation method dependent on the specific objectives to be achieved.

3.1.1 Duty cycle modulation

The output voltage of an AC-DC matrix converter, denoted as V_o^*, is expressed by the equation:

$$V_o^* = d_1(V_a - V_b) + d_2(V_b - V_c) + d_3(V_a - V_c) \tag{3.1}$$

Here, d_1, d_2, and d_3 represent the active duty cycles. The variables V_a, V_b, and V_c denote the ordered set of the input voltages $\{V_{in1}, V_{in2}, V_{in3}\}$ arranged in non-increasing order, such that

$$V_a \geq V_b \geq V_c,$$

where

$$V_a = \max\{V_{in1}, V_{in2}, V_{in3}\}, \quad V_c = \min\{V_{in1}, V_{in2}, V_{in3}\},$$

and $V_b \in \{V_{in1}, V_{in2}, V_{in3}\} \setminus \{V_a, V_c\}$ denotes the intermediate value.

The duty cycles d_1, d_2, and d_3 correspond to the application of the voltage vectors V_{ab}, V_{bc}, and V_{ac}, respectively, defined as

$$V_{ab} = V_a - V_b, \quad V_{bc} = V_b - V_c, \quad V_{ac} = V_a - V_c.$$

Negative duty cycles indicate that the corresponding voltage vector is applied with reversed polarity. V_o^* denotes the output voltage reference.

To ensure correct operation, the following constraint must be fulfilled:

$$|d_1| + |d_2| + |d_3| + d_0 = 1 \tag{3.2}$$

Achieving a unity input power factor requires the following condition to be satisfied:

$$\frac{V_a}{I_a} = \frac{V_b}{I_b} = \frac{V_c}{I_c} \tag{3.3}$$

In this expression, I_a, I_b, and I_c denote the instantaneous input currents of each respective phase, which can be calculated as follows:

$$\begin{aligned} I_a &= d_1 I_{d_1} + d_3 I_{d_3} \\ I_b &= -d_1 I_{d_1} + d_2 I_{d_2} \\ I_c &= -d_2 I_{d_2} - d_3 I_{d_3} \end{aligned} \tag{3.4}$$

Here, I_{d_x} represents the average output current associated with the active duty cycle d_x, where $x \in [1, 2, 3]$. The condition in (3.3) must be maintained throughout each switching period. The system of equations (3.1), (3.2), (3.3), and (3.4) can be solved for d_1, d_2, and d_3 [1].

As previously mentioned, the use of a triangular carrier results in symmetrical voltage and current waveforms. Consequently, the average current during any given duty cycle is identical to the overall average output current, I_{out}, throughout the PWM period.

Therefore, $I_{out} = I_{d_1} = I_{d_2} = I_{d_3}$.

As a result, (3.3) and (3.4) can be simplified as:

$$\frac{V_a}{d_1 + d_3} = \frac{V_b}{-d_1 + d_2} = \frac{V_c}{-d_2 - d_3} \tag{3.5}$$

Equations (3.5) and (3.3) are valid only for a unity input power factor. The phase voltage-to-current relationships, taking into account the displacement angle φ between current and voltage, are expressed as:

$$\frac{V_a sin(\theta_a + \varphi)}{I_a sin(\theta_a)} = \frac{V_b sin(\theta_b + \varphi)}{I_b sin(\theta_b)} = \frac{V_c sin(\theta_c + \varphi)}{I_c sin(\theta_c)} \tag{3.6}$$

Here, θ_a, θ_b, and θ_c are the input angles of the voltages V_a, V_b, and V_c. The input angles are determined from the phase voltages V_{in1}, V_{in2}, and V_{in3} depending on the input voltage angle θ. For example, for θ in the region $[0, \frac{\pi}{6})$, $\theta_a = \theta + \frac{2\pi}{3}$, $\theta_b = \theta$, and $\theta_c = \theta - \frac{2\pi}{3}$.

Relations (3.3) and (3.6) consist of two equations with thee variables, meaning that one of the duty cycles can be chosen freely. Switching losses can be reduces if one of the active duty cycles is set to zero. Below are examples of the solutions to the system of equations (3.1), (3.2), (3.6), and (3.4).

Duty cycle $d_1 = 0$:

$$\begin{cases} A_{23} = \dfrac{sin(\theta_b + \varphi)}{sin(\theta_a + \varphi)} \\ d_3 = \dfrac{V_o^*}{A_{23}(V_b - V_c) + V_a - V_c} \\ d_2 = A_{23} d_3 \end{cases} \tag{3.7}$$

Duty cycle $d_2 = 0$:

$$\begin{cases} A_{13} = \dfrac{sin(\theta_b + \varphi)}{sin(\theta_c + \varphi)} \\ d_3 = \dfrac{V_o^*}{A_{13}(V_a - V_b) + V_a - V_c} \\ d_1 = A_{13} d_3 \end{cases} \tag{3.8}$$

Duty cycle $d_3 = 0$:

$$\begin{cases} A_{12} = \dfrac{sin(\theta_a + \varphi)}{sin(\theta_c + \varphi)} \\ d_2 = \dfrac{V_o^*}{-A_{12}(V_a - V_b) + V_b - V_c} \\ d_1 = -A_{12} d_2 \end{cases} \tag{3.9}$$

Duty cycle $d_0 = 0$ (assuming positive d_1, d_2, d_3):

$$\begin{cases} A_{123} = \dfrac{sin(\theta_a + \varphi)}{sin(\theta_c + \varphi)} \\ d_1 = -\dfrac{V_o^* - V_b + V_c + A_{123}(V_a - V_b)}{-A_{123}(V_a - V_b) + V_b - V_c} \\ d_2 = \dfrac{V_b - V_c + A_{123}(-V_a + V_b + V_o^*)}{-A_{123}(V_a - V_b) + V_b - V_c} \\ d_3 = \dfrac{V_o^* - V_b + V_c + A_{123}(V_a - V_b - V_o^*)}{-A_{123}(V_a - V_b) + V_b - V_c} \end{cases} \tag{3.10}$$

The highest, medium and the lowest line-to-line voltages introduced in the previous chapter, can be derived also from V_a, V_b and V_c:

$$\begin{gathered} V_h = V_{ac} \\ [V_m, V_l] = \begin{cases} [V_{ab}, V_{bc}] & \text{if } V_{ab} > V_{bc} \\ [V_{bc}, V_{ab}] & \text{otherwise} \end{cases} \end{gathered} \tag{3.11}$$

And corresponding duty cycles:

$$\begin{gathered} d_h = d_3 \\ [d_m, d_l] = \begin{cases} [d_1, d_2] & \text{if } V_{ab} > V_{bc} \\ [d_2, d_1] & \text{otherwise} \end{cases} \end{gathered} \tag{3.12}$$

3.1.2 Space-vector modulation

As discussed in the previous chapters, the six bidirectional switches of the converter are commutated in such a way that each output terminal is connected to one input phase at any moment of time, resulting in nine possible states at the converter output. Six of these states are active and apply one of the line-to-line voltages to the converter output, while three are passive states, in which both output terminals are connected to the same input phase. In space-vector modulation, each state is represented as a vector forming a space-vector hexagon (Fig. 3.1) [2, 3].

The direction of each vector is determined by the input phases used for its creation. The subscripts of the vectors $\overline{I_{xy}}$ indicate the phase numbers used in the vector. The hexagon is divided by the active vectors into six sectors. Vectors $\overline{i}$ and $\overline{v}$ represent the

reference input current and input voltage vectors, respectively, and are displaced by the angle φ. The direction of $\overline{v}$ is determined by the input angle θ. In every real-time cycle, the sector is selected based on the direction of the current vector $\overline{i}$. Once the sector is determined (in Fig. 3.1, $\overline{i}$ is located in sector I), the relative angle within the sector is calculated. If the input voltages are defined as in (2.1), then θ_s is given by

$$\theta_s = mod\left(\theta + \frac{\pi}{2} + \frac{\pi}{6} + \varphi, \frac{\pi}{3}\right) \tag{3.13}$$

In conventional SVM, two adjacent active vectors within the sector and a passive vector are combined to reconstruct the reference input current vector $\overline{i}$. The magnitude of the vectors is determined by the modulation index and the displacement angle φ:

$$\begin{aligned} d_r &= \frac{2}{3}\frac{m}{|cos\varphi|}sin\left(\frac{\pi}{3} - \theta_s\right) \\ d_l &= \frac{2}{3}\frac{m}{|cos\varphi|}sin(\theta_s) \end{aligned} \tag{3.14}$$

where d_r and d_l are the duty cycles of the projections of the current vector to the right and to the left side of the sector (see Fig. 3.1), respectively, with respect to the direction of $\overline{i}$. The modulation index is defined as

$$m = \frac{V_o^*}{V_{mag}} \tag{3.15}$$

According to the definition in (3.15), $m \in [0\,1.5]$. For this reason, d_r and d_l are multiplied by $\frac{2}{3}$ in (3.14).

After calculating d_r and d_l, the input phases used for duty cycle application are determined based on the sector number.

3.1.3 Duty cycle space-vector modulation

A different modulation strategy is presented in [4, 5], originally developed for AC–AC matrix converters [6]. In contrast to conventional duty-cycle or space-vector modulation, duty-cycle space-vector modulation (DC-SVM) calculates the duty cycle of each individual bidirectional switch state for the subsequent PWM cycle, rather than determining duty cycles for specific line-to-line voltage applications. Moreover, the method introduces a

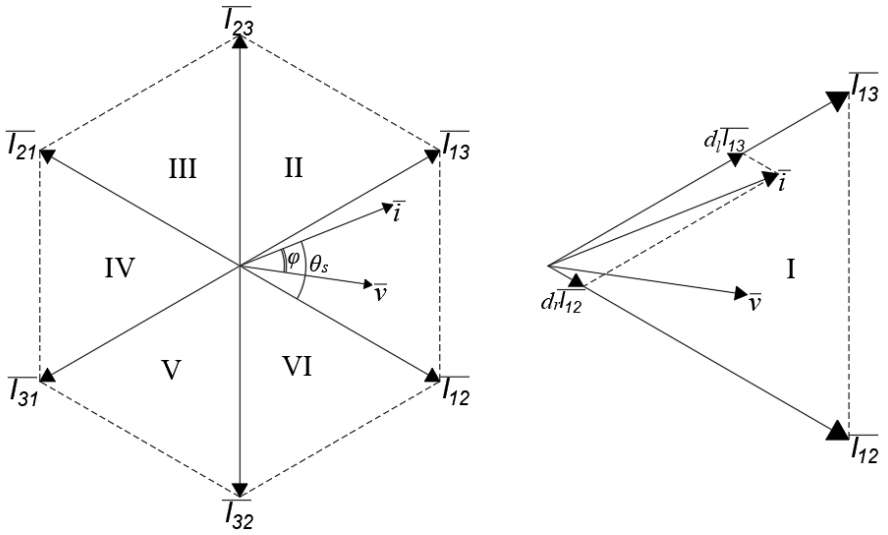

Figure 3.1: Space-vector modulation diagram: full hexagon (left), sector I (right)

freely selectable vector, representing additional degrees of freedom in the system, which can be tuned according to specific performance objectives.

The input voltage $\overline{v}$ and input current $\overline{i}$ space vectors (see Fig. 3.1) can be decomposed into components as

$$\begin{aligned} v_{i,k} &= \overline{v} \cdot \overline{\alpha}_k \\ i_{i,k} &= \overline{i} \cdot \overline{\alpha}_k \end{aligned} \tag{3.16}$$

where $k \in [1, 2, 3]$ denotes the input phase number. $\overline{\alpha}_k$ is defined as

$$\overline{\alpha}_k = e^{j\frac{2\pi}{3}(k-1)} \tag{3.17}$$

If the direction of the desired input current vector is expressed as a unity vector $\overline{\psi}_{ref}$, then the reference vector $\overline{m}_d$ can be obtained as

$$\overline{m}_d = \frac{2}{3}\frac{V_o^* \overline{\psi}_{ref}}{\overline{v} \cdot \overline{\psi}_{ref}} \tag{3.18}$$

The reference vector $\overline{m}_d$ has the same direction and magnitude as the vector $\overline{i}$ in SVM.

The strategy assumes the use of a symmetric carrier wave. The result of the modulation is the duty cycles for each output terminal separately, under the assumption that each output terminal is connected to each input phase only once per switching cycle.

The sequence of input phase connections is chosen freely.

Since at any moment each output terminal must be connected to an input phase, the sum of the duty cycles for each output terminal within one cycle equals 1:

$$m_{h,1} + m_{h,2} + m_{h,3} = 1 \tag{3.19}$$

where $m_{h,k}$ is the duty cycle of terminal $h \in [1, 2]$ connected to input phase k. Geometrically, the output terminal state can be represented as a point inside an equilateral triangle (Fig. 3.2a). In this representation, the duty cycles correspond to the lengths of the perpendiculars from the point to the sides of the triangle.

The states of both output terminals are determined by the positions of the initial point and the terminal point of the vector $\overline{m}_d$. If either point lies outside the triangle, the operational point cannot be reached for the given $\overline{m}_d$ and $\overline{m}_0$. The vector $\overline{m}_0$ determines the relative position of $\overline{m}_d$ within the triangle. The selection of $\overline{m}_0$ introduces additional degrees of freedom, and its proper choice can lead to a reduced number of commutations per cycle and improved input and output current distortion (Fig. 3.2b).

A reduced number of commutations can be achieved if the initial and/or terminal point of $\overline{m}_d$ is placed on a side or a vertex of the triangle. In this case, the corresponding input phase is not used for commutation.

If $\overline{m}_0$ is defined as shown in Fig. 3.2b, such that the initial point is equidistant from the three sides of the triangle and the vector points toward the center of $\overline{m}_d$, then the duty cycles of the output terminals can be calculated as

$$m_{h,k} = \frac{1}{3} + (-1)^{h-1} \frac{\overline{m}_d \cdot \overline{\alpha}_k}{2} + \overline{m}_0 \cdot \overline{\alpha}_k \tag{3.20}$$

The fact that DC-SVM generates duty cycles for each output terminal, rather than directly for specific line-to-line voltages, may represent a limitation in some cases. Additional computational steps are required either to determine the applied line-to-line voltages for a given $\overline{m}_0$ and phase order, or, conversely, to calculate the appropriate $\overline{m}_0$ and phase order required to obtain a desired line-to-line voltages at the output.

On the other hand, this formulation offers important advantages. Since the output terminals are controlled independently, the number of commutations per cycle can be

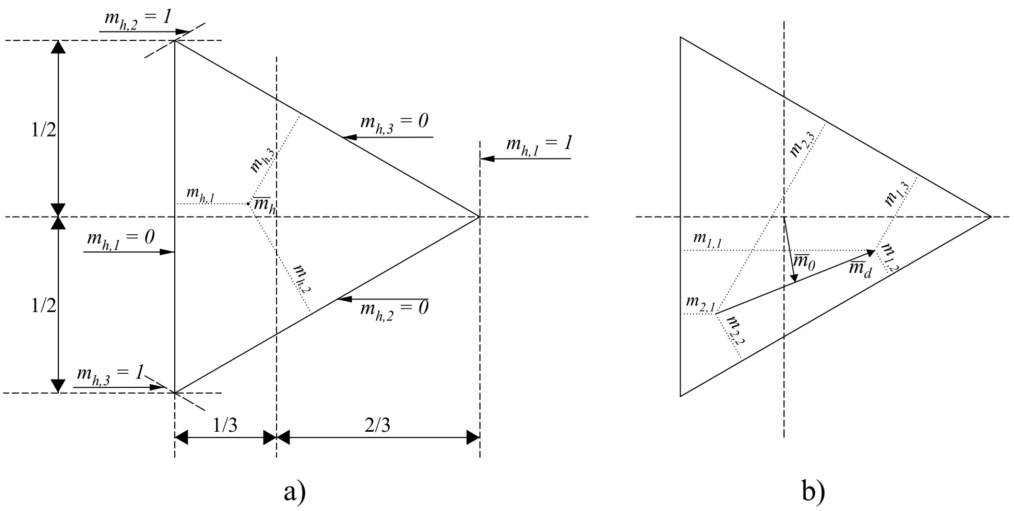

Figure 3.2: Geometrical representation of duty cycle space-vector modulation

managed in a more straightforward manner. Moreover, in certain operating conditions, this approach enables smooth transitions between switching patterns, as will be discussed in more detail later.

3.2 Modulation methods comparison

In this section, space-vector modulation is compared with other modulation methods employing different selections of active duty cycles under various operating conditions.

Conventional space-vector modulation does not provide freedom in selecting active duty cycles, in contrast to duty-cycle modulation or DC-SVM. In SVM, the active duty cycles are predefined for each sector. In DC-SVM, the selection of active duty cycles can be adjusted through an appropriate choice of $\overline{m}_0$.

Figure 3.3 compares the modulation methods presented in (3.7), (3.8), (3.9), (3.10), and (3.14). Each plot shows the dependence of the modulation index on the input angle. The blue area represents the feasible modulation indices for a given set of input line-to-line voltages and a specified displacement angle φ. Since the system is symmetric with a period of $\frac{\pi}{3}$, the presented results can be extended to the entire input voltage period. The green region highlights the voltage set applied for each input angle in SVM. Voltages above the figures indicate voltage vectors that were used for modulation. Absence of certain vector show that the corresponding duty cycles is set to 0. Feasible areas were

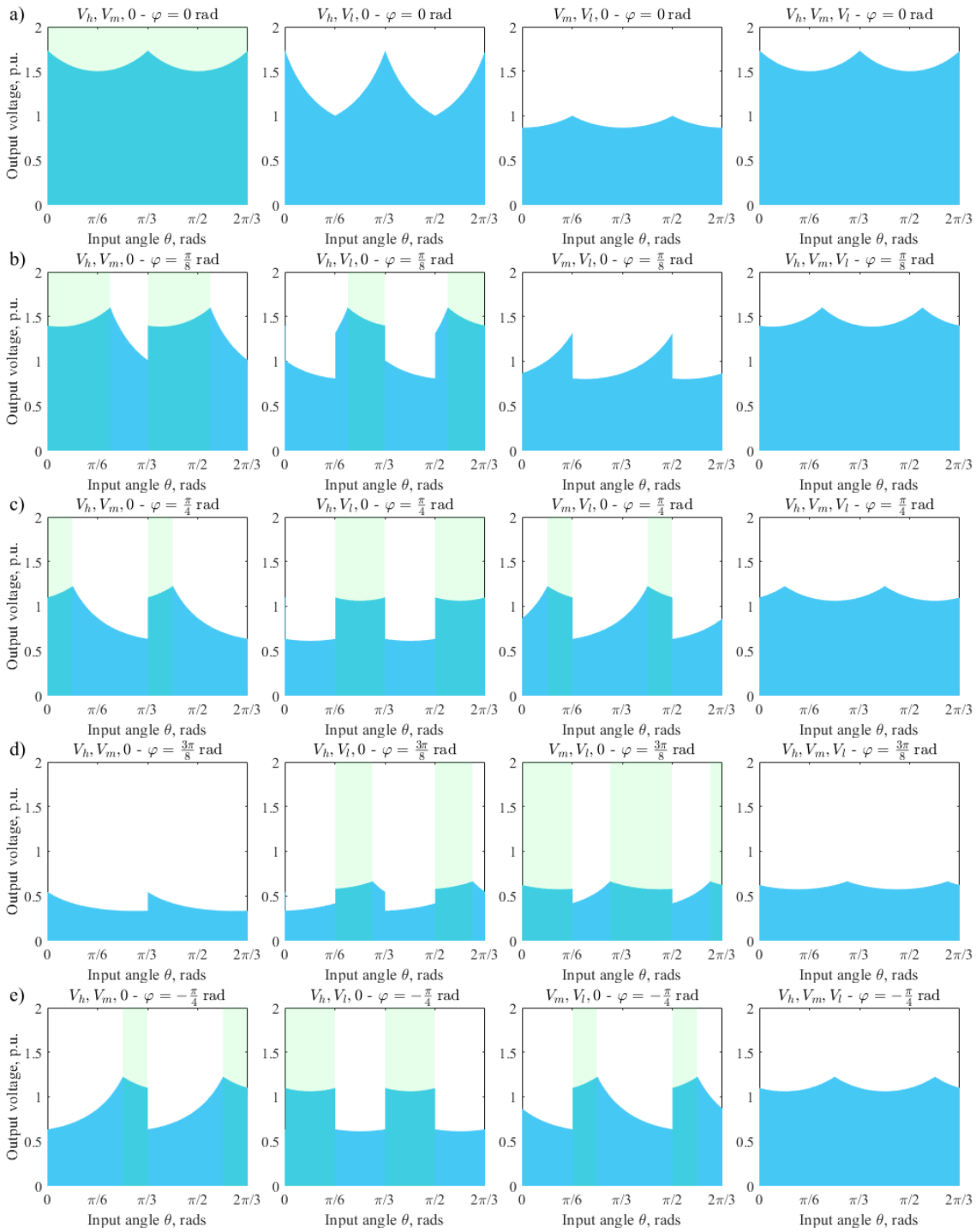

Figure 3.3: Output voltage to input angle relations under different operating conditions; the blue area indicates the achievable output voltage for given input voltages and power factor used for modulation; standard SVM is highlighted by the green area. a) $\varphi = 0$ rad; b) $\varphi = \frac{\pi}{8}$ rad; c) $\varphi = \frac{\pi}{4}$ rad; d) $\varphi = \frac{3\pi}{8}$ rad; e) $\varphi = -\frac{\pi}{4}$ rad.

determined by calculating duty cycles for each pair of input voltage-modulation index and checking whether condition (3.2) is fulfilled.

In the space-vector diagram (Fig. 3.1), $\overline{v}$ indicates the direction of the voltage vector. The projections of $\overline{v}$ onto the vectors $\overline{I_{xy}}$ correspond to the instantaneous line-to-line voltages associated with these vectors. Consequently, the closer the vector $\overline{I_{xy}}$ used in the modulation is to $\overline{v}$, the higher line-to-line voltage used in the modulation. For $\varphi = 0$ rad, SVM operation corresponds to the use of voltage set $V_h, V_m, 0$ in duty-cycle modulation.

When $\varphi \neq 0$, there exist input angle intervals for which the voltage set changes. For $|\varphi| \leq \frac{\pi}{6}$, switching occurs between the sets $V_h, V_m, 0$ and $V_h, V_l, 0$ (see Fig. 3.3b). For $\frac{\pi}{6} \leq |\varphi| \leq \frac{\pi}{3}$, the sets $V_h, V_m, 0$, $V_h, V_l, 0$, and $V_m, V_l, 0$ are used (see Fig. 3.3c and Fig. 3.3e). For $\frac{\pi}{3} \leq |\varphi| \leq \frac{\pi}{2}$, the sets $V_h, V_l, 0$ and $V_m, V_l, 0$ are applied (see Fig. 3.3d).

As shown in Fig. 3.3, SVM inherently selects the voltage sets that yield the highest feasible modulation index, which constitutes an important advantage of the method, as the maximization of the output voltage range is achieved automatically.

The feasible modulation index m_f as a function of φ is defined as

$$m_f \leq \frac{3}{2} cos(\varphi) \tag{3.21}$$

According to Fig. 3.3, the use of V_h, V_m, and V_l (without the 0 state) in the modulation enables the achievement of the maximum voltage range for any power factor. However, since three active duty cycles are involved, additional degrees of freedom must be properly managed to reach this maximum range. Certain operating points can be obtained through multiple combinations of active duty cycles. Figure 3.4 shows the admissible regions for different voltage sets with varying duty-cycle signs. The superscripts of the voltages in the legend indicate the sign of the associated duty cycle. It should be noted that V_h, V_m, and V_l are always positive as defined in (3.11); negative duty cycles indicate that the corresponding voltage is applied with inverted polarity. As a result, the full operational range can be achieved using V_h, V_m, and V_l only if at least one of the voltages is applied with inverted polarity. Certain operational points can be achieved using several sets of voltages (taking into account changing polarity). Low modulation index zone (shown with blue color) is achievable only if V_h is negative or V_m and V_l are

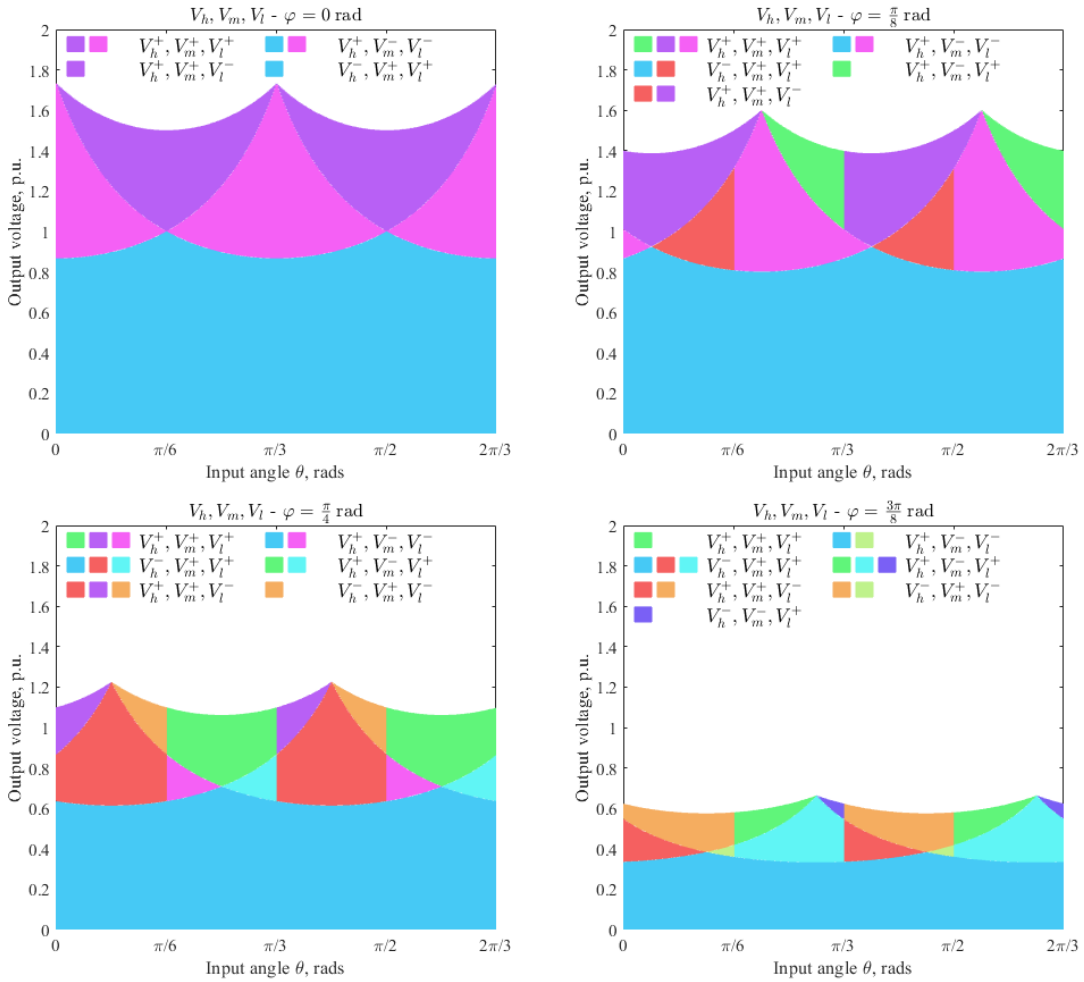

Figure 3.4: Output voltage to input angle maps for various power factors when V_h, V_m, and V_l are used for modulation. The signs of the corresponding duty cycles are taken into account.

negative. This approach has several disadvantages, such as increased switching losses and increased output current ripple, as will be demonstrated in more detail later.

Alternatively, the voltage sets $V_m, V_l, 0$ and V_h^+, V_m^+, V_l^+ can be used to achieve the same voltage range as standard SVM. The selection of the voltage set is governed by the fulfillment of condition (3.2). If this condition is not satisfied, the required modulation index cannot be achieved for a given operating point. This approach has been discussed in [5] for DC-SVM and in [7–9] for SVM. In [7], a modified SVM is presented in which switching between the voltage sets $V_m, V_l, 0$ and V_h, V_m, V_l is based on the magnitude and sector of the current vector. This method is applicable only for unity power factor and becomes unsuitable when the power factor deviates from unity. In [8, 9], operation at high modulation indices and power factors close to unity is considered, and compensation of the

displacement angle introduced by the input filter is addressed in [9]. The solution proposed in [5] accounts for power factor variation and remains applicable over the entire operating range.

3.3 Chapter Summary

In this chapter, modulation methods for the AC–DC matrix converter have been presented, focusing on the calculation of duty cycles. It has been shown that different modulation techniques can produce the same output results under the same operating conditions, while differing in the way the degrees of freedom in the duty-cycle calculation are used.

Duty-cycle modulation determines the duty cycles directly from weighted differences of the input phase voltages. In contrast, space-vector modulation represents the same quantities in a vector form, from which the duty cycles are then derived. The duty-cycle space-vector modulation method differs in that it provides the switching states of each terminal directly, rather than explicitly calculating the duty cycles.

Overall, the methods differ mainly in their formulation and in the way the switching sequence is generated, while leading to the same output quantities. The choice between them therefore depends on the preferred representation and implementation.

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Chapter 4:

Optimal Switching Pattern Selection

Several switching patterns have been proposed in the literature and compared with conventional approaches. However, most studies focus on a limited subset of patterns and do not demonstrate their global optimality. To address this limitation, the method presented in this chapter systematically evaluates the complete set of possible switching patterns and incorporates optimization within each pattern to further minimize the output current ripple. Importantly, switching losses are also taken into account, ensuring that ripple reduction is not achieved merely by selecting patterns with a higher number of commutations.

4.1 Pattern classification

Fig. 4.1 illustrates several examples of possible switching patterns. Each pattern is characterized by its commutation sequence during the first half of the PWM cycle, while the second half mirrors this sequence. For example, in the pattern $hm0$, the output is sequentially connected to the highest voltage level V_h, the medium voltage level V_m, and finally to the zero voltage level V_0. All patterns shown in Fig. 4.1 apply only V_h and V_m to the output; the lowest voltage level is omitted by setting the corresponding duty cycle d_l to zero. The signs of the $[h, m, l]$ patterns are specified using superscripts (for example, $[h^+, m^+, l^+]$) to distinguish patterns with different voltage polarities. Duty cycles d_I, d_{II}, d_{III}, d_{IV}, d_V in the figure represent duration of each state in the pattern.

For future reference, rst denotes a specific pattern in which the output terminals are sequentially connected to V_r, V_s, and V_t. The notation $[r, s, t]$ refers to a set of patterns that connect the output terminals to the specified voltages in any order and with any number of states.

Patterns such as $0h0m0$ and $0hm0h$ contain five switching states per half-cycle, whereas

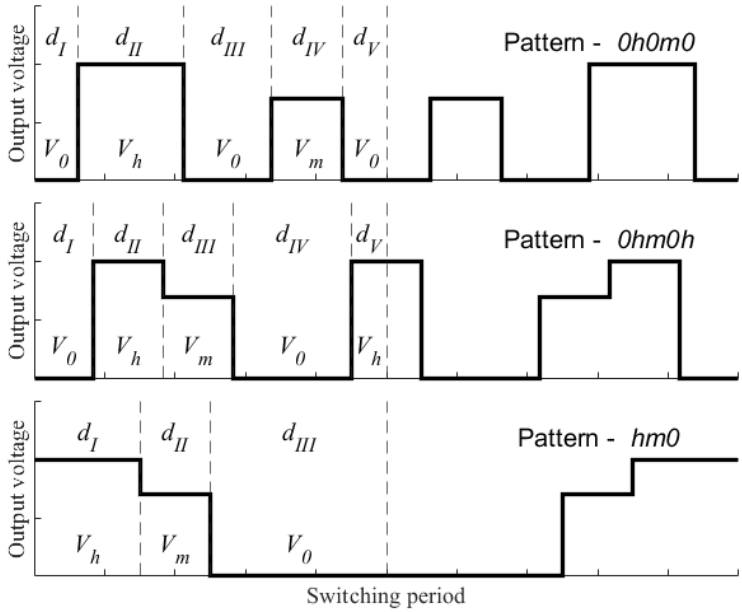


Figure 4.1: Examples of possible switching patterns

the $hm0$ pattern comprises only three. While an increased number of states per half-cycle leads to higher switching losses, it also introduces additional degrees of freedom for modulation. In particular, a pattern with three states per half-cycle has no degrees of freedom, whereas patterns with four and five states provide one and two degrees of freedom, respectively.

For example, in [1, 2], the distribution of the passive duty cycle in the pattern $0h0m0$ is investigated with the objective of minimizing the output current ripple I_{ripple}. Specifically, the duty cycles d_I, d_{III}, and d_V can be freely selected, provided that they are positive and satisfy the constraint $d_0 = d_I + d_{III} + d_V$. The optimized distribution is then compared with the standard case in which $d_{III} = 2d_I = 2d_V$, corresponding to equal zero-voltage intervals.

Similarly, the pattern $0hm0h$ also provides degrees of freedom in the selection of the duty cycles that constitute d_h and d_0. Figure 4.2 compares the optimized and non-optimized implementations of the $0hm0h$ pattern.

Table 4.1 shows existing research of pattern selection and optimization. Generally papers in Table 4.1 focus on a specific patterns and compares them to a standard solutions, showing superior performance of the proposed pattern. However, optimizing a specific pattern to minimize output current ripple does not necessarily yield the optimal trade-

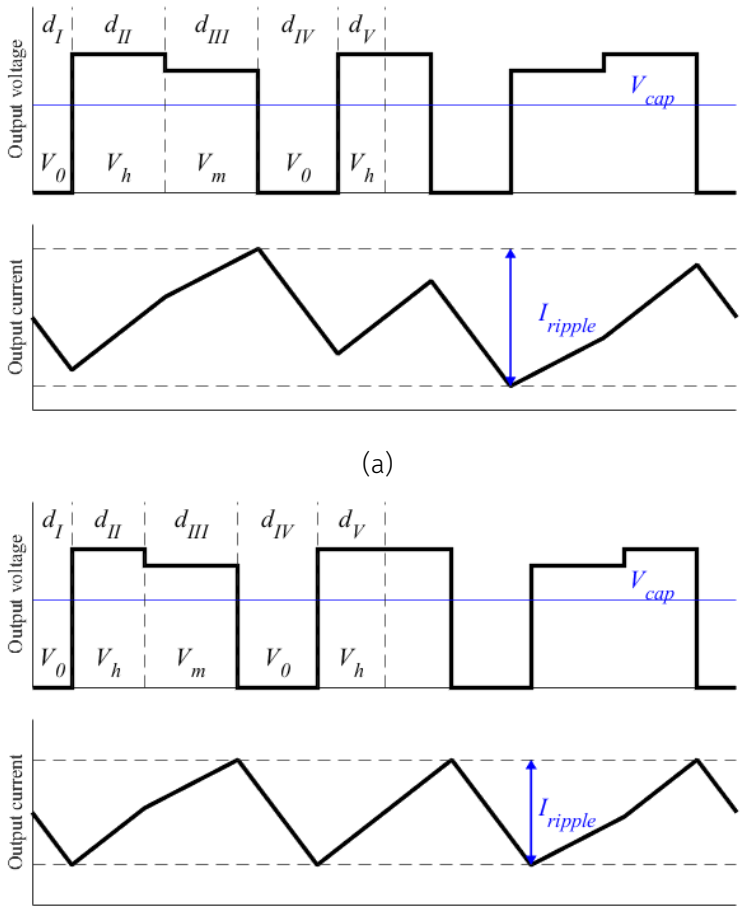


Figure 4.2: Comparison of standard (a) and optimized (b) pattern $0hm0h$

off between I_{ripple} and switching losses. This is because there is always the possibility that another pattern, when properly optimized, could result in a more favorable compromise. Therefore, a comprehensive analysis of multiple patterns is essential to identify those that offer the best balance between output current ripple and switching losses. To this end, this thesis investigates patterns comprising three, four, and five switching states per half-cycle.

Limits are chosen considering that three switching states per cycle is a minimum to provide necessary output voltage and sinusoidal input currents. Five switching states appear in some operation conditions if output terminals are connected to each input phase once per cycle (i.e., $0h0m0$).

The total number of distinct patterns with five switching states per half-cycle can be determined as follows. Assuming that the applied voltage must change in every state,

Table 4.1: Existing research on switching pattern selection and optimization

Reference	Switching Patterns	Key Characteristics
[3]	$m^+h^+l^+$ for higher modulation indexes and $m0l$ for lower modulation indexes	Achieves a smooth transition between patterns for all power factors using DC-SVM.
[4]	Three state $[h^+, m^+, l^+]$ patterns ($m^+h^+l^+$ for unity power factor)	Focuses exclusively on high modulation index operation.
[5]	$m^+h^+l^+h^+$ for unity power factor	Considers only high modulation index operation, with a focus on optimizing the states within the pattern.
[1]	$0h0m0$	Concentrates on the optimization of passive states within the pattern to minimize ripple.
[2]	$0hm$, $h0m$, $hm0$, $0hm0$	Optimizes the passive states for the $0hm0$ pattern to minimize output ripple.
[6]	$0h0m0$, $0h0m$, $0hm0$, $h0m0$, $0hm$, $h0m$, $hm0$	States that the $0h0m$ pattern minimizes total harmonic distortion (THD) of input current, $0hm$ maximizes efficiency, $hm0$ and $h0m0$ have lowest output current THD.
[7]	$m^+h^+l^+$ for higher modulation indexes and $lm0$ for lower modulation indexes	The proposed transition strategy between patterns is effective only for a unity power factor.

there are seven possible structural templates: $rsrst$, $rsrts$, $rstrs$, $rtsrs$, $rstsr$, $trsrs$, and $rsrtr$, where r, s, and t denote three different duty cycle selections. For any specific set of voltage levels (e.g., $[h, m, 0]$), the sequence (r, s, t) can be permuted in $3! = 6$ distinct ways (i.e., $0mh$, $0hm$, $m0h$, $mh0$, $h0m$, and $hm0$). Thus, for each template, there are 6 unique permutations, resulting in $7 \times 6 = 42$ possible patterns per voltage set. Since there are ten such combinations of voltage levels—namely $[h, m, 0]$, $[h, l, 0]$, $[m, l, 0]$ and 7 possible sets for $[h, m, l]$ depending on the duty cycles sign (excluding V_h^-, V_m^-, V_l^-) — the total number of patterns with five states per half-cycle is $10 \times 42 = 420$.

Similarly, patterns with four switching states have three structural templates: $rstr$, $rsrt$, $srtr$. Leading to $10 \times 6 \times 3 = 180$ patterns with four states per cycle. Total amount of patterns with three states is $10 \times 6 \times 1 = 60$.

The patterns discussed above contain only three unique states. For the patterns with four and five states per cycle it is possible to have all four distinct states $[h, m, l, 0]$. Five state patterns in this case have six structural patterns: $rstur$, $rstru$, $rsrtu$, $srtru$, $srtur$, $strur$. The sequence (r, s, t, u) can be permuted in $4! = 24$ distinct ways. Total amount of patterns is $6 \times 24 = 144$. Total amount of four state patterns is 24.

As a result total amount of patterns to consider is 828.

4.2 Optimization approach

Patterns with four and five states must be optimized in order to exploit the additional degrees of freedom they provide. Since manually determining the optimal duty-cycle distribution for each pattern is impractical, the problem is formulated as a constrained optimization. The cost function is defined as the maximum output current ripple over one switching period, while the independent variables are the duty cycles:

$$\underset{\boldsymbol{z_{opt}} \in [0,1]}{\text{minimize}} \quad I_{ripple,max}(\boldsymbol{z_{opt}}, m, L, T_s, \theta, pattern) \tag{4.1}$$

where $\boldsymbol{z_{opt}}$ is the vector of optimization variables and L is the output inductance.

The constraints depend on the specific pattern being optimized and are specified in the following subsections.

The quantity $I_{ripple,max}$ is defined as

$$I_{ripple,max} = \max_{1 \le k \le 2n_p} I_{out}(k) - \min_{1 \le k \le 2n_p} I_{out}(k) \tag{4.2}$$

where n_p is the number of states in the pattern within a half-cycle, and $I_{out}(k)$ denotes the output current value after state k.

The general equation describing the output current is

$$L \frac{dI_{out}}{dt} = V_o - V_{cap} \tag{4.3}$$

where V_o is the converter output voltage defined by (3.1), and V_{cap} is the output capacitor voltage.

After substituting (3.1) into (4.14), the output current after each state of a given pattern can be expressed as

$$I_{out}(k) = I_{init} + \frac{T_s}{L} \sum_{k=1}^{2n_p} \left(V_k d_k - V_{cap} |d_k| \right) \tag{4.4}$$

where I_{init} is the initial current value at the beginning of the switching cycle, d_k is the duty cycle applied during state k, and V_k is the line-to-line voltage at the output terminals during state k.

4.2.1 Five-state switching patterns with three distinct states

Five-state switching patterns with three distinct states can be divided into two groups. In the first group, two distinct states appear twice during the half-cycle: $rsrst$, $rsrts$, $rstrs$, $rtsrs$, $rstsr$, $trsrs$. In the second group, one distinct state appears three times during the half-cycle: $rsrtr$. An example of the first group is $0hm0h$, while an example of the second group is $0h0m0$. The formulation of constraints and the associated optimization problems differs for each group.

For patterns in which two distinct states appear twice during the half-cycle, the constraints are formulated as

$$\begin{aligned} \text{subject to} \quad & 0 \leq z_{opt}(1) \leq |d_{opt1}| \\ & 0 \leq z_{opt}(2) \leq |d_{opt2}| \end{aligned} \tag{4.5}$$

where d_{opt} denotes the duty cycles of the states that appear twice per half-cycle. For the pattern $0hm0h$, $d_{opt1} = d_0$ and $d_{opt2} = d_h$.

Assuming that d_{opt1} is applied at two states $k_{1,1}$ and $k_{1,2}$ ($1 \leq k_{1,1}, k_{1,2} \leq n_p$), the duty cycles at these states in the optimization problem are defined as

$$\begin{aligned} d_{k_{1,1}} &= d_{opt1} - \text{sign}(d_{opt1}) z_{opt}(1) \\ d_{k_{1,2}} &= \text{sign}(d_{opt1}) z_{opt}(1) \end{aligned} \tag{4.6}$$

Similarly, for d_{opt2} the corresponding duty cycles are defined as

$$\begin{aligned} d_{k_{2,1}} &= d_{opt2} - \text{sign}(d_{opt2}) z_{opt}(2) \\ d_{k_{2,2}} &= \text{sign}(d_{opt2}) z_{opt}(2) \end{aligned} \tag{4.7}$$

For the pattern $0hm0h$, d_h is applied in states II and V (see Fig. 4.1); therefore, $d_{II} = d_h - \text{sign}(d_h) z_{opt}(2)$ and $d_V = \text{sign}(d_h) z_{opt}(2)$.

For patterns in which one distinct state appears three times during the half-cycle, the constraints are formulated as

$$\begin{aligned} \text{subject to} \quad z_{opt}(1) &\geq 0 \\ z_{opt}(2) &\geq 0 \\ z_{opt}(1) + z_{opt}(2) &\leq |d_{opt1}| \end{aligned} \tag{4.8}$$

Assuming that d_{opt1} is applied at three states $k_{1,1}$, $k_{1,2}$, and $k_{1,3}$ ($1 \leq k_{1,1}, k_{1,2}, k_{1,3} \leq n_p$), the duty cycles at these states in the optimization problem are defined as

$$\begin{aligned} d_{k_{1,1}} &= d_{opt1} - \text{sign}(d_{opt1}) z_{opt}(1) - \text{sign}(d_{opt1}) z_{opt}(2) \\ d_{k_{1,2}} &= \text{sign}(d_{opt1}) z_{opt}(1) \\ d_{k_{1,3}} &= \text{sign}(d_{opt1}) z_{opt}(2) \end{aligned} \tag{4.9}$$

For the pattern $0h0m0$, d_0 is applied in states I, III, and V (see Fig. 4.1); therefore, $d_I = d_0 - \text{sign}(d_0) z_{opt}(1) - \text{sign}(d_0) z_{opt}(2)$, $d_{III} = \text{sign}(d_0) z_{opt}(1)$, and $d_V = \text{sign}(d_0) z_{opt}(2)$.

4.2.2 Four-state switching patterns with three distinct states

Four-state switching patterns with three distinct states have identical constraints and optimization problem formulation as five-state switching patterns with three distinct states in which two distinct states appear twice during the half-cycle. The only difference is the presence of only one repeating distinct state.

The constraints are defined as

$$\text{subject to} \quad 0 \leq z_{opt}(1) \leq |d_{opt1}| \tag{4.10}$$

Assuming that d_{opt1} is applied at two states $k_{1,1}$ and $k_{1,2}$ ($1 \leq k_{1,1}, k_{1,2} \leq n_p$), the duty cycles at these states for the optimization problem are defined as

$$\begin{aligned} d_{k_{1,1}} &= d_{opt1} - \text{sign}(d_{opt1}) z_{opt}(1) \\ d_{k_{1,2}} &= \text{sign}(d_{opt1}) z_{opt}(1) \end{aligned} \tag{4.11}$$

4.2.3 Five-state switching patterns with four distinct states

Patterns with four distinct states $(V_h, V_m, V_l, 0)$ have an additional degree of freedom compared to patterns with three distinct states (two active duty cycles). This degree of freedom can be used for pattern optimization to further decrease the output current ripple. At the same time, duty cycle calculation and pattern optimization are no longer separate steps, which significantly complicates the optimization procedure. In total, five-state switching patterns have two degrees of freedom: the first degree arises from the possibility to freely distribute one duty cycle between repeated states (as in the previous cases), and the second degree arises from the presence of three active duty cycles in the pattern.

Constraints are formulated as

$$\text{subject to} \quad -1 \leq z_{opt}(1) \leq 1 \tag{4.12a}$$

$$0 \leq z_{opt}(2) \leq |d_{opt1}| \tag{4.12b}$$

$$|d_1| + |d_2| + |d_3| < 1 \tag{4.12c}$$

where the duty cycles are calculated from (3.1) and (3.6) as

$$\begin{aligned} d_3 &= z_{opt}(1) \\ d_2 &= -\frac{(V_0^* - V_b d_3 - V_c d_3) sin(\theta_c + \varphi) + (V_a d_3 - V_b d_3) sin(\theta_a + \varphi)}{(V_a - V_b) sin(\theta_a + \varphi) + (V_c - V_b) sin(\theta_c + \varphi)} \\ d_1 &= \frac{(V_0^* - V_a d_3 - V_b d_3) sin(\theta_a + \varphi) + (V_b d_3 - V_c d_3) sin(\theta_c + \varphi)}{(V_a - V_b) sin(\theta_a + \varphi) + (V_c - V_b) sin(\theta_c + \varphi)} \end{aligned} \tag{4.13}$$

Unlike the previous cases, the limits (4.12a) and (4.12b) for z_{opt} cannot be directly enforced, as the duty cycle values change during the optimization process. Constraint (4.12c) is therefore added to ensure that $z_{opt}(1)$ does not violate condition (3.2).

Assuming that d_{opt1} is applied at two states $k_{1,1}$ and $k_{1,2}$ ($1 \leq k_{1,1}, k_{1,2} \leq n_p$), the duty cycles at these states for the optimization problem are defined as in (4.11). Condition (4.12a) can be verified only after the optimization process is completed, since d_{opt1} is not known a priori. If the condition is not fulfilled, the optimization result is discarded and the process is repeated with different initial conditions. In general, for this type of pattern, the optimization must be executed for each operating point with several hundred randomized initial conditions to avoid convergence to suboptimal values of z_{opt}.

4.2.4 Four state switching patterns with four distinct states

Four-state switching patterns with four distinct states require a simplified optimization process compared to the previous case. The pattern has one degree of freedom due to the presence of three active duty cycles. The optimization constraints are given in (4.12a) and (4.12c), and the duty cycles are calculated as in (4.13).

4.3 Pattern selection results

All patterns are optimized as needed and subsequently analyzed. Due to space limitations, the complete results for every pattern cannot be presented; instead, intermediate results are shown for selected patterns at unity power factor. Afterward, the final list of patterns and modulation schemes that yield optimal results is provided, along with a comparison to standard techniques.

For the following tests, the output current ripple is normalized as

$$I_{ripple,p.u.} = I_{ripple,max} \frac{L}{\sqrt{3} V_{mag} T_s} \tag{4.14}$$

to remove dependence on specific system parameters.

After optimization, the duty cycles within each switching cycle are distributed to minimize the output current ripple. Optimization must be performed for every combination of modulation index and input voltage angle.

4.3.1 Output current ripple variation within one input voltage period

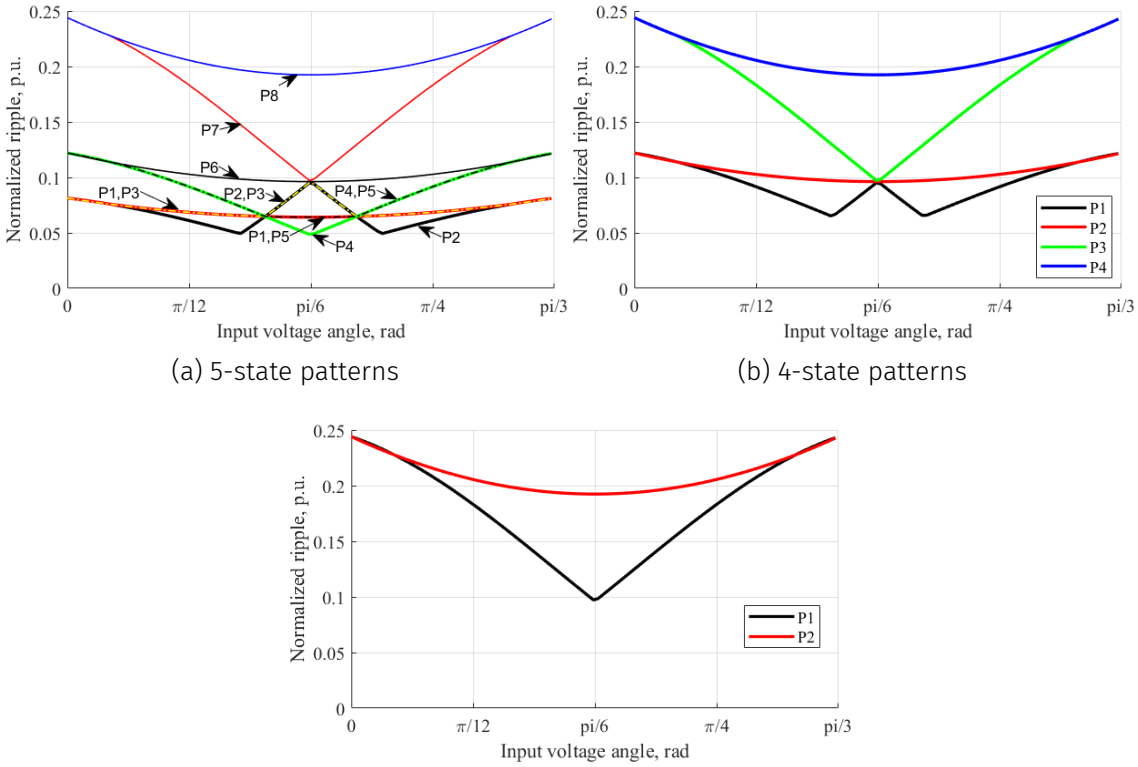
Assuming that the switching frequency is significantly higher than the grid frequency, the maximum output current ripple within a single PWM cycle is shown with respect to the input voltage angle. In this subsection, the maximum ripple is presented for the patterns $[h, m, 0]$, $[m, l, 0]$, and $[h^+, m^+, l^+]$ with different numbers of states. These patterns were selected for presentation because they are the most frequently referenced in the literature. Standard SVM converges to the use of $[h, m, 0]$ patterns for unity power factor (Fig. 3.3), whereas the pair $[m, l, 0]$ and $[h^+, m^+, l^+]$ is employed in [5, 7] to reduce output current ripple.

Fig. 4.3 shows the dependence of the maximum output current ripple for the optimized $[h, m, 0]$ patterns on θ, given a modulation index $m = 1$. $P1, P2 \dots P8$ in the figure are pattern groups. Each group contains of the several patterns that have identical ripple.

Patterns with 5, 4, and 3 states per half-cycle are presented separately. There are 42, 18, and 6 possible patterns for the 5-, 4-, and 3-state cases, respectively. As seen from the figures, the 5-state patterns can be grouped into 8 distinct groups, 4-state patterns into 4 groups, and 3-state patterns into 2 groups. The distribution of patterns within each group is shown in Table 4.2. The group number is determined by the average ripple over one grid period, with smaller group numbers corresponding to lower average ripple.

Because a symmetric carrier wave is used, mirrored patterns exhibit identical output ripple (e.g., $h0hm0$ and $0mh0h$) and therefore belong to the same group. The pattern $0h0m0$ optimized in [1] belongs to the group $P4^{5:states}_{[h,m,0]}$, whereas there exist groups $P1^{5:states}_{[h,m,0]}$, $P2^{5:states}_{[h,m,0]}$, and $P3^{5:states}_{[h,m,0]}$ that achieve lower ripple within one grid period. Similarly, the pattern $0hm0$ optimized in [2] belongs to the group $P2^{4:states}_{[h,m,0]}$.

Fig. 4.4 and Table 4.3 present the same type of results for the patterns $[m, l, 0]$ with 3 and 4 states per half-cycle. The modulation index is $m = 0.5$. Five-state patterns are omitted, as they are distributed across a larger number of groups compared to $[h, m, 0]$, making their presentation in a single figure impractical. Since the results in this section are intended to be intermediate, it was decided to exclude the 5-state patterns. The pattern $lm0$ proposed in [7] belongs to the group $P1^{3:states}_{[m,l,0]}$, which achieves the best ripple performance among the 3-state patterns at the given PWM frequency. In contrast, the pattern $m0l$ presented in [3] belongs to $P2^{3:states}_{[m,l,0]}$, resulting in suboptimal ripple.



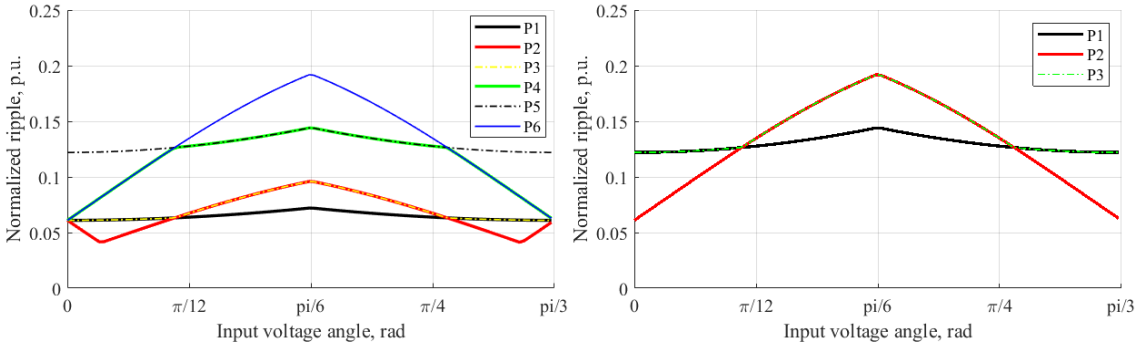
(a) 5-state patterns (b) 4-state patterns

(c) 3-state patterns

Figure 4.3: Normalized output current ripple for the optimized patterns $[h, m, 0]$ with different amount of states. Modulation index $m = 1$. $\varphi = 0$ rad.

Fig. 4.5 and Table 4.4 show the same type of results for the patterns $[h^+, m^+, l^+]$ with 3 and 4 states per half-cycle. Five-state patterns are omitted for the same reason as in the previous sections.

The papers [7], [4], and [3] propose the use of the pattern $m^+h^+l^+$ for higher modulation indexes; this pattern belongs to the group $P2^{3:states}_{[h^+,m^+,l^+]}$, which does not achieve optimal ripple given an identical PWM frequency. In [5], the pattern $m^+h^+l^+h^+$ is proposed,



(a) 4-state patterns (b) 3-state patterns

Figure 4.4: Normalized output current ripple for the optimized patterns $[m, l, 0]$ with different amount of states. Modulation index $m = 0.5$. $\varphi = 0$ rad.

Table 4.2: Pattern distribution within groups for the optimized patterns $[h, m, 0]$ with different amount of states

(a) 5-state patterns

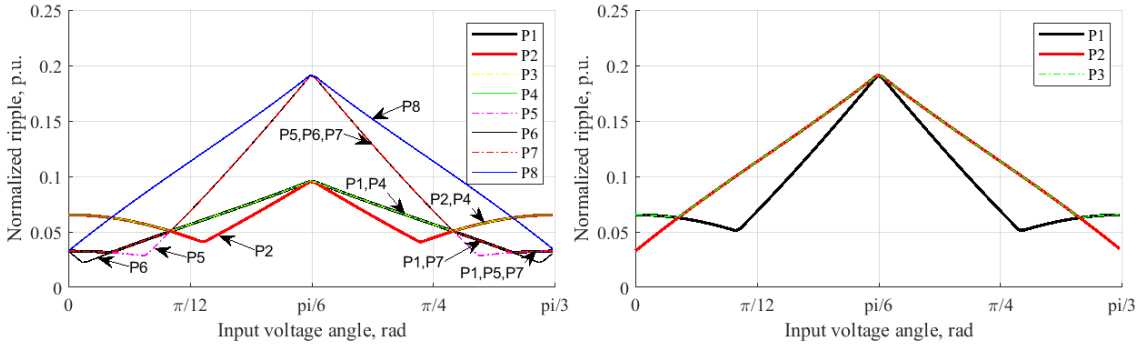
Group Number	Pattern
$P1^{5\ states}_{[h,m,0]}$	$0mh0h$, $0hm0h$ $h0mh0$, $h0hm0$
$P2^{5\ states}_{[h,m,0]}$	$m0h0h$, $h0h0m$
$P3^{5\ states}_{[h,m,0]}$	$hm0h0$, $mh0h0$ $0h0hm$, $0h0mh$
$P4^{5\ states}_{[h,m,0]}$	$m0h0m$, $0m0h0$ $0h0m0$, $h0m0h$
$P5^{5\ states}_{[h,m,0]}$	$m0mh0$, $m0hm0$ $0hm0m$, $0mh0m$
$P6^{5\ states}_{[h,m,0]}$	$hm0hm$, $hm0mh$, $mh0mh$ $mh0hm$, $0hmh0$ $0mhm0$, $h0mhm$, $hmh0h$ $h0hmh$, $mhm0h$
$P7^{5\ states}_{[h,m,0]}$	$0m0mh$, $0m0hm$, $h0m0m$ $m0m0h$, $mh0m0$ $hm0m0$, $m0mhm$, $m0hmh$ $hmh0m$, $mhm0m$
$P8^{5\ states}_{[h,m,0]}$	$hmhm0$, $mhmh0$ $0mhmh$, $0hmhm$

(b) 4-state patterns

Group Number	Patterns
$P1^{4\ states}_{[h,m,0]}$	$m0h0$, $0h0m$
$P2^{4\ states}_{[h,m,0]}$	$h0hm$, $mh0h$, $0mh0$ $0hm0$, $hm0h$, $h0mh$
$P3^{4\ states}_{[h,m,0]}$	$m0hm$, $mh0m$, $0m0h$ $m0mh$, $h0m0$, $hm0m$
$P4^{4\ states}_{[h,m,0]}$	$0mhm$, $mhm0$ $0hmh$, $hmh0$

(c) 3-state patterns

Group Number	Patterns
$P1^{3\ states}_{[h,m,0]}$	$m0h$, $h0m$
$P2^{3\ states}_{[h,m,0]}$	$0hm$, $mh0$ $hm0$, $0mh$



(a) 4-state patterns (b) 3-state patterns

Figure 4.5: Normalized output current ripple for the optimized patterns $[h^+, m^+, l^+]$ with different amount of states. Modulation index $m = 1$. $\varphi = 0$ rad.

which belongs to the group $P6^{4:states}_{[h^+,m^+,l^+]}$, far from the most optimal 4-state $[h^+, m^+, l^+]$ patterns.

Table 4.3: Pattern distribution within groups for the optimized patterns $[m, l, 0]$ with different amount of states

(a) 4-state patterns

Group Number	Patterns
$P1^{4\ states}_{[m,l,0]}$	$lm0m$, $m0ml$
$P2^{4\ states}_{[m,l,0]}$	$l0m0$, $0m0l$
$P3^{4\ states}_{[m,l,0]}$	$ml0m$, $m0lm$, $0lm0$, $0ml0$
$P4^{4\ states}_{[m,l,0]}$	$l0ml$, $lm0l$
$P5^{4\ states}_{[m,l,0]}$	$mlm0$, $lml0$, $0lml$, $0mlm$
$P6^{4\ states}_{[m,l,0]}$	$l0lm$, $0l0m$, $m0l0$, $ml0l$

(b) 3-state patterns

Group Number	Patterns
$P1^{3\ states}_{[m,l,0]}$	$lm0$, $0ml$
$P2^{3\ states}_{[m,l,0]}$	$m0l$, $l0m$
$P3^{3\ states}_{[m,l,0]}$	$ml0$, $0lm$

4.3.2 Output current ripple variation depending on modulation index

In this subsection, the variation of output current ripple with respect to the modulation index is analyzed. The output current ripple is evaluated for every modulation index and input voltage angle, and the maximum ripple is selected for each modulation index. For instance, patterns from the group $P8^{5:states}_{[h,m,0]}$ at modulation index $m = 1$ (Fig. 4.3a) exhibit the maximum ripple at angle $\theta = 0$, rad. In the same way, the maximum value is determined for all modulation indexes.

Table 4.4: Pattern distribution within groups for the optimized patterns $[h^+, m^+, l^+]$ with different amount of states

(a) 4-state patterns

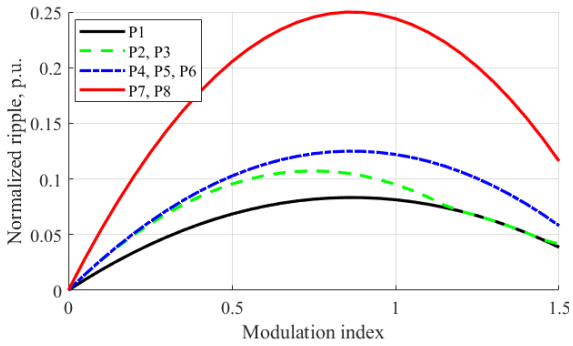
Group Number	Patterns
$P1^{4\ states}_{[h^+,m^+,l^+]}$	$lhml$, $lmhl$
$P2^{4\ states}_{[h^+,m^+,l^+]}$	$hlml$, $lmlh$
$P3^{4\ states}_{[h^+,m^+,l^+]}$	$mlhm$, $mhlm$
$P4^{4\ states}_{[h^+,m^+,l^+]}$	$mlmh$, $hmlm$
$P5^{4\ states}_{[h^+,m^+,l^+]}$	$lhlm$, $mlhl$
$P6^{4\ states}_{[h^+,m^+,l^+]}$	$hlhm$, $mhlh$
$P7^{4\ states}_{[h^+,m^+,l^+]}$	$hlmh$, $hmlh$
$P8^{4\ states}_{[h^+,m^+,l^+]}$	$mhml$, $hmhl$, $lmhm$, $lhmh$

(b) 3-state patterns

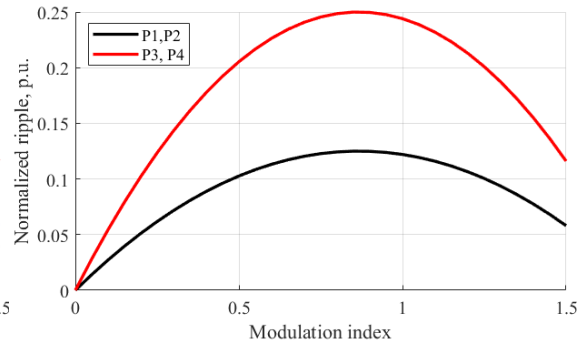
Group Number	Patterns
$P1^{3\ states}_{[h^+,m^+,l^+]}$	mlh, hlm
$P2^{3\ states}_{[h^+,m^+,l^+]}$	mhl, lhm
$P3^{3\ states}_{[h^+,m^+,l^+]}$	hml, lmh

Results in Fig. 4.6 show the maximum ripple for patterns $[h, m, 0]$ with 5, 4, and 3 states per half-cycle. The distribution of patterns in the groups is the same as in the previous subsection and is listed in Table 4.2. Fig. 4.7b presents the maximum output current ripple for patterns $[m, l, 0]$ with 4 and 3 states, while Fig. 4.8 shows the results for patterns $[h^+, m^+, l^+]$.

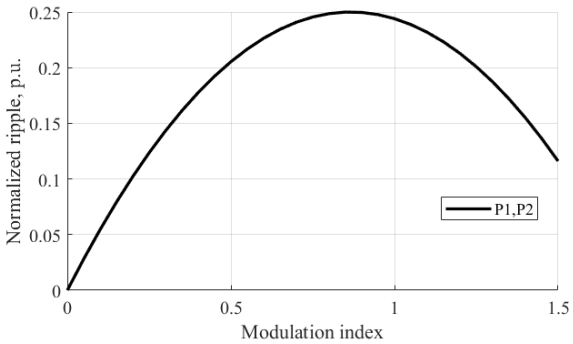
For unity power factor, the achievable modulation index range for patterns $[h, m, 0]$ is $m \in [0, 1.5]$ (see Fig. 3.3). For patterns $[m, l, 0]$, the modulation index range that can be achieved for any input voltage angle is $m \in [0, \frac{\sqrt{3}}{2}]$. For patterns $[h^+, m^+, l^+]$, the modulation index range for all input voltage angles is $m \in [1, 1.5]$. As discussed previously, patterns $[m, l, 0]$ and $[h^+, m^+, l^+]$ can be used together to cover the full modulation index range. For $m \in [\frac{\sqrt{3}}{2}, 1]$, the choice of pattern set ($[m, l, 0]$ or $[h^+, m^+, l^+]$) depends on the input voltage angle (see Fig. 3.3 and Fig. 3.4). These operating points are not illustrated in the presented figures and will be discussed in more detail later.



(a) 5-state patterns

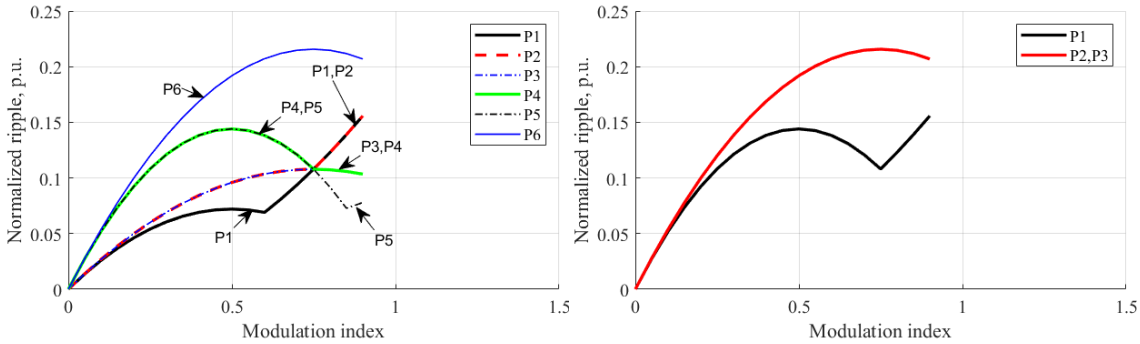


(b) 4-state patterns



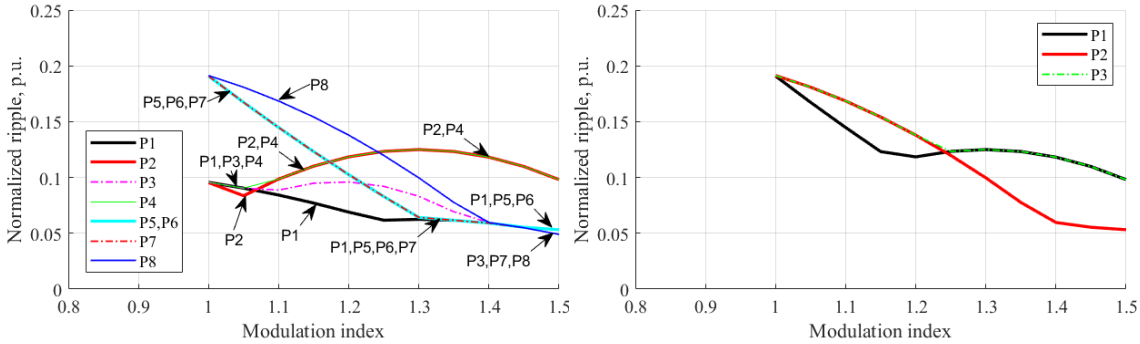
(c) 3-state patterns

Figure 4.6: Normalized output current ripple for the optimized patterns $[h, m, 0]$ with different amount of states with respect to modulation index. $\varphi = 0$ rad.



(a) 4-state patterns (b) 3-state patterns

Figure 4.7: Normalized output current ripple for the optimized patterns $[m, l, 0]$ with different amount of states with different amount of states with respect to modulation index



(a) 4-state patterns (b) 3-state patterns

Figure 4.8: Normalized output current ripple for the optimized patterns $[h^+, m^+, l^+]$ with different amount of states with different amount of states with respect to modulation index. $\varphi = 0$ rad.

4.3.3 Selection of the optimal patterns considering switching losses

The results presented in the previous subsections assume an identical switching frequency. As a consequence, patterns with a higher number of states exhibit lower output current ripple. For example, for patterns $[h, m, 0]$ at modulation index $m = 1$, the ratio of the maximum ripple for patterns from the groups $P1^{5:states}_{[h,m,0]}$, $P1^{4:states}_{[h,m,0]}$, and $P1^{3:states}_{[h,m,0]}$ is $1 : 1.5 : 3$.

At the same time, patterns with a larger number of states incur higher switching losses. Moreover, even patterns with the same number of states can result in different switching losses depending on the exact sequence of states within the pattern.

Therefore, switching losses must be taken into account in order to identify patterns that provide an optimal trade-off between output current ripple and switching losses. The principles of switching loss calculation are discussed in Subsection 2.3.1.

Below, several representative patterns are presented together with their corresponding terminal connections. The letters in the tables denote the input phase to which the output terminal is connected. Without loss of generality, it is assumed that the input phase voltages satisfy the condition

$$V_A > V_B > V_C. \tag{4.15}$$

Furthermore, $V_{AB} > V_{BC}$, such that $V_m = V_{AB}$ and $V_l = V_{BC}$. These assumptions are introduced to simplify the analysis; however, the results can be directly extended to other cases with identical conclusions.

The analysis is carried out assuming a constant output current. For clarity, only patterns with three states are considered in the following discussion.

Table 4.5 shows the terminal connections for the pattern $hm0$. It can be seen that terminal $t1$ (Fig. 2.1) is connected to phase A for the entire period. Phase A is selected for the zero state in order to reduce the number of commutations. Terminal $t2$ undergoes four commutations per period. The voltages involved during these commutations are V_{CB}, V_{BA}, V_{AB}, and V_{BC}.

Table 4.6 shows the terminal connections for the pattern $h0m$. Compared to $hm0$, the number of states is the same: terminal $t1$ remains connected to phase A for the entire period, and terminal $t2$ again undergoes four commutations. However, the voltages involved during the commutations are different, namely V_{CA}, V_{AB}, V_{BA}, and V_{AC}. Since V_{AC} is always higher than V_{BC} under the assumption (4.15), the switching losses associated with these commutations are higher. As a result, despite exhibiting identical ripple in Fig. 4.6c, the pattern $hm0$ is preferable due to lower switching losses.

Tables 4.7 and 4.8 show the terminal connections for the patterns $ml0$ and $m0l$, re-

Table 4.5: Switching pattern $hm0$ with corresponding terminal connections

	Switching Sequence				
Pattern $hm0$	h	m	0	m	h
Terminal $t1$	A	A	A	A	A
Terminal $t2$	C	B	A	B	C

Table 4.6: Switching pattern $h0m$ with corresponding terminal connections

	Switching Sequence				
Pattern $h0m$	h	0	m	0	h
Terminal $t1$	A	A	A	A	A
Terminal $t2$	C	A	B	A	C

Table 4.7: Switching pattern $ml0$ with corresponding terminal connections

	Switching Sequence				
Pattern $ml0$	m	l	0	l	m
Terminal $t1$	A	B	C	B	A
Terminal $t2$	B	C	C	C	B

Table 4.8: Switching pattern $m0l$ with corresponding terminal connections

	Switching Sequence				
Pattern $m0l$	m	0	l	0	m
Terminal $t1$	A	B	B	B	A
Terminal $t2$	B	B	C	B	B

spectively. The pattern $ml0$ results in six commutations per period, whereas $m0l$ requires only four. Consequently, $m0l$ exhibits lower switching losses; however, as shown in Fig. 4.7b, it produces higher output current ripple. The preferable pattern can therefore be identified by adjusting the switching frequency of one of the patterns such that both exhibit identical switching losses, and then comparing the resulting ripple, as discussed below.

The commutation voltages for the pattern $m0l$ are V_{AB}, V_{BC}, V_{BC}, and V_{BA}, which are identical to those of the pattern $hm0$. This results in identical switching losses for both patterns. According to Fig. 4.6c and Fig. 4.7b, the pattern $m0l$ exhibits lower output current ripple for modulation indexes $m \in \left[0, \frac{\sqrt{3}}{2}\right]$, making it the preferable option compared to $hm0$ within this modulation range.

Tables 4.9 and 4.10 show the terminal connections for the patterns $hl0$ and $h0l$. These patterns were not discussed in the previous sections. Unlike the patterns $[h, m, 0]$ and $[m, l, 0]$, for unity power factor the duty-cycle calculation for patterns $[h, l, 0]$ always leads to $d_l < 0$. As a result, the voltage applied to the output terminals must be inverted. The pattern $hl0$ results in six commutations per period, whereas the pattern $h0l$ has four commutations with voltages V_{AC}, V_{CB}, V_{BC}, and V_{CA}. This leads to higher switching losses compared to the pattern $hm0$, and, as the analysis shows, does not provide lower

Table 4.9: Switching pattern $hl0$ with corresponding terminal connections

	Switching Sequence				
Pattern $hl0$	h	l	0	l	h
Terminal $t1$	A	C	C	C	A
Terminal $t2$	C	B	C	B	C

Table 4.10: Switching pattern $h0l$ with corresponding terminal connections

	Switching Sequence				
Pattern $h0l$	h	0	l	0	h
Terminal $t1$	A	C	C	C	A
Terminal $t2$	C	C	B	C	C

Table 4.11: Switching pattern $m^+h^+l^+$ with corresponding terminal connections

	Switching Sequence				
Pattern $m^+h^+l^+$	m	h	l	h	m
Terminal $t1$	A	A	B	A	A
Terminal $t2$	B	C	C	C	B

Table 4.12: Switching pattern $m^+h^-l^+$ with corresponding terminal connections

	Switching Sequence				
Pattern $m^+h^-l^+$	m	h	l	h	m
Terminal $t1$	A	C	B	C	A
Terminal $t2$	B	A	C	A	B

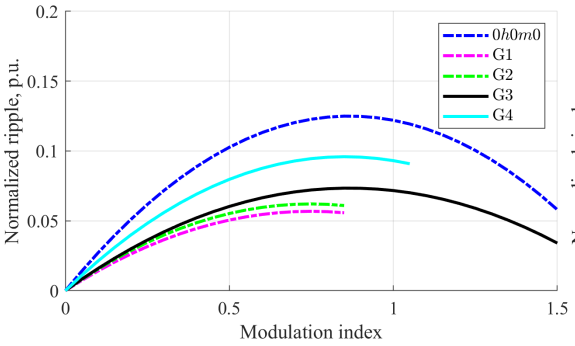
output current ripple.

A similar analysis can be carried out for the patterns $[h^+, m^+, l^+]$. The pattern $m^+l^+h^+$ has six commutations per period. The pattern $h^+m^+l^+$ has four commutations with voltages V_{CB}, V_{AC}, V_{CA}, and V_{BC}, while the pattern $m^+h^+l^+$ has four commutations with voltages V_{CB}, V_{AB}, V_{BA}, and V_{BC} (see Table 4.11). Due to the lower commutation voltages and consequently lower switching losses, the pattern $m^+h^+l^+$ is preferable. However, the minimum ripple shown in Fig. 4.8b depends on the modulation index, and therefore a definitive conclusion can only be drawn after accounting for switching losses. In general, the advantage of the patterns $[h^+, m^+, l^+]$ compared to patterns including the zero state lies in the commutation between line-to-line voltages that are closer to the capacitor voltage, which leads to reduced ripple.

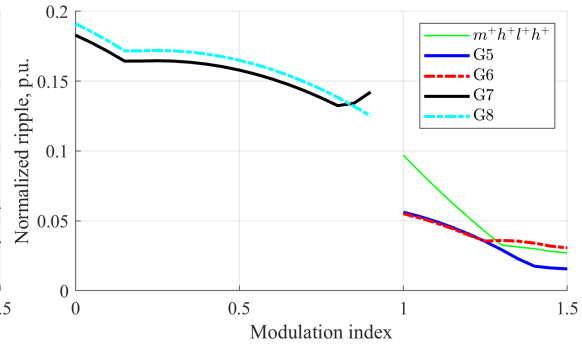
According to Fig. 3.3, patterns $[h, m, l]$ can be used to achieve the full voltage range. For unity power factor, Fig. 3.4 shows that patterns $[h^+, m^+, l^+]$ are applicable at higher modulation indexes, while patterns $[h^-, m^+, l^+]$ are applicable at lower modulation indexes. Table 4.12 shows the terminal connections for the pattern $m^+h^-l^+$. In this case, the sequence of states does not affect the result, as there are always eight commutations per period. Moreover, the necessity to apply a negative voltage inherently increases the output current ripple compared to patterns that include the zero state. As a result, the use of the pattern $[h^-, m^+, l^+]$ does not provide any advantage over the use of the pattern $[m, l, 0]$ for lower modulation indexes, as it is suggested in [3, 7].

4.3.3.1 Results for unity power factor

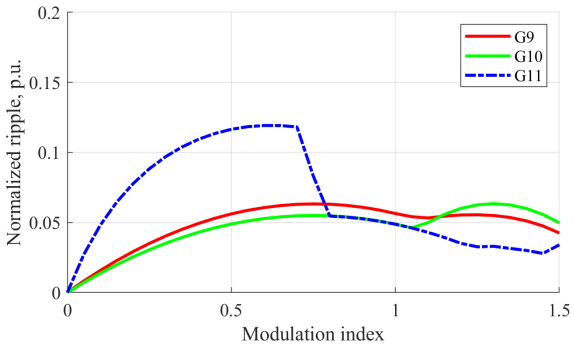
The switching losses for each pattern were calculated over one input voltage period. The switching frequency was then adjusted such that the total switching losses were equalized across all patterns. After this normalization, the output current ripple for each



(a) Patterns $[h, m, 0]$, $[h, l, 0]$, $[m, l, 0]$



(b) Patterns $[h, m, l]$



(c) Patterns $[h, m, l, 0]$

Figure 4.9: Patterns with the optimal ripple/losses relation. $\varphi = 0\,rad$

pattern was recalculated while accounting for the adjusted switching frequency.

Figure 4.9 presents a comparison of selected pattern groups $G1, G2 \ldots G11$ that yield the lowest output current ripple under equalized switching losses. Only a subset of all pattern groups is shown for clarity and conciseness; detailed information on all groups is provided in Table 4.13. The table shows pattens from which each group consists of and PWM scaling. The switching frequency scaling is referenced to the pattern $0h0m0$, and the switching frequencies of the remaining patterns are adjusted accordingly to achieve identical switching losses. This implies that, if the PWM frequency of pattern $0h0m0$ is f_{PWM}, then the PWM frequency of any other pattern should be scaled as $f_{\text{PWM}} \cdot k$ in order to achieve identical switching losses.

The plots for groups $G1_{[m,l,0]}$, $G2_{[m,l,0]}$, and $G4_{[m,l,0]}$ in Fig. 4.9a are truncated at higher modulation indices, since these indices cannot be achieved using the line-to-line voltages available in the respective patterns. In particular, groups $G1_{[m,l,0]}$ and $G2_{[m,l,0]}$ utilize the medium and lowest line-to-line voltages, while group $G4_{[h,l,0]}$ employs only the highest and lowest voltage levels.

Analysis of Fig. 4.9a indicates that, for systems requiring a wide output voltage range,

Table 4.13: Pattern groups that have optimal ripple/losses relation

Group Number	Pattern	f_{PWM} scaling k
-	$0h0m0$ [1]	1
$G1_{[m,l,0]}$	$0ml0m,\ m0lm0$	1.265
$G2_{[m,l,0]}$	$l0m0l$	1.702
	$m0lm,\ ml0m$	1.736
	$m0l$ [3], $l0m$	3.404
$G3_{[h,m,0]}$	$0hm0h,\ 0mh0h,\ h0hm0,\ h0mh0$	1.157
	$0mhm0,\ hm0mh$	1.702
	$0mh0,\ 0hm0,\ h0mh,\ hm0h$	1.727
	$0mh,\ hm0$	3.404
$G4_{[h,l,0]}$	$l0h0l,\ h0l0h$	1.371
	$h0lh,\ hl0h$	1.371
	$l0h,\ h0l$	2.742
-	$m^+h^+l^+h^+$ [5]	1.967
$G5_{[h^+,m^+,l^+]}$	$lhmhl$	1.702
	mhl [3, 4, 7],lhm	3.404
$G6_{[h^+,m^+,l^+]}$	$lmhl,\ lhml$	1.736
$G7_{[h^-,m^+,l^+]}$	$mhlmh,\ hmlhm$	0.607
$G8_{[h^-,m^+,l^+]}$	$mlhm,\ mlhm$	0.872
$G9_{[h,m,l,0]}$	$l0h0m,\ m0h0l$	-
$G10_{[h,m,l,0]}$	$hl0m,\ m0lh$	-
$G11_{[h,m,l,0]}$	$lhm0,\ 0mhl$	-

patterns from group $G3_{[h,m,0]}$ are generally suitable. If additional ripple reduction is desired at lower modulation indices, patterns from groups $G1_{[m,l,0]}$ and $G2_{[m,l,0]}$ can be employed. As the modulation index increases, a transition back to patterns from $G3_{[h,m,0]}$ is required. Patterns from group $G4_{[h,l,0]}$, and more generally those that simultaneously utilize the highest and lowest voltage levels, do not offer significant benefits.

Patterns from groups $G5_{[h^+,m^+,l^+]}$ and $G6_{[h^+,m^+,l^+]}$ exhibit improved performance compared to $G3_{[h,m,0]}$ at high modulation indices, as shown in Fig. 4.9b. In contrast, groups $G7_{[h^-,m^+,l^+]}$ and $G8_{[h^-,m^+,l^+]}$ do not provide advantages over other groups due to increased switching losses.

Figure 4.9c presents the results for patterns $[h, m, l, 0]$. At low modulation indices, the performance of groups $G9_{[h,m,l,0]}$ and $G10_{[h,m,l,0]}$ matches that of $G2_{[m,l,0]}$ and $G1_{[m,l,0]}$, respectively. At higher modulation indices, group $G11_{[h,m,l,0]}$ exhibits behavior similar to $G5_{[h^+,m^+,l^+]}$. The step observed in $G11_{[h,m,l,0]}$ at $m = 0.7$ can be explained by the fact that, after optimization, the duty cycles of patterns $[h, m, l, 0]$ may change sign due to the additional degree of freedom. Since switching losses depend on the signs of the duty cycles, accounting for switching losses can result in stepwise changes in the normalized ripple when a sign change occurs.

The selection of patterns with different numbers of switching states per cycle involves an inherent trade-off. Although the resulting output current ripple is similar across all cases, patterns with three states per cycle require no optimization but lead to a higher real-time control task frequency, assuming a fixed ratio between switching frequency and control task frequency. Patterns with a larger number of states per cycle require optimization; however, this optimization is computationally simple, as discussed later, and allows for a reduction in the real-time task frequency.

Some results from existing literature are included in Table 4.13 and Fig. 4.9 for comparison. Patterns proposed in [3, 4, 7] correspond to optimal solutions identified in this work, whereas patterns from [1, 5] are shown to be suboptimal.

As was previously mentioned the full operating range can be covered using patterns $[m, l, 0]$ and $[h^+, m^+, l^+]$. However, the region $[\frac{\sqrt{3}}{2}, , 1]$ can be covered by either pattern set depending on the input voltage angle. Analyzing ripple solely as a function of modulation index is therefore inconvenient when a given pattern does not cover all input voltage angles, and when multiple patterns can be used for the same modulation index. This issue becomes even more pronounced for non-unity power factor operation (see Fig. 3.3). For this reason, the next section presents ripple maps as functions of modulation index and input voltage angle.

4.3.4 Optimal modulation/pattern selection

In this section, standard modulation methods employing optimized patterns are compared with selected pattern sets that yield the lowest average output current ripple. The comparison is performed for several power factors. The standard modulation methods

considered include SVM and the combination of $[m, l, 0]$ and $[h^+, m^+, l^+]$ patterns, as proposed in [3, 4, 7].

The pattern sets are defined as collections of s patterns that are applied over the entire operational range of the converter, i.e., for all input voltage angles and modulation indices. The outcome of the optimization procedure therefore consists of (i) a specific set of patterns that minimizes the maximum output current ripple, and (ii) a corresponding map that indicates which pattern is used at each operating point. As a result, for a given modulation index, the selected pattern may vary within a single input-voltage period. This approach can introduce additional implementation challenges, which are discussed in detail later. The obtained results inherently depend on both the number of states allowed in the candidate patterns and the selected value of s.

Since the map may assign different patterns within a single input-voltage period, pattern transitions can occur during the mains cycle. To ensure a fair comparison under these conditions, the PWM frequency is assumed to be identical for all patterns.

The selection of pattern sets is performed by a brute-force check of all possible combinations of patterns, selecting sets of different sizes that lead to the lowest maximum ripple across the entire operating range.

The main disadvantage of patterns $[h, m, l, 0]$ lies in the complexity of their optimization process. While other patterns can be optimized algebraically with negligible computational effort, the use of patterns $[h, m, l, 0]$ requires solving an optimization problem numerically in real time or relying on lookup tables. Furthermore, the use of patterns $[h, m, l, 0]$ does not provide performance improvements compared to the other considered patterns. For these reasons, they are excluded from further analysis.

4.3.4.1 Issues related to pattern switching within an input voltage period

Switching between patterns within one input voltage period can lead to several issues related to dead time. The impact of dead time is pattern-dependent, since different patterns are affected differently by the insertion of dead time. As a result, the actual output voltage may deviate from its reference value.

Assuming that the output current is controlled by a PI regulator with the output voltage as the control variable, a constant mismatch between the reference and the actual

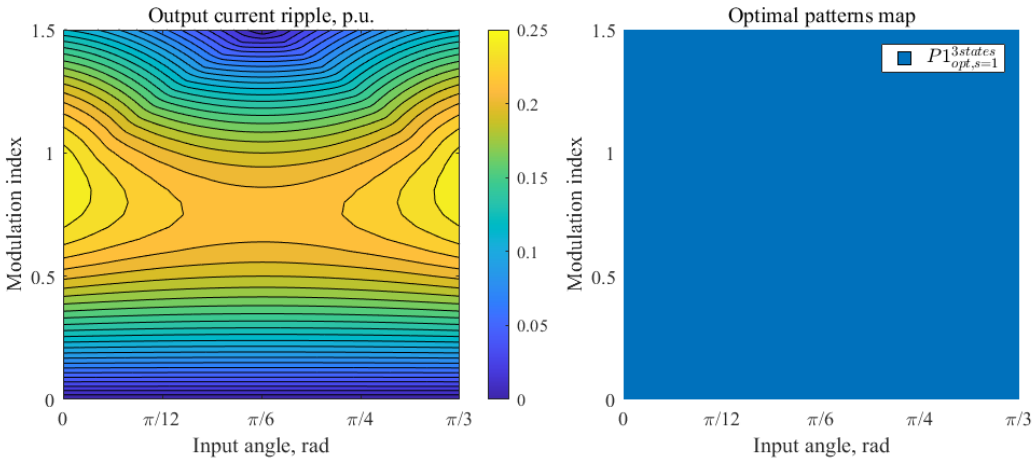


Figure 4.10: Map of normalized current ripple for optimized set of 3-state patterns $s = 1$ for unity power factor

voltage can be compensated when a fixed pattern is used. However, if the applied pattern changes within the input voltage period, the voltage mismatch also changes, which may result in current spikes caused by abrupt variations of the effective applied voltage.

Several approaches can be used to mitigate this issue: reduction of dead time if the switching devices allow it, dead-time compensation, or restriction to patterns that exhibit similar mismatch between the reference and the actual output voltage.

The influence of dead time also depends on the sequence of states within a pattern and can therefore be minor or more pronounced. For example, in the $hm0$ pattern, the h state is always prolonged by one dead-time interval, whereas the m state is not affected. In contrast, in the $m0l$ pattern both the m and l states are increased by one dead-time interval.

4.3.4.2 Comparison at unity power factor

According to Fig.3.3, in SVM, only $[h, m, 0]$ patterns are used at unity power factor. For unity power factor optimization for $s = 1$ coincides with SVM. The map of normalized output current ripple and patterns used for three state patterns are presented in Fig. 4.10. Patterns $P1^{3states}_{opt,s=1}$ can be selected from Table 4.14a. Alternatively, patterns that have the optimal ripple/losses relation are presented in Table 4.13 in the group $G3_{[h,m,0]}$.

DC-SVM map is presented in Fig. 4.11. It consists of two types of patterns: $[m, l, 0]$ and $[h^+, m^+, l^+]$. Compared to the SVM map (Fig. 4.10), the normalized current ripple is smaller. Moreover, optimization for $s = 2$ results in the usage of the same patterns.

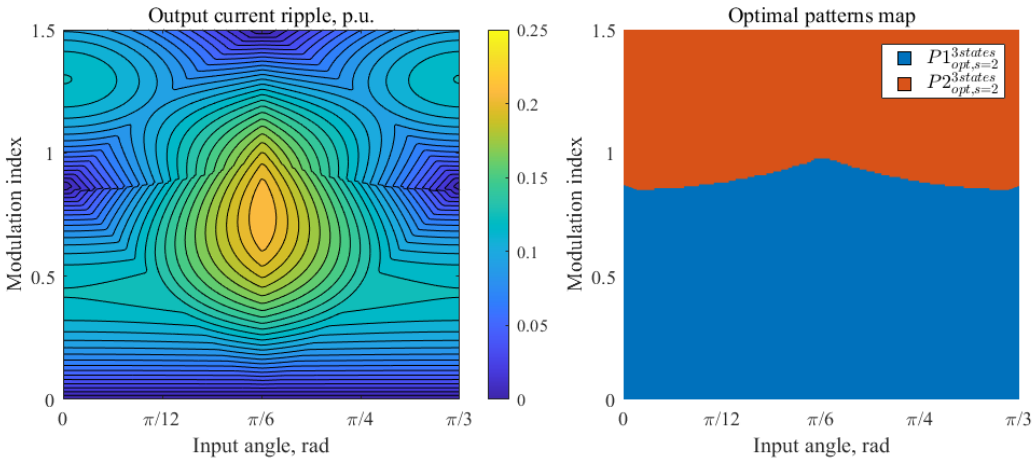


Figure 4.11: Map of normalized current ripple for optimized set of 3-state patterns $s = 2$ for unity power factor

Patterns $P1^{3states}_{opt,s=2}$ and $P2^{3states}_{opt,s=2}$ are shown in Table 4.14b.

Results for the optimization with $s = 3$ are presented in Fig. 4.12. Patterns $P1^{3states}_{opt,s=2}$ and $P2^{3states}_{opt,s=2}$ are the same as $P1^{3states}_{opt,s=3}$ and $P2^{3states}_{opt,s=3}$ (Table 4.14c). Pattern $P3^{3states}_{opt,s=3}$ covers zone of the maximum ripple in $s = 2$ optimization, allowing to further decrease current ripple.

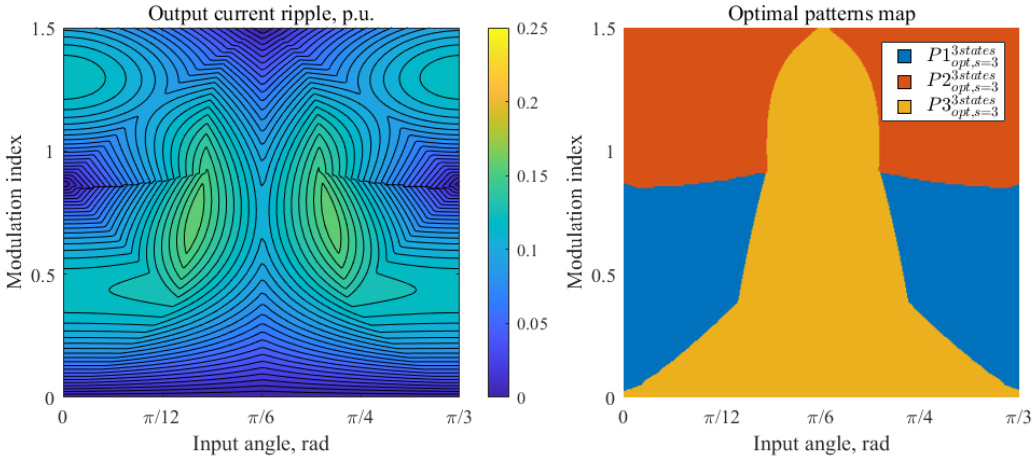


Figure 4.12: Map of normalized current ripple for optimized set of 3-state patterns $s = 3$ for unity power factor

Maps of the optimization sets for 4- and 5-state patterns at each power factor are presented in Appendix A. Due to the higher number of commutations per PWM cycle, these patterns inherently exhibit lower current ripple. However, patterns for $s = 1$ still match SVM, $s = 2$ match DC-SVM, and $s = 3$ introduces an additional pattern compared to $s = 2$.

Table 4.14: 3-state patterns used in optimized sets for different set number s for unity power factor

(a) $s = 1$

Group Number	Pattern
$P1^{3\ states}_{opt,s=1}$	$0mh$, $0hm$, $m0h$ $mh0$, $h0m$, $hm0$

(b) $s = 2$

Group Number	Patterns
$P1^{3\ states}_{opt,s=2}$	$0lm$, $l0m$, $m0l$, $ml0$
$P2^{3\ states}_{opt,s=2}$	lmh, lhm, mhl, hml

(c) $s = 3$

Group Number	Patterns
$P1^{3\ states}_{opt,s=3}$	$0lm$, $l0m$, $m0l$, $ml0$
$P2^{3\ states}_{opt,s=3}$	lmh, mlh, mhl, hml
$P3^{3\ states}_{opt,s=3}$	$m0h$, $h0m$

Fig. 4.13 shows the dependencies of maximum current ripple on modulation index, considering various s and numbers of states. The gray line corresponds to the lowest possible ripple if, for each operational point, the pattern with the least ripple is used. According to the figure, the benefits of using a higher number of patterns depend not only on the operational point but also on the number of states of the patterns employed. Maximum ripple values depending on modulation strategy and number of states are shown in Table 4.15.

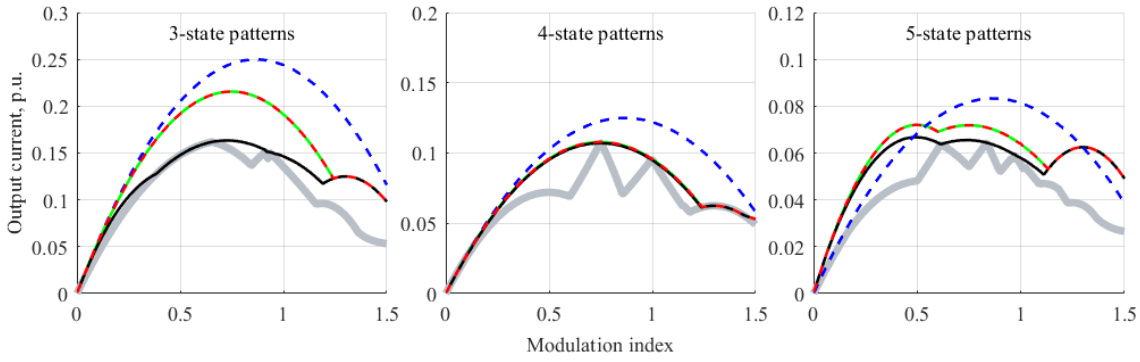


Figure 4.13: Dependencies of maximum current ripple on modulation index, considering various s and number of states (unity power factor): SVM (blue), $s = 2$ (green), $DC - SVM$ (red), $s = 3$ (black), $s =$ inf (gray)

Table 4.15: Maximum ripple for different modulation strategies and number of states at unity power factor

Modulation Used	Max Ripple 3 states	Max Ripple 4 states	Max Ripple 5 states
SVM	0.2499	0.125	0.0833
DC-SVM	0.2156	0.1078	0.072
Optimized $s = 1$	0.2499	0.125	0.0833
Optimized $s = 2$	0.2156	0.1078	0.072
Optimized $s = 3$	0.1634	0.1071	0.0667
Best	0.1618	0.1071	0.0643

4.3.4.3 Comparison at $\varphi = \frac{\pi}{8}$ rad

An identical analysis is performed for the power factor $\varphi = \frac{\pi}{8}$ rad.

For this power factor, SVM consists of two patterns, as shown in Fig. 4.14. Patterns that lead to the lowest ripple are presented in Table 4.16a. DC-SVM is similar to the unity power factor case, where $[m, l, 0]$ patterns are used for low modulation indices, and $[h, m, l]$ patterns for high modulation indices (Table 4.16b). The DC-SVM map is shown in Fig. 4.15.

The optimization set with $s = 2$ does not coincide with DC-SVM, even though the patterns consist of the same states (Table 4.16c). The corresponding map is shown in Fig. 4.16. The optimization set with $s = 3$ is presented in Fig. 4.17 (Table 4.16d).

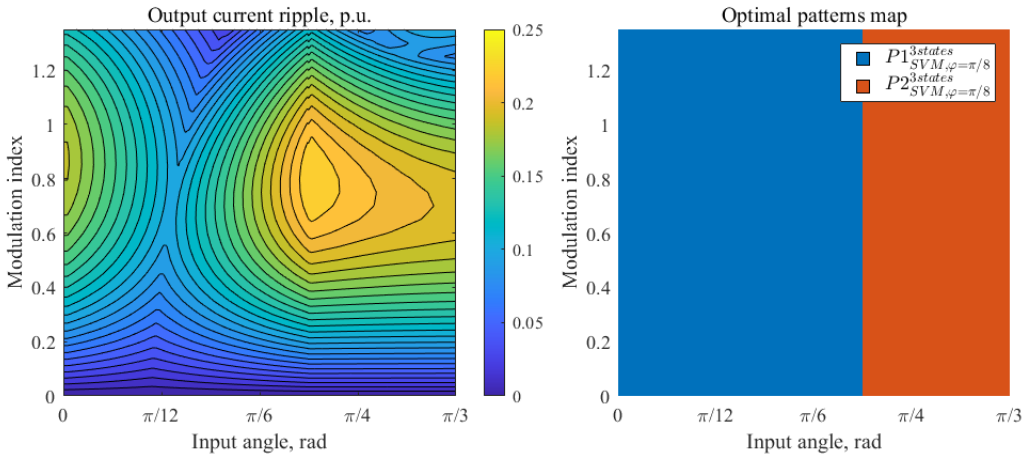


Figure 4.14: Map of normalized current ripple for SVM with 3-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

Fig. 4.18 shows the dependence of the maximum current ripple on the modulation index, considering various modulation strategies and numbers of states. The optimization performed in this thesis aims to minimize the maximum ripple across all operational

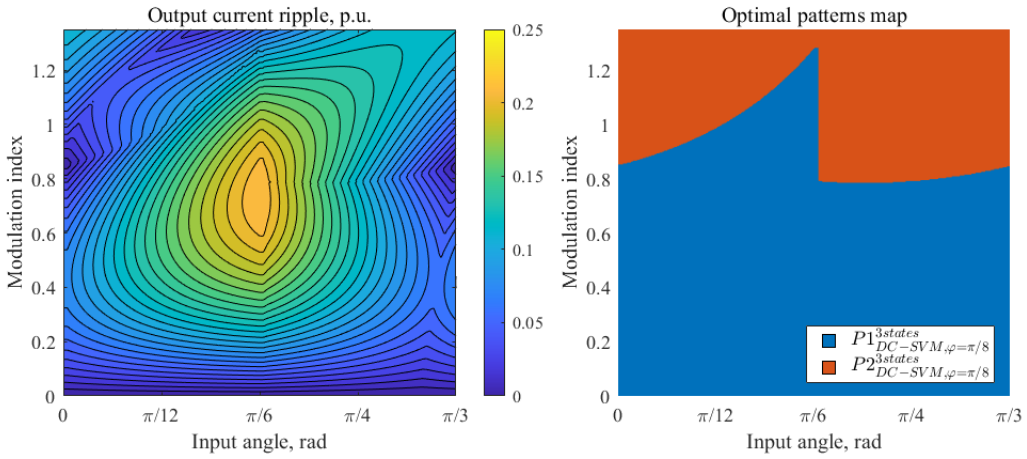


Figure 4.15: Map of normalized current ripple for DC-SVM with 3-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

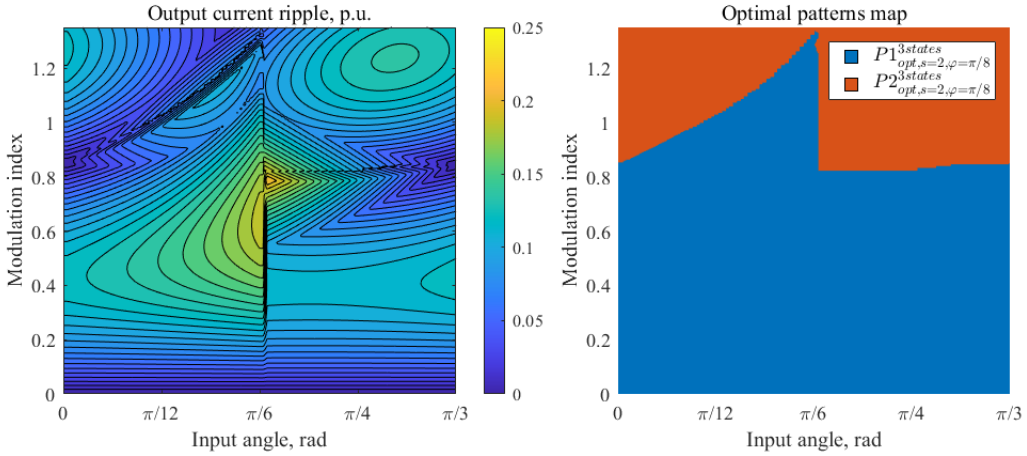


Figure 4.16: Map of normalized current ripple for optimized set of 3-state patterns $s = 2$ for power factor $\varphi = \frac{\pi}{8}\ rad$

points. Therefore, under certain operating conditions, an optimization with a higher number of patterns can locally result in a higher ripple compared to an optimization with fewer patterns. For example, the 5-state patterns optimized with $s = 3$ exhibit higher ripple in the low modulation index region compared to the $s = 2$ optimization.

For this power factor, the $s = 2$ optimization for 4- and 5-state patterns results in the selection of patterns identical to those used in SVM, although their distribution in the modulation index–input angle map is different.

Maximum ripple values depending on the modulation strategy and the number of states are shown in Table 4.17.

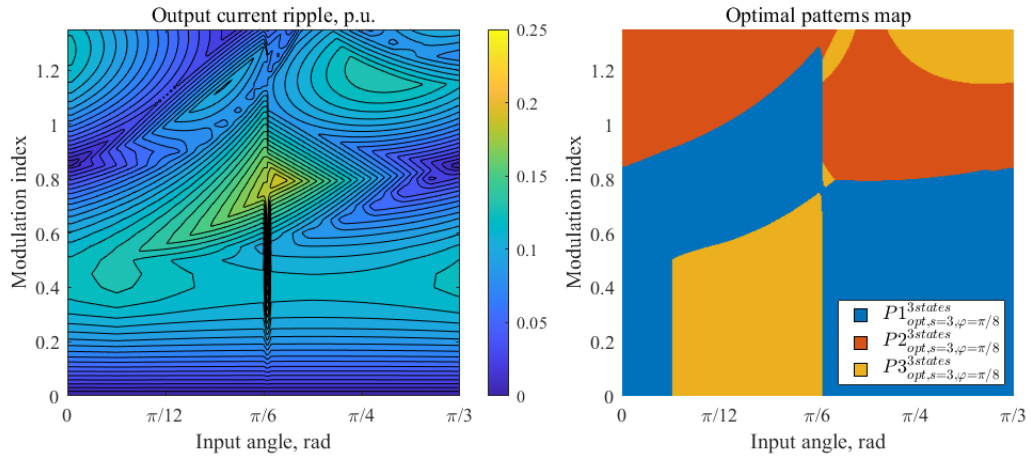


Figure 4.17: Map of normalized current ripple for optimized set of 3-state patterns $s = 3$ for power factor $\varphi = \frac{\pi}{8}\ rad$

Table 4.16: 3-state patterns used in different modulation strategies for power factor $\varphi = \frac{\pi}{8}\ rad$

(a) SVM

Group Number	Pattern
$P1^{3\ states}_{SVM,\varphi=\pi/8}$	$0mh$, $0hm$, $m0h$ $mh0$, $h0m$, $hm0$
$P2^{3\ states}_{SVM,\varphi=\pi/8}$	$lh0$, $0hl$

(b) $DC-SVM$

Group Number	Patterns
$P1^{3\ states}_{DC-SVM,\varphi=\pi/8}$	$m0l$, $l0m$
$P2^{3\ states}_{DC-SVM,\varphi=\pi/8}$	lhm, mhl

(c) $s = 2$

Group Number	Patterns
$P1^{3\ states}_{opt,s=2,\varphi=\pi/8}$	$0ml$, $lm0$
$P2^{3\ states}_{opt,s=2,\varphi=\pi/8}$	hlm, mlh

(d) $s = 3$

Group Number	Patterns
$P1^{3\ states}_{opt,s=3,\varphi=\pi/8}$	$lm0$, $0ml$
$P2^{3\ states}_{opt,s=3,\varphi=\pi/8}$	hlm, mlh
$P3^{3\ states}_{opt,s=3,\varphi=\pi/8}$	$lh0$, $0hl$

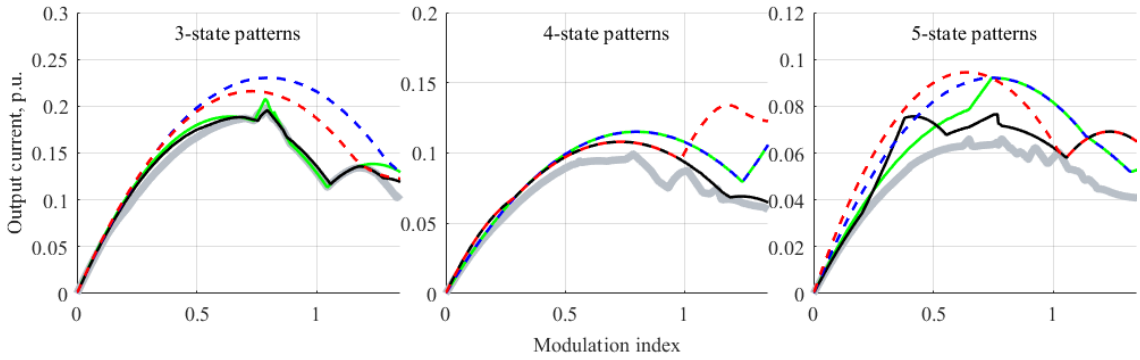


Figure 4.18: Dependencies of maximum current ripple on modulation index, considering various modulation strategies and number of states ($\varphi = \frac{\pi}{8}\ rad$): SVM (blue), $s = 2$ (green), $DC - SVM$ (red), $s = 3$ (black), $s = \inf$ (gray)

Table 4.17: Maximum ripple for different modulation strategies and number of states at power factor $\varphi = \frac{\pi}{8}\ rad$

Modulation Used	Max Ripple 3 states	Max Ripple 4 states	Max Ripple 5 states
SVM	0.2304	0.1152	0.0921
DC-SVM	0.2160	0.1342	0.0944
Optimized $s = 2$	0.2076	0.1152	0.0921
Optimized $s = 3$	0.1982	0.1080	0.0765
Best	0.1982	0.0992	0.0666

4.3.4.4 Comparison at $\varphi = \frac{\pi}{4}$ rad

An identical analysis is performed for a power factor of $\varphi = \frac{\pi}{4}$ rad. For this power factor, SVM consists of three patterns (Fig. 4.19). DC-SVM (Fig. 4.20) and the $s = 2$ optimization (Fig. 4.21) employ the same types of patterns, although the specific patterns differ, as shown in Table 4.18. The advantage of DC-SVM and SVM in this case is that the switching between patterns is always smooth. For SVM, this is due to the nearly identical voltage levels at the moments of switching between patterns, while for DC-SVM, the switch between the patterns happens naturally by smooth change duty cycles in each output terminal.

The dependence of maximum current ripple on the modulation index for this power factor is shown in Fig. 4.23, while the maximum ripple for each modulation strategy is summarized in Table 4.19.

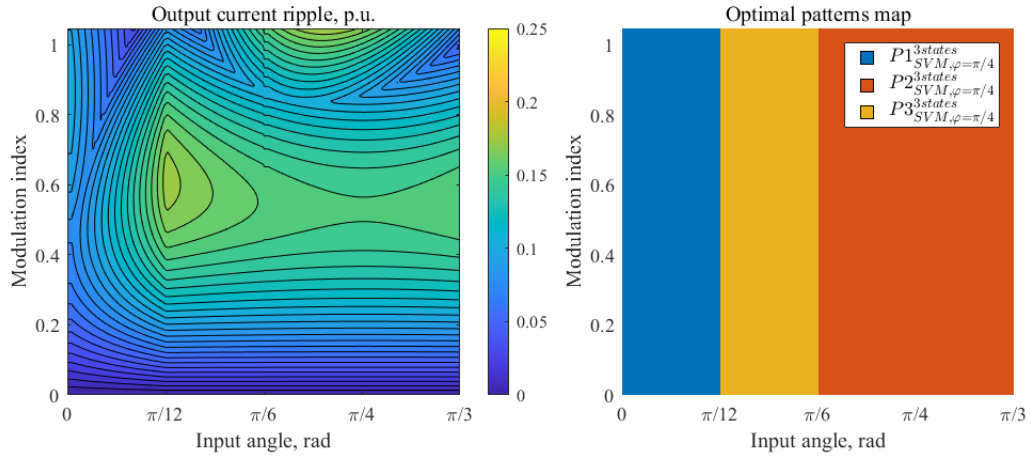


Figure 4.19: Map of normalized current ripple for SVM with 3-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

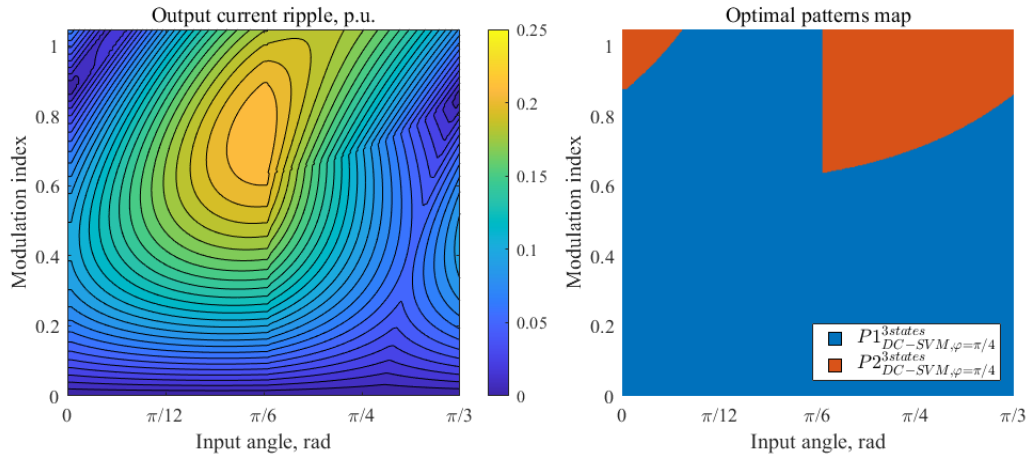


Figure 4.20: Map of normalized current ripple for DC-SVM with 3-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

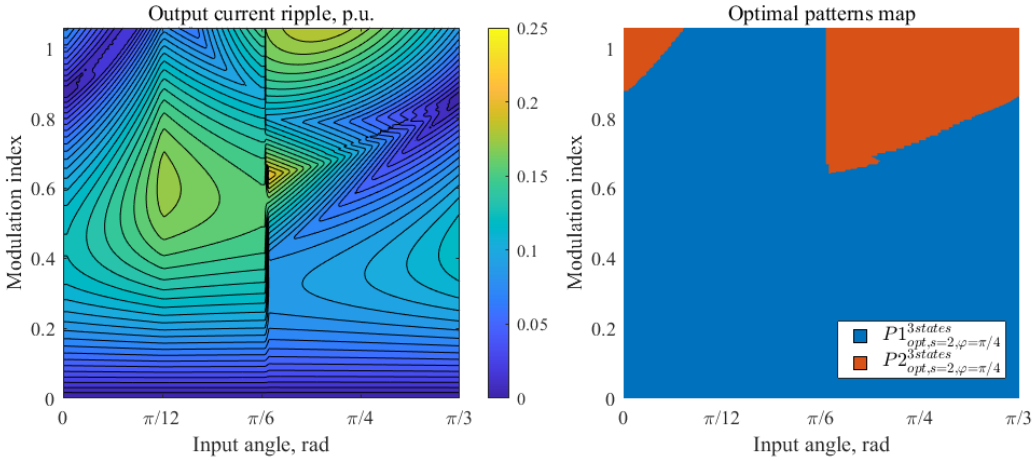


Figure 4.21: Map of normalized current ripple for optimized set of 3-state patterns $s = 2$ for power factor $\varphi = \frac{\pi}{4}\ rad$

4.4 Conclusions regarding modulation strategy and pattern selection

Based on the results presented in this chapter, several conclusions can be drawn. The most straightforward approach to achieving the full operational range at unity power factor is the use of SVM or duty-cycle modulation, as both methods cover the entire range using a single pattern type, namely $[h, m, 0]$. The corresponding optimal pattern selection is summarized in Table 4.13.

Compared to $[h, m, 0]$, the combined use of $[m, l, 0]$ and $[h^+, m^+, l^+]$ (set $s = 2$) yields lower ripple for the same level of losses at unity power factor. This combination is

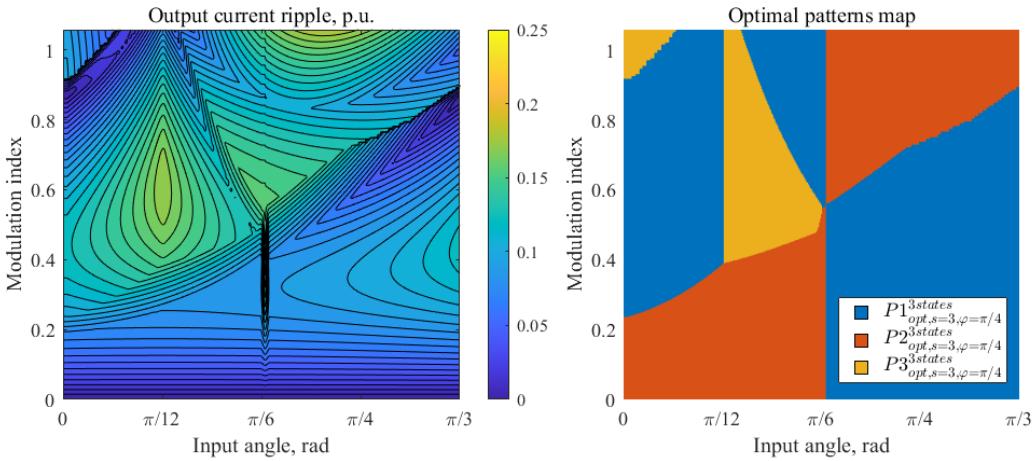


Figure 4.22: Map of normalized current ripple for optimized set of 3-state patterns $s = 3$ for power factor $\varphi = \frac{\pi}{4}\, rad$

Table 4.18: 3-state patterns used in different modulation strategies for power factor $\varphi = \frac{\pi}{4}\, rad$

(a) SVM

Group Number	Pattern
$P1^{3\ states}_{SVM,\varphi=\pi/4}$	$0mh$, $0hm$, $m0h$ $mh0$, $h0m$, $hm0$
$P2^{3\ states}_{SVM,\varphi=\pi/4}$	$lh0$, $0hl$
$P3^{3\ states}_{SVM,\varphi=\pi/4}$	$0ml$, $lm0$

(b) $DC-SVM$

Group Number	Patterns
$P1^{3\ states}_{DC-SVM,\varphi=\pi/4}$	$m0l$, $l0m$
$P2^{3\ states}_{DC-SVM,\varphi=\pi/4}$	lhm, mhl

(c) $s = 2$

Group Number	Patterns
$P1^{3\ states}_{s=2,\varphi=\pi/4}$	$0ml$, $lm0$
$P2^{3\ states}_{s=2,\varphi=\pi/4}$	hlm, mlh

(d) $s = 3$

Group Number	Patterns
$P1^{3\ states}_{opt,s=3,\varphi=\pi/4}$	$lm0$, $0ml$
$P2^{3\ states}_{opt,s=3,\varphi=\pi/4}$	$0hl$, $lh0$
$P3^{3\ states}_{opt,s=3,\varphi=\pi/4}$	$hm0$, $0mh$

Table 4.19: Maximum ripple for different modulation strategies and number of states at power factor $\varphi = \frac{\pi}{4}\, rad$

Modulation Used	Max Ripple 3 states	Max Ripple 4 states	Max Ripple 5 states
SVM	0.1800	0.1085	0.0791
DC-SVM	0.2164	0.1763	0.0926
Optimized $s = 2$	0.2038	0.1082	0.0925
Optimized $s = 3$	0.1800	0.1071	0.0767
Best	0.1800	0.1052	0.0720

most easily implemented using DC-SVM. Alternatively, duty-cycle modulation may also be employed, although it requires the incorporation of an appropriate switching strategy

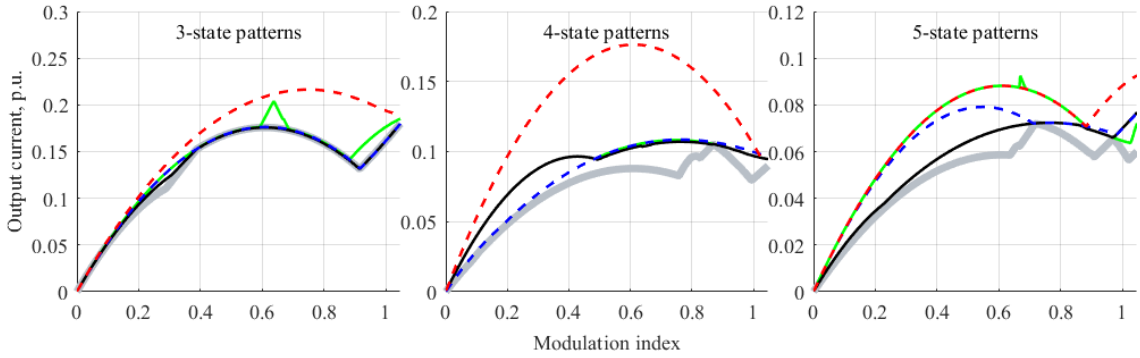


Figure 4.23: Dependencies of maximum current ripple on modulation index, considering various modulation strategies and number of states ($\varphi = \frac{\pi}{4}\ rad$): SVM (blue), $s = 2$ (green), $DC - SVM$ (red), $s = 3$ (black), $s = \text{inf}$ (gray)

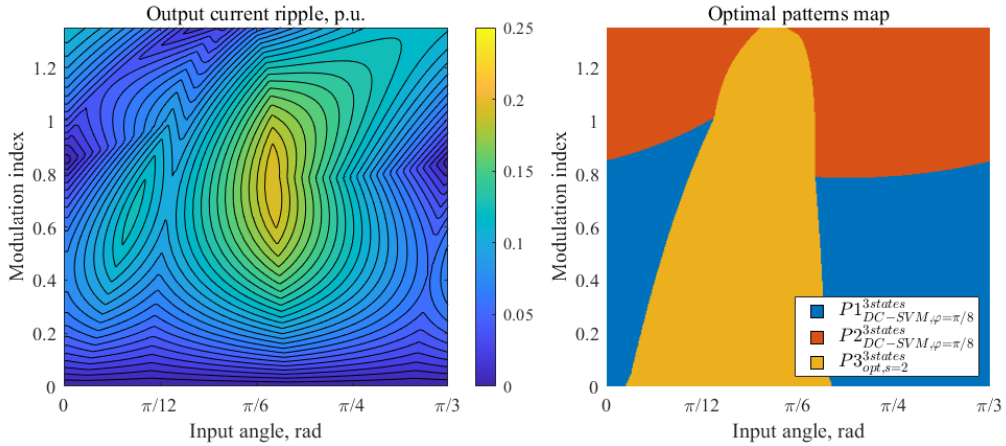


Figure 4.24: Map of normalized current ripple using optimized set $s = 3(\varphi = 0\ rad)$ for 3-state patterns at power factor $\varphi = \frac{\pi}{8}\ rad$

between patterns.

If additional ripple reduction is needed, the optimized strategy with $s = 3$ demonstrates superior performance. This improvement, however, comes at the cost of increased modulation complexity, as look-up tables (LUTs) are required to determine the appropriate pattern for each operating point. Alternatively, as will be shown in the experimental section, the optimal pattern can also be identified through calculations. The extent of improvement provided by the $s = 3$ strategy relative to the $s = 2$ combination depends on the number of states in the pattern. For example, Fig. 4.13 shows that the maximum ripple values obtained with $s = 2$ and $s = 3$ optimizations for 4 state patterns are nearly identical. This figure, however, does not reflect the average ripple, which is lower in the $s = 3$ case.

The choice of modulation strategy and pattern set is strongly influenced by the op-

erating conditions, including the expected power factor, modulation index, and available computational resources. Furthermore, the optimized strategies discussed in Section 4.3.4 are derived based on the criterion of minimizing the maximum ripple. The same optimization framework can be readily adapted to minimize the average ripple or to target a specific range of modulation indices.

In the previous section, optimal pattern sets were identified for $\varphi = [0, \frac{\pi}{8}, \frac{\pi}{4}]$ rad. For certain power factors, the optimizations for $s = 2$ and $s = 3$ result in different pattern sets. In practical applications, however, determining optimal patterns for every possible power factor and continuously switching between pattern sets as the power factor varies is not feasible. A practical alternative is to employ a sub-optimal pattern set that offers improved performance within a given power-factor range without requiring continuous pattern changes.

For $s = 2$, the use of $[m, l, 0]$ and $[h^+, m^+, l^+]$ represents a suitable compromise, as it provides relatively low ripple and an optimal ripple-to-loss ratio. At low power factors, conventional SVM approaches the ripple performance of DC-SVM and may even yield superior results as the power factor further decreases.

For $s = 3$, one viable option is to employ the pattern set optimized for unity power factor (Table 4.14c). This set consists of $[m, l, 0]$ and $[h^+, m^+, l^+]$ patterns (same as for $s = 2$), augmented by the $h0m$ pattern to reduce the peak ripple value. Among the patterns used in combination with $s = 2$ for $\varphi = \frac{\pi}{8}$ rad, the $h0m$ pattern results in the lowest ripple, as illustrated in Fig. 4.24.

4.5 Calculation of the optimized patterns algebraically

Once the patterns that provide the best trade-off between output current ripple and switching losses have been identified, it is convenient to calculate the duty cycles algebraically for those specific patterns. This approach is preferred as it avoids the need for numerical optimization in real time.

One of the optimized and subsequently experimentally tested patterns in this thesis is $0hm0h$. Nonetheless, the optimization method presented below is applicable to any other pattern.

Fig. 4.2 shows the output voltage and current waveforms without and with the optimization applied, respectively. The duty cycles d_h, d_m, and d_0 are calculated as described in the previous sections. To minimize the output current ripple, the duty cycle d_h must be appropriately distributed between d_{II} and d_V, while d_0 must be distributed between d_I and d_{IV}.

The method without optimization assigns equal pulse widths to the corresponding voltages. Thus, the duty cycles d_I through d_V are calculated as

$$\begin{aligned} d_{IV} &= 2d_I = 2d_0/3, \\ d_{II} &= 2d_V = 2d_h/3, \\ d_{III} &= d_m, \end{aligned} \tag{4.16}$$

The optimization is performed by equalizing I_{ripple} during each rising and falling period of the current waveform. The specific optimization conditions depend on the relationship between V_m and V_{cap}, and can be derived as follows:

$$\begin{aligned} &\text{If } V_m > V_{cap}: \\ &\quad d_{IV} = 2d_I = 2d_0/3, \\ &\quad d_V = \frac{d_{IV} V_{cap}}{2(V_h - V_{cap})}, \\ &\quad d_{II} = d_h - d_V, \\ &\quad d_{III} = d_m, \\ &\text{If } V_m \leq V_{cap}: \\ &\quad d_{II} = 2d_V = 2d_h/3, \\ &\quad d_I = \frac{d_{II}(V_h - V_{cap})}{2V_{cap}}, \\ &\quad d_{IV} = d_0 - d_I, \\ &\quad d_{III} = d_m, \end{aligned} \tag{4.17}$$

As observed, the computational overhead introduced by this optimization is negligible, indicating that it can be employed in real-time systems without adverse effects. In the following section, the presented approach is validated experimentally.

4.6 Experimental results

The section presents description of the experimental setup and experimental results that prove validity of theoretical findings regarding pattern optimization and pattern selection.

4.6.1 Experimental setup

Scheme of the experimental setup is presented in Fig. 4.25. A power supply is used to reduce the three-phase input voltage amplitude. An input filter is employed to reduce input current distortion, improve power quality, and to avoid significant voltage variations during the PWM period. The uCube control platform collects information about input voltages, output current, and capacitor voltage, and generates control pulses for the AC-DC matrix converter.

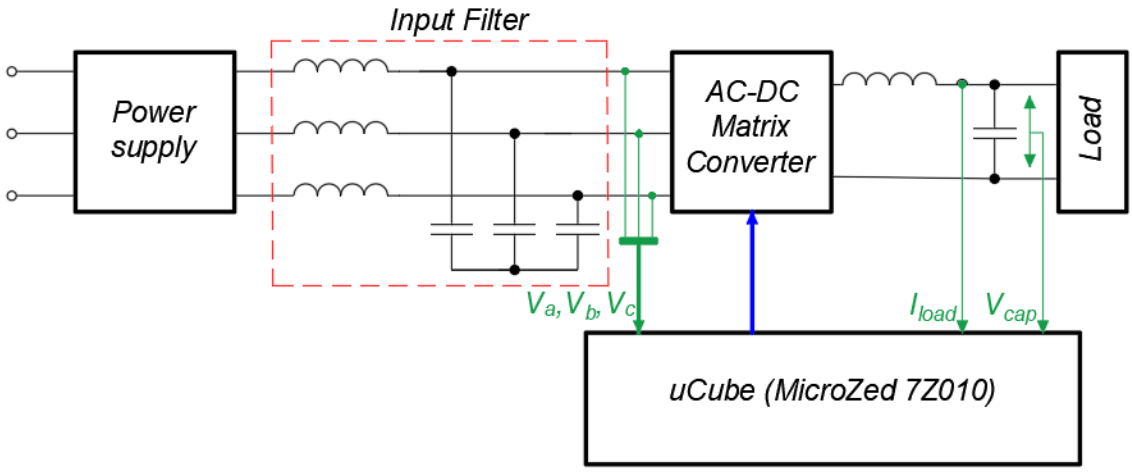


Figure 4.25: Experimental setup scheme

The power supply is a National Instruments NHR 9410 bidirectional unit (Fig. 4.26). In this work, it is used to reduce the input voltage amplitude to ensure safe experimental conditions. The results, however, are equally valid for any other input voltage amplitude.

The control platform is based on the MicroZed 7Z010 evaluation board (Fig. 4.27). The Zynq 7010 chip is a System on a Chip (SoC) consisting of two parts: PS (Processing System), which is an ARM processor executing the real-time control algorithm, and PL (Programmable Logic), which is an FPGA handling the modulator, the "4-step commutation" required for matrix converter operation as discussed previously, signal acquisition,

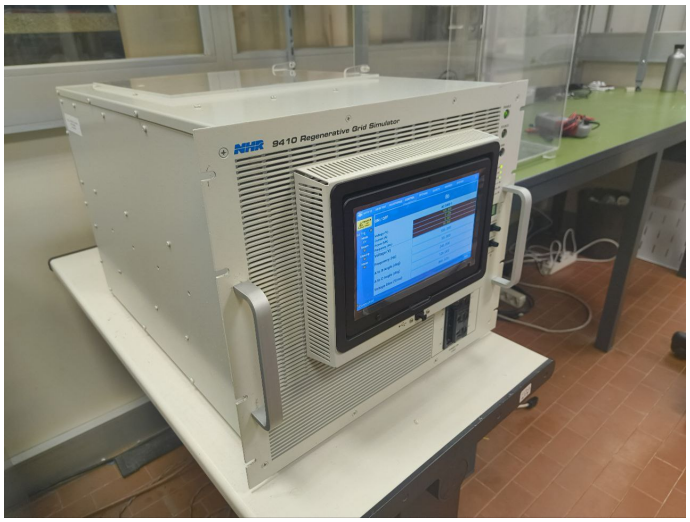


Figure 4.26: Power supply

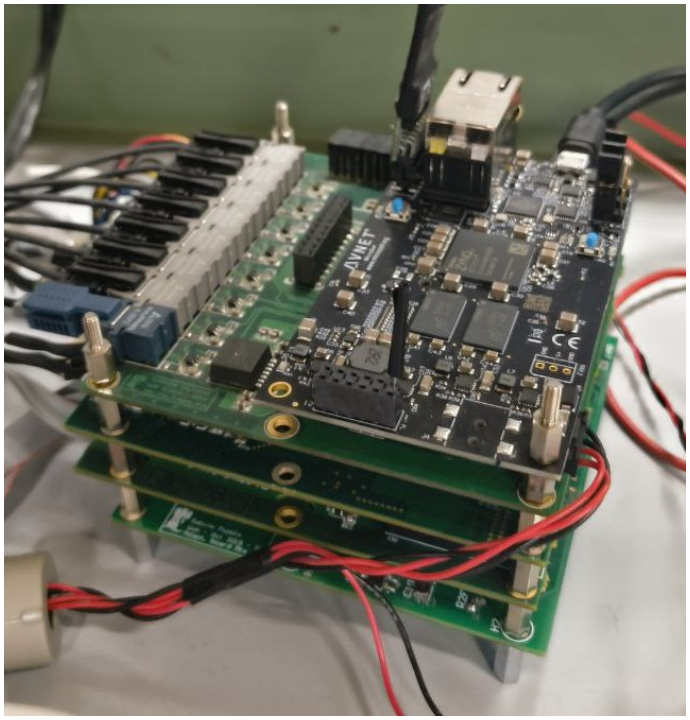


Figure 4.27: Control platform

and various protection functions.

The matrix converter is shown in Fig. 4.28. Converter parameters used in the experiments are listed in Table 4.20. Infineon IHW40N120R5 devices are used as power switches.

The load depends on the specific tests, but it is generally simulated either as a resistor in parallel with a voltage source or as a resistor alone. The parallel connection is required when using a voltage source, since the source is unidirectional.

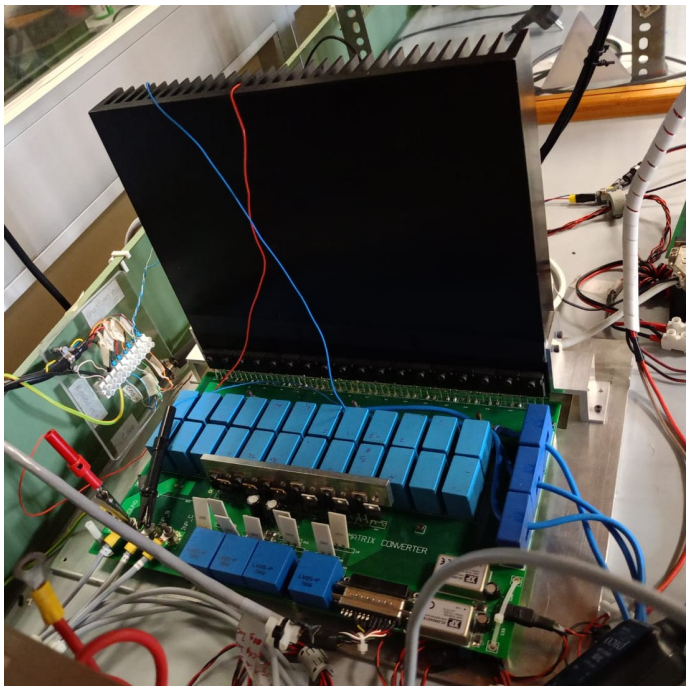


Figure 4.28: Matrix converter

Table 4.20: Setup Configuration

Input Side	
Capacitance C_f (μF)	1.2
Inductance L_f (mH)	2.4
Supply	
Input Voltage (RMS p-p), V	100
Input Frequency (Hz)	50

Output Side	
Capacitance C (μF)	50
Inductance L (mH)	1.6

4.6.2 Comparison of selected patterns considering switching losses

An experimental comparison was performed for several selected patterns, taking switching losses into account. Procedure that evaluates switching losses is described in the Section 4.3.3. Using information about the switching losses from the datasheet of the power switch used in the experimental setup, losses are calculated for each pattern assuming symmetrical carrier. Since input voltage is changing in a real time, average value of losses is calculated in whole input voltage period. The PWM frequency for each pattern was adjusted according to Table 4.13 to make a comparison between patterns that have equal switching losses. The selected patterns and their corresponding groups (see Table 4.13) are: $0h0m0$ ([1]), $0hm0h$ ($G3_{[h,m,0]}$), $hm0$ ($G3_{[h,m,0]}$), $0ml0m$ ($G1_{[m,l,0]}$),

and $m0l$ ($G2_{[m,l,0]}$). In the experiments shown below, voltage on the capacitor is set by power supply to simplify testing in certain operation conditions. While output current is controlled using PI controller that output voltage reference V_o^*. In the description of each figure, modulation index is specified. Output voltage can be calculated based on the index value considering that $V_{mag} = 80V$ in the experiments.

The PWM frequency for $0hm0h$ was set to 3000 Hz. Due to its inherently higher switching losses, f_{PWM} for $0h0m0$ was set to 2700 Hz. To match the switching losses of $0hm0h$ (by scaling PWM frequency according to the Table 4.13), the PWM frequency of $hm0$ was increased to 8800 Hz. Pattern $0ml0m$ has matching losses at 3300 Hz, while f_{PWM} for $m0l$ was set to 8800 Hz, as it exhibits the same switching losses as $hm0$.

Fig. 4.29 shows the system performance when the optimized $0h0m0$ pattern is used. Figs. 4.30 and 4.31 illustrate the performance of the $0hm0h$ pattern without and with optimization, respectively. Fig. 4.32 presents the system performance for the $hm0$ pattern. The right side of the graphs shows a zoomed view of the output voltage and current. Results in Figs. 4.29–4.32 correspond to a load voltage that gives a modulation index of $m = 1.25$ ($V_{cap} = 100$ V).

Despite exhibiting higher switching losses, the pattern $0h0m0$ produces higher output current ripple compared to the optimized $0hm0h$ and $hm0$ patterns. These results are consistent with the analytical predictions presented in Fig. 4.9.

The switching frequency ratio between $hm0$ and $0hm0h$ was chosen according to the values in Table 4.13, ensuring that both patterns have identical switching losses.

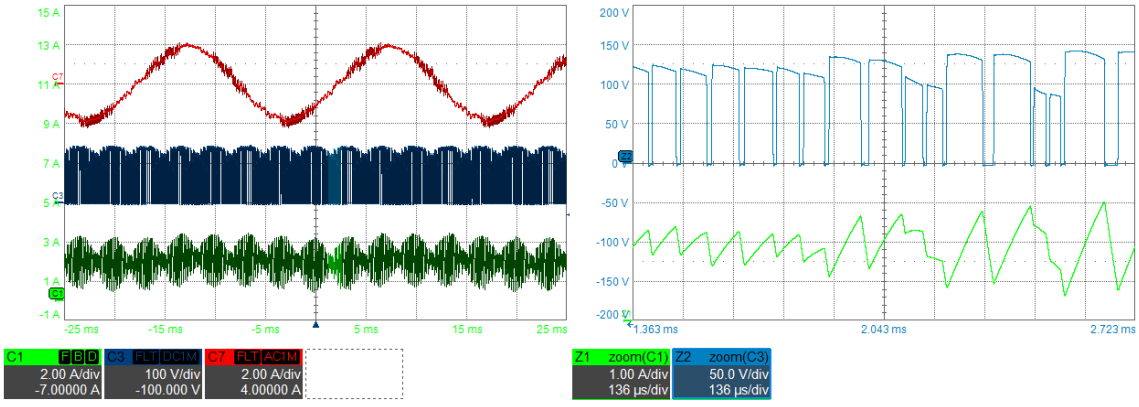


Figure 4.29: Experimental results for the $0h0m0$ pattern with optimization at a modulation index of $m = 1.25$ and a switching frequency of 2700 Hz. Input current (red), output voltage (blue), and output current (green).

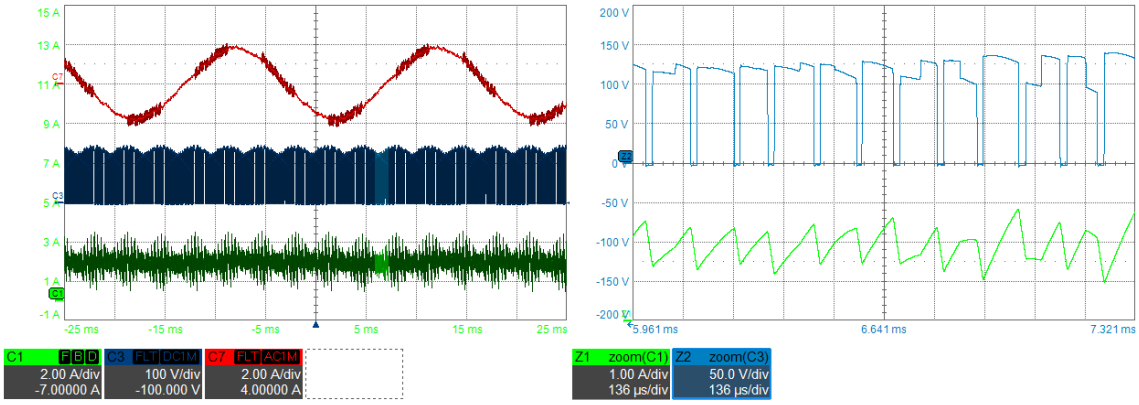


Figure 4.30: Experimental results for the $0hm0h$ pattern without optimization at a modulation index of $m = 1.25$ and a switching frequency of 3000 Hz. Input current (red), output voltage (blue), and output current (green).

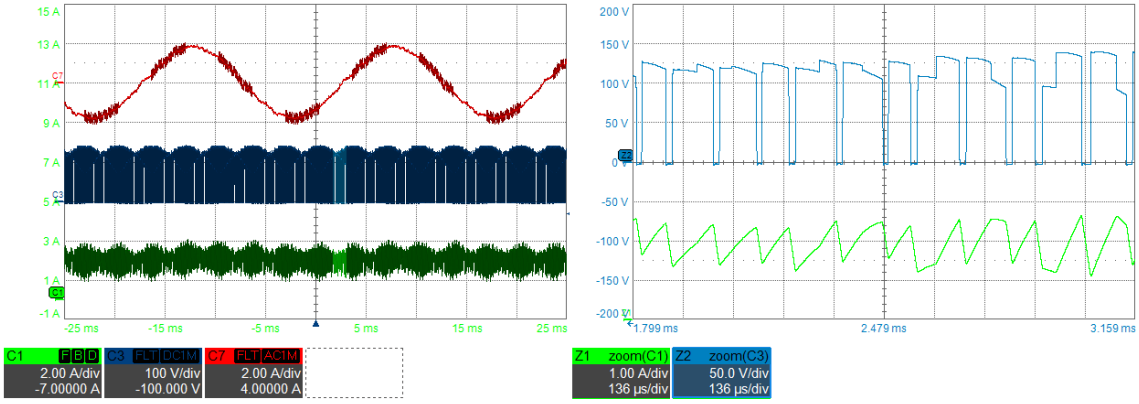


Figure 4.31: Experimental results for the $0hm0h$ pattern with optimization at a modulation index of $m = 1.25$ and a switching frequency of 3000 Hz. Input current (red), output voltage (blue), and output current (green).

The total harmonic distortion (THD) and current ripple for each pattern are summarized in Table 4.21. Pattern optimization for both $0hm0h$ and $0h0m0$ improves ripple and THD. The output ripple for $hm0$ closely matches that of $0hm0h$, confirming the theoretical conclusions discussed in the previous sections.

Due to the limited modulation index range of the $[m, l, 0]$ patterns, the performance of the converter using the $0ml0m$ and $m0l$ patterns is shown for a modulation index of $m = 0.7$. Results are presented in Figs. 4.33 and 4.34. Despite belonging to different groups, the patterns exhibit almost identical ripple, as seen in Fig. 4.9 and confirmed by the experimental results. The corresponding current ripple and input current THD are summarized in Table 4.21.

The input phase voltage lags the corresponding input current due to the effect of the input filter. At higher power levels, the phase shift between input current and voltage is

Table 4.21: Ripple and THD of selected patterns

Pattern	I_{ripple} (A)	THD (%)
$0h0m0$ Optimized	2.63	6.78
$0h0m0$ Not optimized	3.95	9.3
$0hm0h$ Optimized	1.73	4.41
$0hm0h$ Not optimized	2.6	4.48
$hm0$	1.75	4.16
$0ml0m$	2.03	6.42
$m0l$	2.01	3.68

expected to approach zero.

In Fig. 4.34, the output voltage exhibits pulses corresponding to V_h, despite the absence of a higher line-to-line voltage state in the pattern. This behavior is caused by the "4-step commutation" of the converter. Specifically, if at a given instant both output terminals must change phase, and one commutation is "soft" while the other is "hard," then during one dead-time interval the voltage between the terminals may be connected to a line-to-line voltage that is not the reference. In Fig. 4.34, this occurs when changes in the input angle alter the input voltages that form V_m. In Fig. 4.33, it happens more frequently due to switches between V_m and V_l, as discussed in more detail in Subsection 4.3.3.

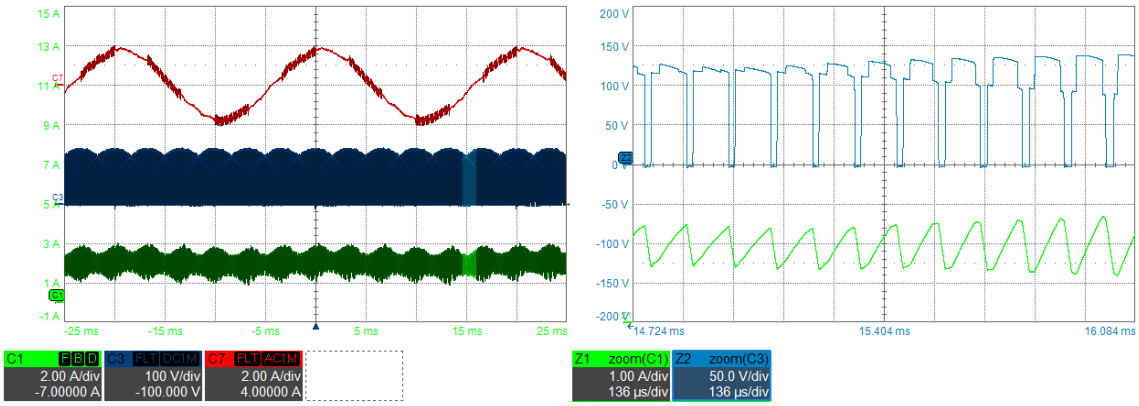


Figure 4.32: Experimental results for the $hm0$ pattern at a modulation index of $m = 1.25$ and a switching frequency of $8800\,\text{Hz}$. Input current (red), output voltage (blue), and output current (green).

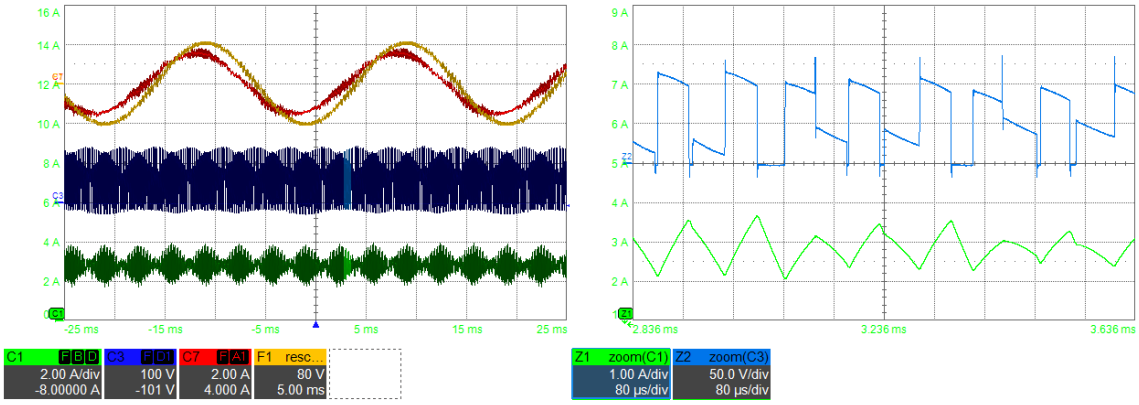


Figure 4.33: Experimental results for the $0ml0m$ pattern with optimization at a modulation index of $m = 0.7$ and a switching frequency of 3300 Hz. Input current (red), input voltage (yellow), output voltage (blue), and output current (green).

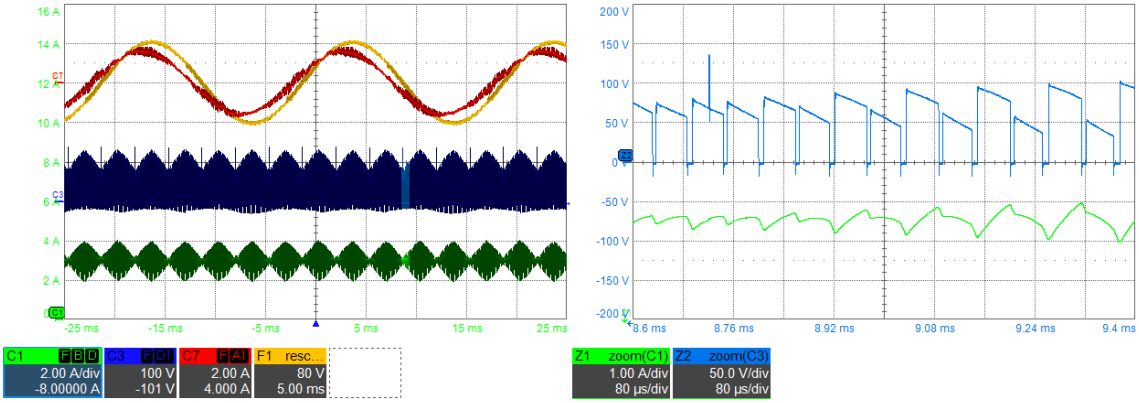


Figure 4.34: Experimental results for the $m0l$ pattern at a modulation index of $m = 0.7$ and a switching frequency of 8800 Hz. Input current (red), input voltage (yellow), output voltage (blue), and output current (green).

4.6.3 Comparison of experimental results to the analytical data for a selected patterns

Selected patterns are tested experimentally for the whole modulation index range, and the results are compared to the curves derived analytically.

Fig. 4.35 shows the comparison of normalized output current for the optimized $0h0m0$ pattern [1]. Experimental points are depicted with dots, and the line is a fitted curve. The experimental curve matches closely with the analytical curve, especially for medium values of the modulation index. For low modulation indexes, the differences are slightly higher, which can be explained by the larger impact of dead time and inverter nonlinearities in the low-voltage region, as will be explained later.

Fig. 4.36 shows several $[h, m, 0]$ patterns compared to the analytical curve. The exper-

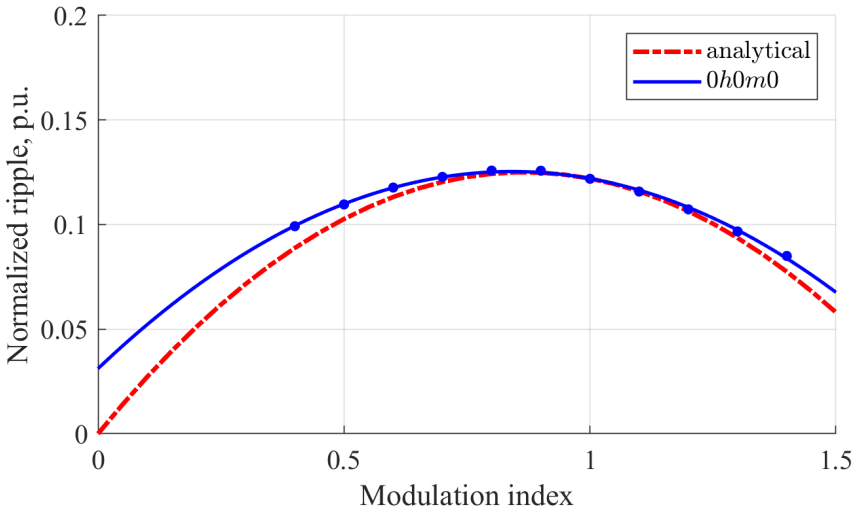


Figure 4.35: Comparison of experimental and analytical output current ripple for the optimized $0h0m0$ pattern. The analytical curve is shown in red, experimental points as blue dots, and the fitted experimental curve as a blue line.

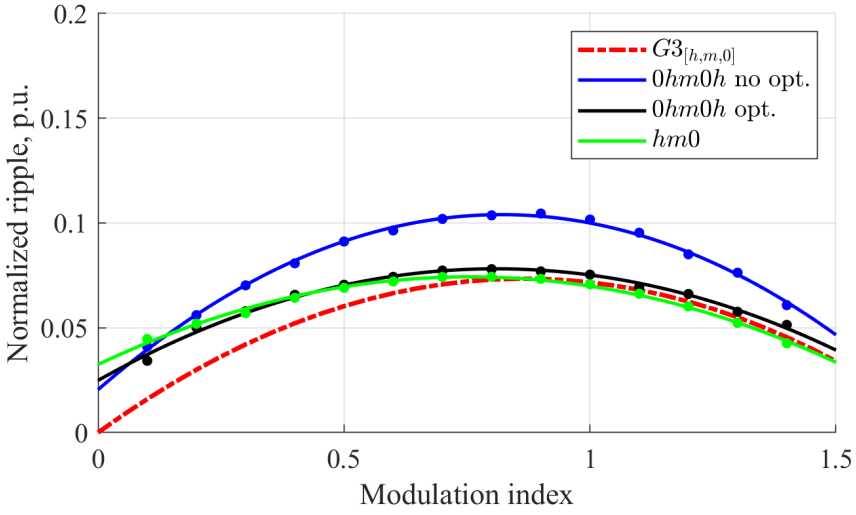


Figure 4.36: Comparison of experimental and analytical output current ripple for the selected $[h, m, 0]$ patterns. Experimental points are shown as dots, fitted experimental curves as solid lines, and the analytical curve as a dashed line.

imental patterns belong to the group $G3_{[h,m,0]}$ (see Table 4.13). The not optimized pattern $0hm0h$, depicted by a blue line, is shown as an experimental proof of the effectiveness of pattern optimization in reducing output current ripple. Optimized patterns $0hm0h$ and $hm0$ match closely with the computationally derived curve for $G3_{[h,m,0]}$. The deviation in the low modulation zone is the same as for the pattern $0h0m0$.

Fig. 4.37 presents a comparison of experimental and analytical output current ripple curves for selected $[m, l, 0]$ patterns. Patterns $0ml0m$ and $m0l$ belong to pattern groups $G1_{[m,l,0]}$ and $G2_{[m,l,0]}$, respectively. Computationally derived curves are close to the ex-

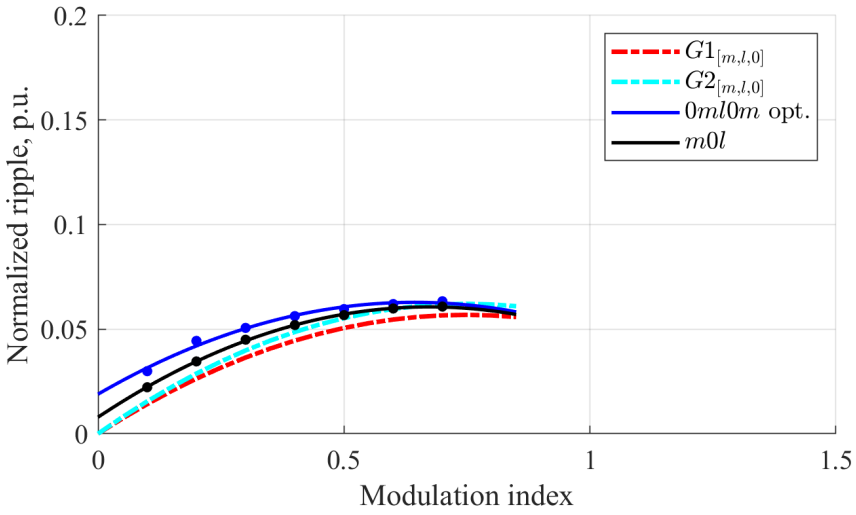


Figure 4.37: Comparison of experimental and analytical output current ripple for the selected $[m, l, 0]$ patterns. Experimental points are shown as dots, fitted experimental curves as solid lines, and the analytical curve as a dashed line.

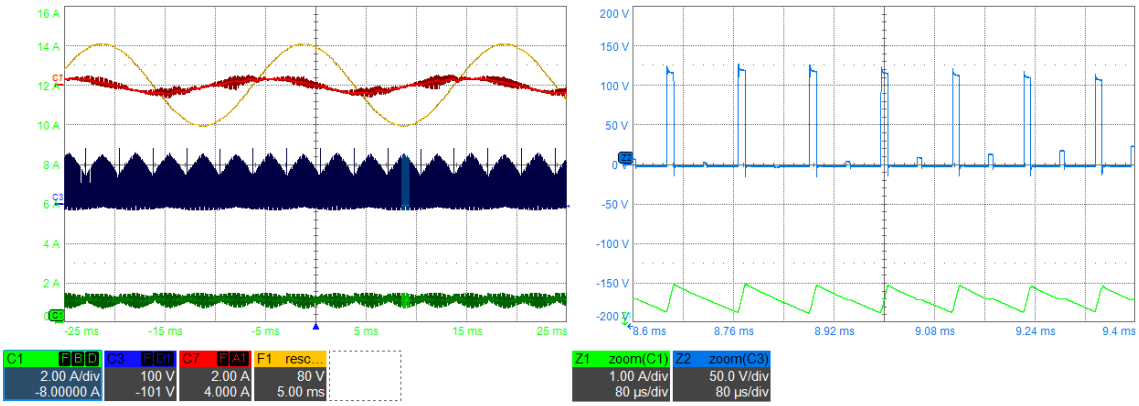


Figure 4.38: Experimental results for the $m0l$ pattern at a modulation index of $m = 0.1$ and a switching frequency of 8800 Hz. Input current (red), input voltage (yellow), output voltage (blue), and output current (green).

perimental ones. Moreover, the ripple for $[m, l, 0]$ patterns is much smaller compared to the ripple for $[h, m, 0]$ patterns in the low modulation index zone and matches the analytical curve better in this region. This can be explained by the smaller dead-time effects on the presented $[m, l, 0]$ patterns compared to $[h, m, 0]$. At low modulation index, the effect of dead time can be significant, especially if the duty cycle of the corresponding state approaches zero.

Fig. 4.38 and Fig. 4.39 show the performance of $m0l$ and $hm0$ patterns at modulation index $m = 0.1$. The output current for $m0l$ is much cleaner, and the ripple of the fundamental component is much smaller compared to the $hm0$ pattern. Zoomed output voltage pulses are wider in $m0l$, which can be partially explained by the application of

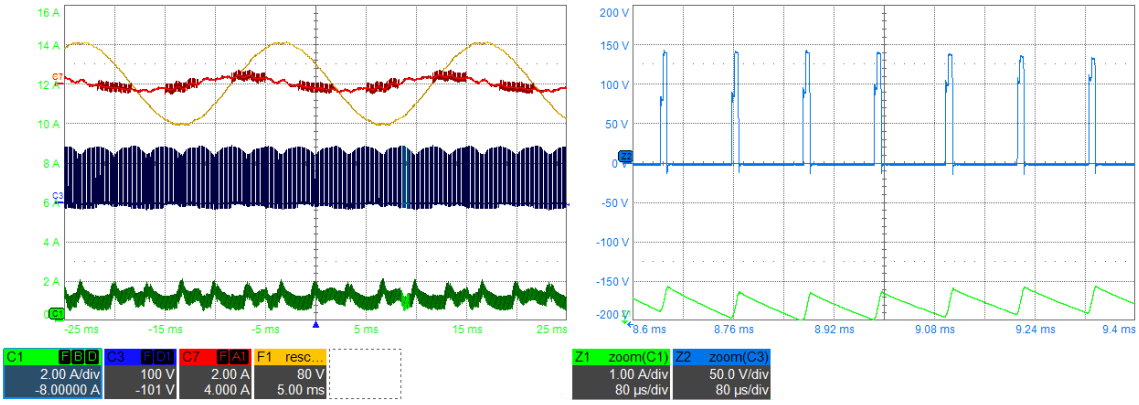


Figure 4.39: Experimental results for the $hm0$ pattern at a modulation index of $m = 0.1$ and a switching frequency of 8800 Hz. Input current (red), input voltage (yellow), output voltage (blue), and output current (green).

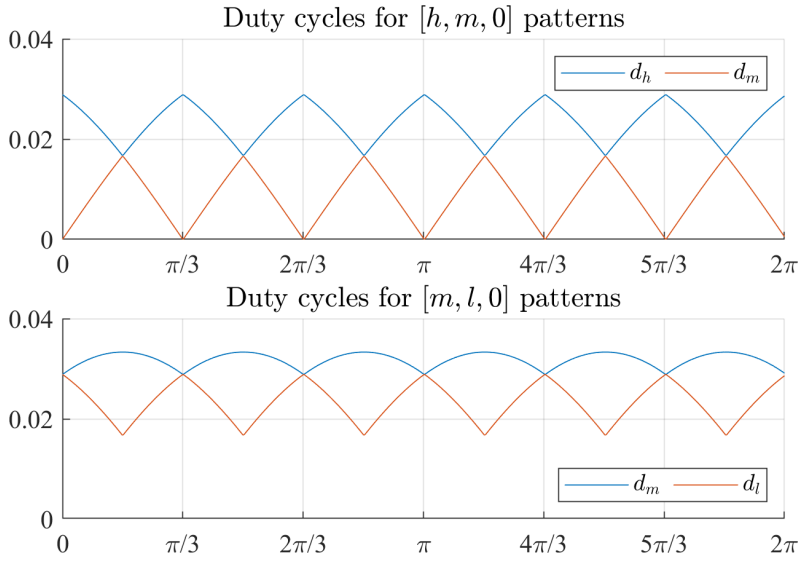


Figure 4.40: Duty cycles for the $[m, l, 0]$ and $[h, m, 0]$ patterns as a function of the input voltage angle at a modulation index of $m = 0.1$.

lower voltages but also by variations in active duty cycle during the input voltage period. Fig. 4.40 shows the duty cycles as a function of input voltage angle for modulation index $m = 0.1$ for patterns $[m, l, 0]$ and $[h, m, 0]$. It should be noted that the duty cycles for $[m, l, 0]$ never approach zero; therefore, the effect of dead time is lower.

Fig. 4.41 shows the input current THD for selected patterns. Results are not shown for low modulation index due to the low fundamental component of the input current and the increased impact of converter nonlinearities in this region and low signal-to-noise ratio, as can be seen from the current waveform (red) in Fig. 4.39.

The $0h0m0$ pattern exhibits the highest THD among all patterns at high modulation index, which can be explained by its higher ripple. For the other patterns, the average

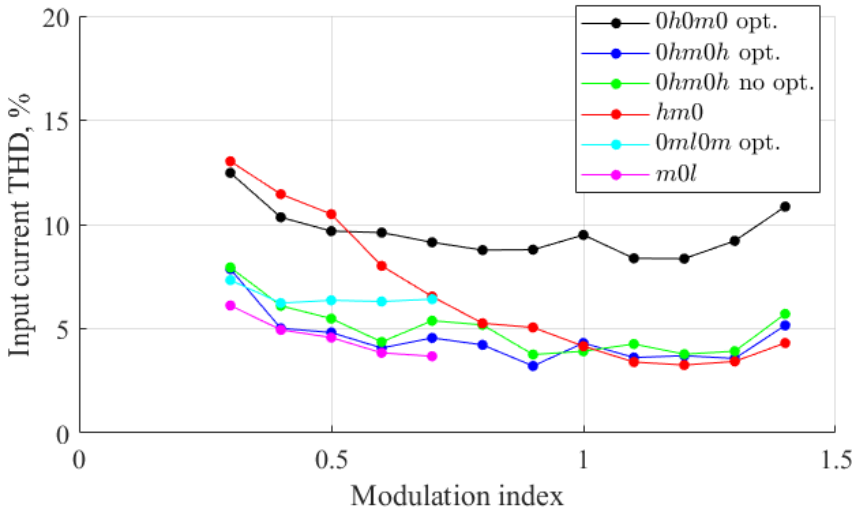


Figure 4.41: Measured input current THD for the selected patterns. Experimental points are shown as dots.

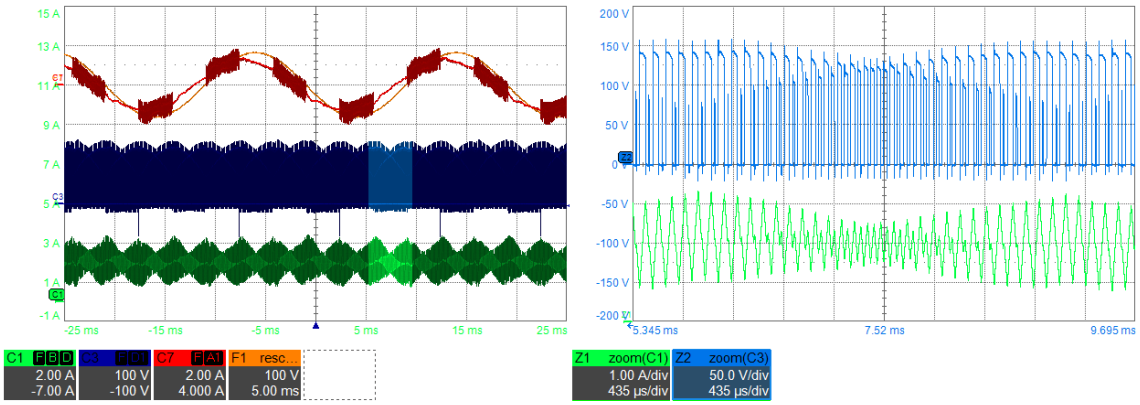


Figure 4.42: Experimental results for the $h0m$ pattern at a modulation index of $m = 0.8$ and a switching frequency of 8800 Hz. Input current (red), input voltage (orange), output voltage (blue), and output current (green).

THD is around 5%. The $[m, l, 0]$ patterns have the lowest THD at $m = 0.3$, for the reasons described above.

4.6.4 Pattern switch within input voltage period

Experimental tests were conducted for the optimized pattern sets with $s = 2$ and $s = 3$. The corresponding pattern maps are shown in Fig. 4.11 for $s = 2$ and in Fig. 4.12 for $s = 3$. For the $s = 2$ set, the patterns $m0l$ and mhl were selected (Table 4.14b). These patterns were chosen because, according to Table 4.13, they provide an optimal ripple-to-loss relationship. For the $s = 3$ set, the patterns $m0l$, mhl, and $h0m$ were selected (Table 4.14c). The first two patterns are common to both sets.

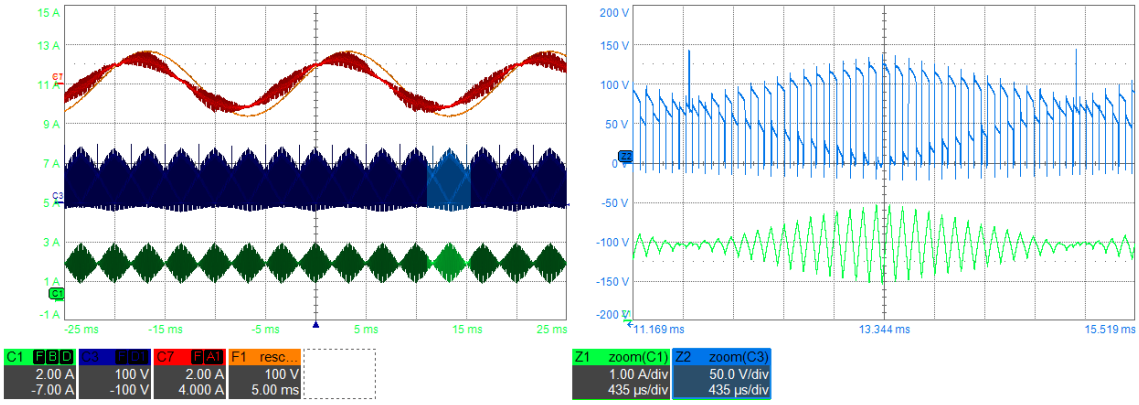


Figure 4.43: Experimental results for the $s = 2$ pattern set at a modulation index of $m = 0.8$ (pattern $m0l$) and a switching frequency of 8800 Hz. Input current (red), input voltage (orange), output voltage (blue), and output current (green).

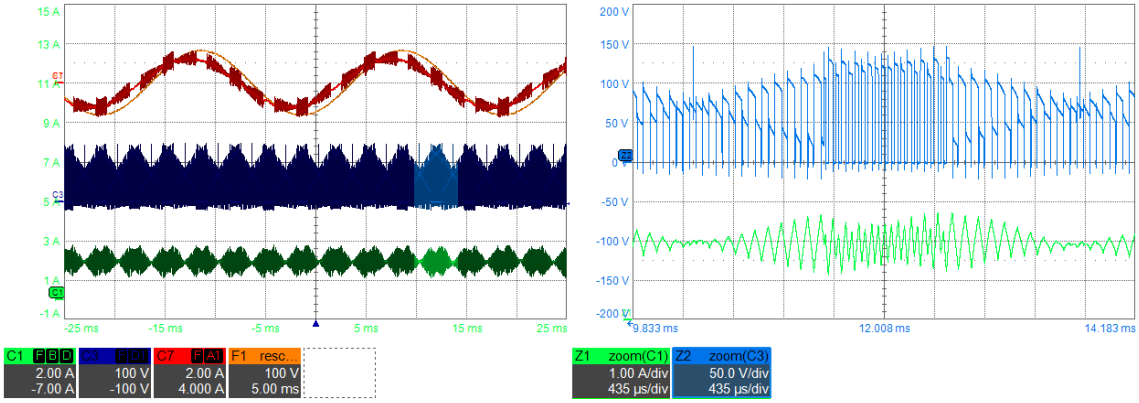


Figure 4.44: Experimental results for the $s = 3$ pattern set at a modulation index of $m = 0.8$ (patterns $m0l$ and $h0m$) and a switching frequency of 8800 Hz. Input current (red), input voltage (orange), output voltage (blue), and output current (green).

If multiple patterns can be applied at a given operating point, look-up tables (LUTs) can be used to select the pattern that results in the lowest ripple. An example of this situation is the switching between the $m0l$ and $h0m$ patterns at low modulation indices under unity power factor.

In other cases, switching between patterns is mandatory because the operational regions of the patterns are adjacent but do not overlap. In such situations, the pattern selection is performed by calculating the duty cycles for each candidate pattern and selecting the one that satisfies the condition

$$|d_1| + |d_2| + |d_3| < 1. \tag{4.18}$$

An example of this case is the switching between the $s = 2$ patterns ($m0l$ and mhl). Al-

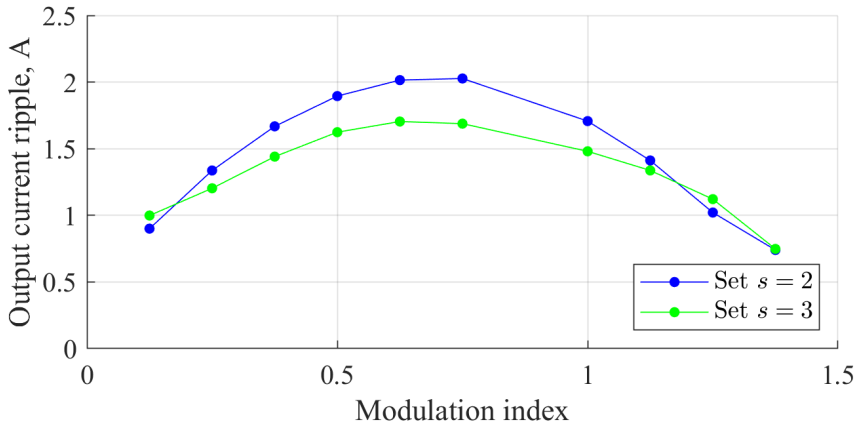


Figure 4.45: Measured maximum output current ripple for the $s = 2$ and $s = 3$ pattern sets.

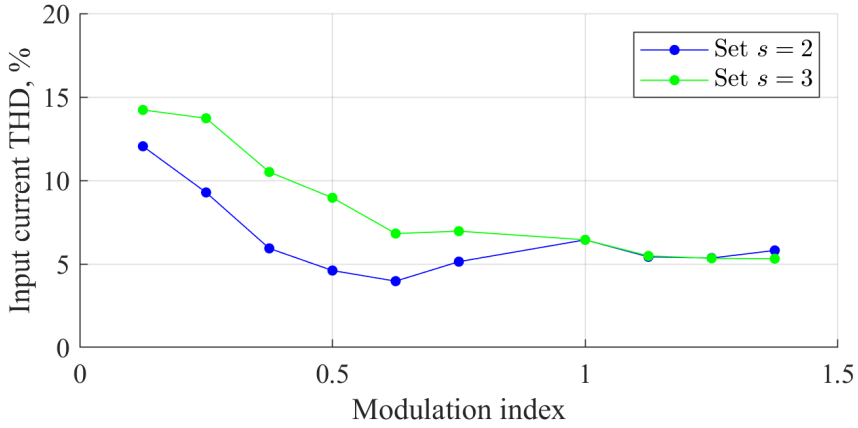


Figure 4.46: Measured input current THD for the $s = 2$ and $s = 3$ pattern sets.

though LUT-based selection is possible, it would require high precision to avoid selecting patterns that violate condition (4.18).

Alternatively, at each control step, the duty cycles for all patterns in the selected set can be computed, and the corresponding output current ripple can be evaluated based on the duty cycles and the voltage angle. The pattern that satisfies condition (4.18) and yields the lowest ripple is then selected for the next step. This approach increases computational effort but eliminates the need for LUT storage. This method was adopted for the experimental results presented below.

Fig. 4.42 and Fig. 4.43 show the measured waveforms for the $h0m$ pattern and the $s = 2$ pattern set, respectively. At a modulation index of $m = 0.8$ and unity power factor, only the $m0l$ pattern is active within the $s = 2$ set. The zoomed-in output current waveforms illustrate the ripple over approximately a $\frac{\pi}{3}$ interval of the input voltage angle. From the comparison, it is evident that the $h0m$ pattern exhibits a minimum ripple region around

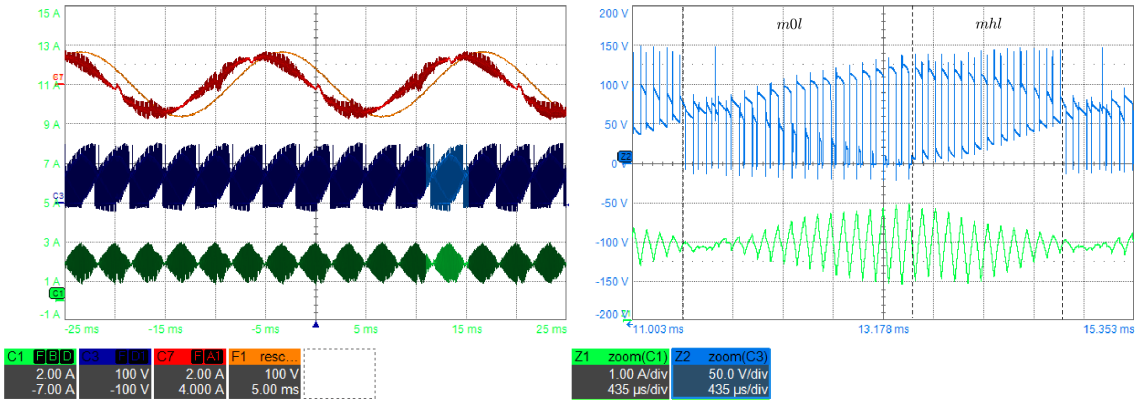


Figure 4.47: Experimental results for the $s = 2$ pattern set at a modulation index of $m = 0.8$ and a power factor of $\varphi = \frac{\pi}{8}$ rad. Switching frequency 8800 Hz. Input current (red), input voltage (orange), output voltage (blue), and output current (green).

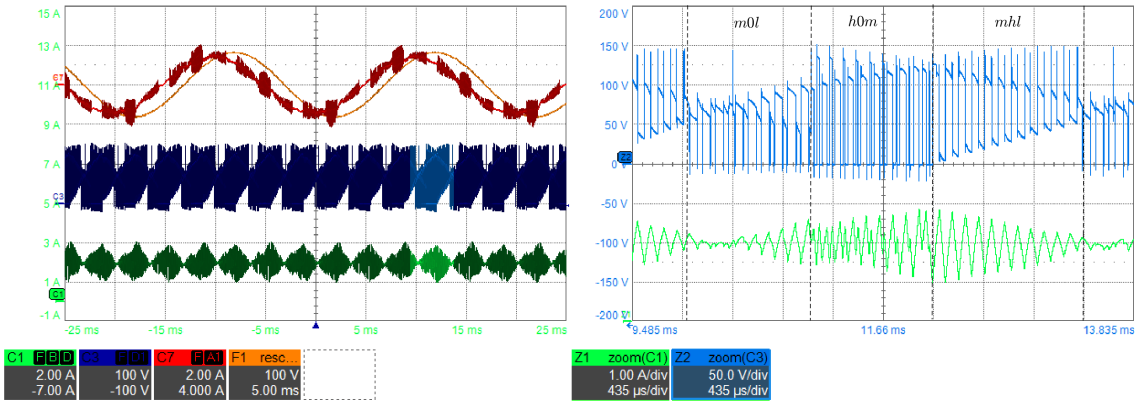


Figure 4.48: Experimental results for the $s = 3$ pattern set at a modulation index of $m = 0.8$ (patterns $m0l$ and $h0m$) and a power factor of $\varphi = \frac{\pi}{8}$ rad. Switching frequency 8800 Hz. Input current (red), input voltage (orange), output voltage (blue), and output current (green).

an angle of $\frac{\pi}{6}$ rad, whereas the $m0l$ pattern produces its highest ripple in this same region. The combination of patterns forming the $s = 3$ set, shown in Fig. 4.44, results in reduced ripple, in agreement with the analytical calculation provided by the map in Fig. 4.12.

Figure 4.45 presents a comparison of the maximum output current ripple for the $s = 2$ and $s = 3$ sets. As expected, the $s = 3$ set yields a lower ripple. However, the input current THD for the $s = 3$ set is higher at low modulation indices compared to the $s = 2$ set, as shown in Fig. 4.46. This behavior is attributed to the different sensitivity of the patterns to dead-time effects, as discussed in Subsection 4.3.4.1.

A comparison between the $s = 2$ pattern set $(m0l + mhl)$ and the $s = 3$ pattern set $(m0l + mhl + h0m)$ at a power factor of $\varphi = \frac{\pi}{8}$ rad is presented in Fig. 4.47 and

Fig. 4.48. At a modulation index of $m = 0.8$ and $\varphi = \frac{\pi}{8}$ rad, both pattern sets operate by switching between patterns within a single input voltage period. The black dashed lines indicate the instants at which pattern transitions occur. The maximum peak-to-peak output current ripple is $1.92\,\mathrm{A}$ for the $s = 3$ set and $2.06\,\mathrm{A}$ for the $s = 2$ set. The corresponding input current THD values are 6.7% and 7.8%, respectively.

4.7 Chapter Summary

This chapter presented a systematic way for identifying and optimizing switching patterns in AC–DC matrix converters to achieve a superior trade-off between output current ripple and switching losses. Unlike conventional studies that focus on a limited selection of sequences, this work evaluated the complete set of feasible patterns. The core of the proposed approach lies in the automated optimization of duty-cycle distributions. For patterns with four or five states, the additional degrees of freedom were leveraged to minimize the maximum output current ripple. Switching losses were integrated into the optimization process, ensuring that ripple reduction was not achieved through an inefficient increase in commutations. This resulted in the identification of optimal pattern groups that maintain high efficiency while reducing the output current ripple.

Experimental validation confirmed the analytical predictions and demonstrated good agreement between the calculated and measured results. The selection of the modulation strategy and switching pattern depends on specific system requirements. For systems operating over a wide range of conditions, the DC-SVM strategy combined with the optimized patterns identified in this chapter represents a suitable solution.

Further reduction of the output current ripple can be achieved if patterns are switched within the input voltage period. Pattern sets that provide the lowest maximum current ripple were determined and experimentally verified. It was shown that if the operating range is limited or the power factor is specified, the optimization can be repeated to identify locally optimal pattern sets.

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Chapter 5:

Discontinuous conduction mode modulation

Another way to increase converter performance, namely efficiency and input current THD, at low-current operating points is to employ discontinuous conduction mode (DCM) modulation. Existing research on matrix converter modulation primarily focuses on the selection of switching patterns and/or distribution of active and passive states. The method proposed in this chapter can be applied to any of the presented patterns, with minor modifications, leading to further improvements in converter efficiency at low output currents. In this work, DCM modulation was implemented specifically for the $h0m$-$m0l$ patterns. The investigation of this topic predates the results presented in Chapter 4. Therefore, the adopted patterns were selected based on earlier insights and do not reflect the more optimal solutions identified subsequently.

Zero-current switching (ZCS) operation for isolated matrix-based AC–DC converters has been investigated in [1–3]. In these studies, ZCS is achieved by equalizing volt-seconds in the primary and secondary windings during each cycle and aligning the rising or falling edges of the primary and secondary voltages, ensuring that the same current flows at the start and end of the cycle. Reference [1] further proposes a voltage commutation compensation method to eliminate current offsets between cycles caused by commutation delays.

In the configuration considered in this thesis (Fig. 2.1), the load voltage cannot be directly controlled, unlike the isolated converter variations. Consequently, DCM must occur naturally, requiring a different approach from existing solutions.

Existing DCM strategies developed for standard buck converters cannot be directly applied to AC–DC matrix converters due to the additional requirement of maintaining sinusoidal input currents. In DCM, the output current waveform becomes asymmetrical, so applying CCM-based modulation methods results in significant input-current distortion. The method proposed here explicitly addresses this challenge, ensuring sinusoidal input

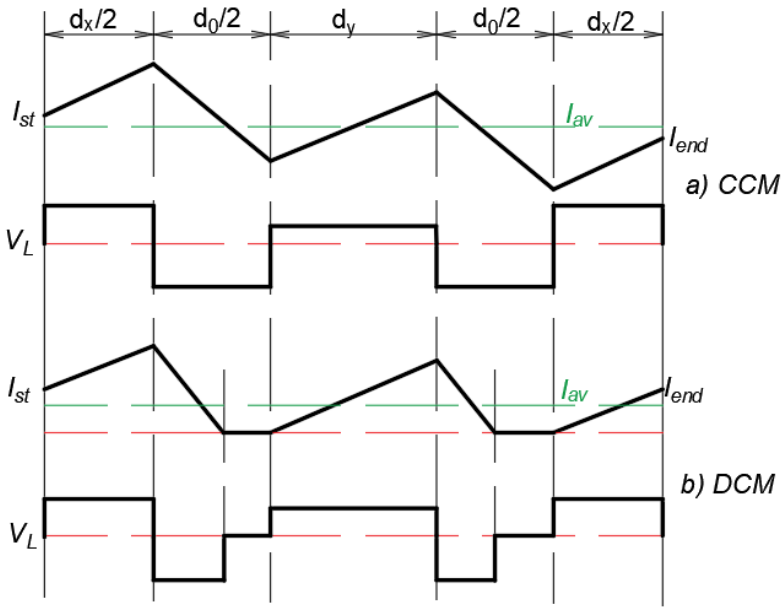

Figure 5.1: Inductor voltage form in CCM and DCM

currents even when DCM occurs at the output.

This chapter presents a new DCM modulation scheme capable of reducing converter losses while simultaneously decreasing input and output current total harmonic distortion (THD).

5.1 Comparison of standard CCM and DCM voltage control modulation

In this section, a review of the standard modulation approach in CCM and the implementation difficulties of voltage control in DCM are presented.

5.1.1 CCM Modulation

Standard CCM voltage control is presented in Section 3.1.1.

Due to the usage of a triangular carrier in Fig. 5.1a, voltage, and as a result, current have a symmetrical structure. The current average value during the application of each duty cycle is the same and equals the average current value I_{out} during the whole PWM

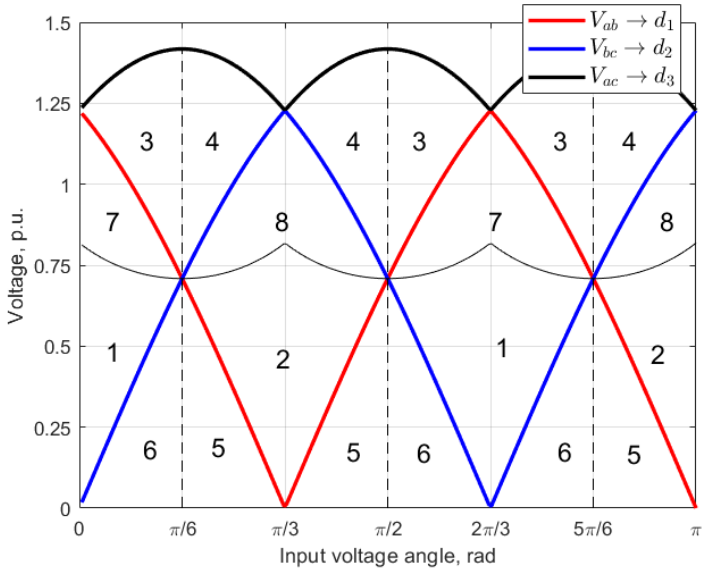

Figure 5.2: Output voltage map in steady-state (voltage is normalized with respect to input phase-to-phase RMS voltage)

period, so:

$$I_{d_x} = I_{d_y} = I_{out} \tag{5.1}$$

The average current value I_{av} can be found as:

$$I_{av} = \frac{I_{st} + I_{end}}{2} \tag{5.2}$$

where I_{st}, I_{end} are current values at the start and the end of the PWM cycle, respectively.

Taking into account the constraint (3.2) and the input voltage angle φ_{in}, the voltage map shown in Fig. 5.2 can be constructed. This map allows determination of the duty cycles required to achieve a given V_o^* at steady state.

In this chapter for lower modulation indexes, $[m, l, 0]$ pattern is used, while for higher modulation indexes - $[h, m, 0]$. According to Fig. 5.2, eight distinct operation modes can be identified. In modes 1, 2, 5, and 6, vectors V_{ab} and V_{bc} are used to generate the required voltage V_o^*, while V_{ac} is not applied. In modes 1 and 6, V_{ab} is applied first, whereas in modes 2 and 5, V_{bc} is applied first.

For continuous conduction mode (CCM) in steady state, the maximum possible output voltage achievable using only the voltage vectors V_{ab} and V_{bc} (i.e. pattern $[m, l, 0]$) can be

calculated from (3.1), (3.2), and (3.5), resulting in:

$$V_{o_{max(d_1,d_2)}} = \frac{-V_a(V_a - V_b) + V_c(V_b - V_c)}{V_c - V_a} \tag{5.3}$$

Equation (5.3) is represented by a thin black line in Fig. 5.2. Therefore, modes 3, 4, 7, and 8 require the use of V_{ac}. The voltage modes and corresponding voltage vectors that will be used throughout this research are presented in Table 5.1. The voltage vectors application order does not matter in CCM; however, in DCM, the upper vector in the table is applied first in direct power flow, and second in reverse power flow. This aspect is discussed in more detail in the following sections.

Table 5.1: Voltage Modes

Voltage mode	1	2	3	4	5	6	7	8
Used voltage vectors	V_{ab} V_{bc}	V_{bc} V_{ab}	V_{ac} V_{ab}	V_{ac} V_{bc}	V_{bc} V_{ab}	V_{ab} V_{bc}	V_{ac} V_{ab}	V_{ac} V_{bc}

5.1.2 DCM Modulation

As previously mentioned, in CCM, the voltage applied to the inductor in one PWM cycle is symmetrical (Fig. 5.1a), which leads to the fulfillment of conditions (5.1) and (5.2). In the case of DCM, once the current reaches zero, the effective voltage applied to the inductor is also zero. As a result, voltage symmetry is lost (Fig. 5.1b). Voltage control in DCM can be achieved by solving the system of equations (3.3), (3.4), and the modified (3.1):

$$V_o^* = d_1(V_a - V_b) + d_2(V_b - V_c) + d_3(V_a - V_c) + d_{DCM}V_{cap} \tag{5.4}$$

where d_{DCM} is the duty cycle that corresponds to the time during which I_{out} is zero. During d_{DCM}, I_{out} is constant, so the equivalent inductor voltage is zero. As a result, the equivalent V_o must be equal to V_{cap}.

Assuming that V_{cap} is constant during one PWM cycle, and the reference V_o^* is reached,

the current at the end of the PWM cycle can be calculated in both CCM and DCM as:

$$I_{end} = I_{st} + T_s(V_o^* - V_{cap})/L \tag{5.5}$$

where L is the inductance value. However, unlike CCM, the current average in DCM cannot be calculated directly from I_{st} and I_{end} as in (5.2). Instead, it depends on input voltages, output current, inductance value, PWM frequency, and so on, which makes DCM voltage control unacceptable given a fixed symmetrical switching pattern (Fig. 5.1a).

Condition (5.2) can be achieved not only when symmetrical voltage is applied. The output current variation $i_{var} = I_{end} - I_{st}$ can be expressed as:

$$i_{var}(t) = \frac{1}{L}\int_0^t v_L(\tau)d\tau \tag{5.6}$$

where v_L is inductor voltage. The condition that forces the average current variation to be half of i_{var} during the whole cycle (which leads to the fulfillment of (5.2)) is:

$$\frac{1}{2}i_{var}(T_s) = \frac{1}{T_s}\int_0^{T_s} i_{var}(\tau)d\tau \tag{5.7}$$

After substituting (5.6) into (5.7), the condition for the v_L shape during one cycle that guarantees (5.2) can be found:

$$\int_0^{T_s} \tau v_L(\tau)d\tau = \frac{T_s}{2}\int_0^{T_s} v_L(\tau)d\tau \tag{5.8}$$

where $\frac{1}{2}\frac{1}{T_s}\int_0^{T_s} v_L(\tau)d\tau = \frac{1}{2}(V_o^* - V_{cap})$ represents half of the average voltage on the inductor.

Condition (5.8) is inherently fulfilled in CCM when symmetrical voltage is applied. In DCM, an additional degree of freedom has to be introduced to fulfill this condition, given that the commutation sequence is unchanged. If the number of commutations per cycle is fixed, one way to satisfy (5.8) is to introduce a shift δ for the duty cycles (Fig. 5.3). With a correctly calculated δ, condition (5.8) can be achieved without changing the average V_o.

The introduction of this additional variable leads to an increase in computation difficulty. However, it can be avoided if the output current is controlled directly. In the following section, a modulator for current control in CCM and DCM is presented.

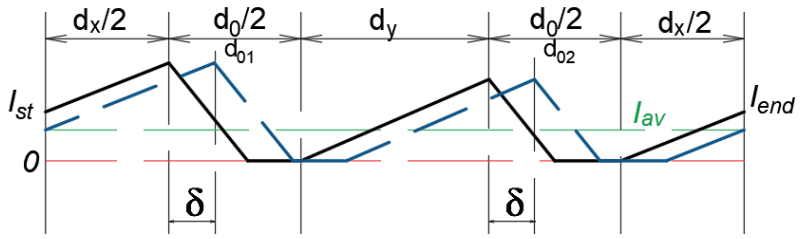

Figure 5.3: Current form with shift δ. Original current waveform (black), modified current waveform (blue)

5.2 Proposed current control modulation

As mentioned in the previous section, voltage control in DCM operation increases computational complexity and requires additional degree of freedom compared to current control. Therefore, this section proposes a modulation and control scheme that directly regulates the output current I_{out}.

To make the control approach homogeneous, the new modulation scheme is adopted both when the converter is operating in DCM and CCM. The next subsection starts describing the latter case.

5.2.1 CCM Modulation

Let's define a new variable I^* that represents the reference value for the current at the start and the end of the PWM period. This value has to be calculated in order to guarantee $I_{av} = I_{ref}$, where I_{ref} is the average current reference.

In CCM, in steady state, since condition (5.2) is fulfilled, I^* can be easily derived as

$$I^* = I_{ref} \tag{5.9}$$

The output current transient from I_{st} to $I_{end} = I^*$ (Fig. 5.1a) can be described in the following way:

$$I_{st} + k_{d_x} d_x T_s + k_{d_y} d_y T_s + k_{d_0} d_0 T_s = I^* \tag{5.10}$$

where $x \in [1, 2, 3]$, $y \in [1, 2, 3]$ are the duty cycle indexes that are applied during one cycle, $d_0 = 1 - d_x - d_y$ is the passive duty cycle, and T_s is the PWM period. Slopes k_{d_x},

k_{d_y}, k_{d_0} are calculated as

$$\begin{aligned} k_{d_1} &= (V_a - V_b - V_{cap})/L \\ k_{d_2} &= (V_b - V_c - V_{cap})/L \\ k_{d_3} &= (V_a - V_c - V_{cap})/L \\ k_{d_0} &= (-V_{cap})/L \end{aligned} \tag{5.11}$$

The selection of active duty cycles is the same as presented in previous chapters, however, the voltage mode is chosen based on V_{cap} instead of V_0^*. This assumption is reasonable since, at steady state, the average inductance voltage is zero. Duty cycles are calculated by solving the system of equations (3.5), (5.9), (5.10), (5.11). The system can be solved analytically. The solution when d_1 and d_2 are applied is

$$\begin{aligned} d_1 &= \frac{V_a(I_{st} - I^* + T_s k_{d_0})}{T_s(V_a(k_{d_0} - k_{d_1}) - V_c(k_{d_0} - k_{d_2}))} \\ d_2 &= -\frac{V_c d_1}{V_a} \end{aligned} \tag{5.12}$$

The solution for pair d_1, d_3 is

$$\begin{aligned} d_1 &= \frac{V_b(I_{st} - I^* + T_s k_{d_0})}{T_s(V_b(k_{d_0} - k_{d_1}) - V_c(k_{d_0} - k_{d_3}))} \\ d_3 &= \frac{V_c d_1}{V_b} \end{aligned} \tag{5.13}$$

The solution for pair d_2, d_3 is

$$\begin{aligned} d_2 &= \frac{V_b(I_{st} - I^* + T_s k_{d_0})}{T_s(V_a(k_{d_0} - k_{d_3}) - V_b(k_{d_0} - k_{d_2}))} \\ d_3 &= \frac{V_a d_1}{V_b} \end{aligned} \tag{5.14}$$

5.2.2 DCM Modulation

In DCM, conditions (5.2) and (5.9) do not hold, and additional steps are required to calculate I^*. Depending on the working point, 4 possible current waveform cases in direct power flow can arise, as shown in Fig. 5.4. d_0 is a passive duty cycle and corresponds to the application of zero voltage between the output terminals. Due to symmetrical carrier, voltage that corresponds to d_0 and d_x is applied two times in two equal time periods.

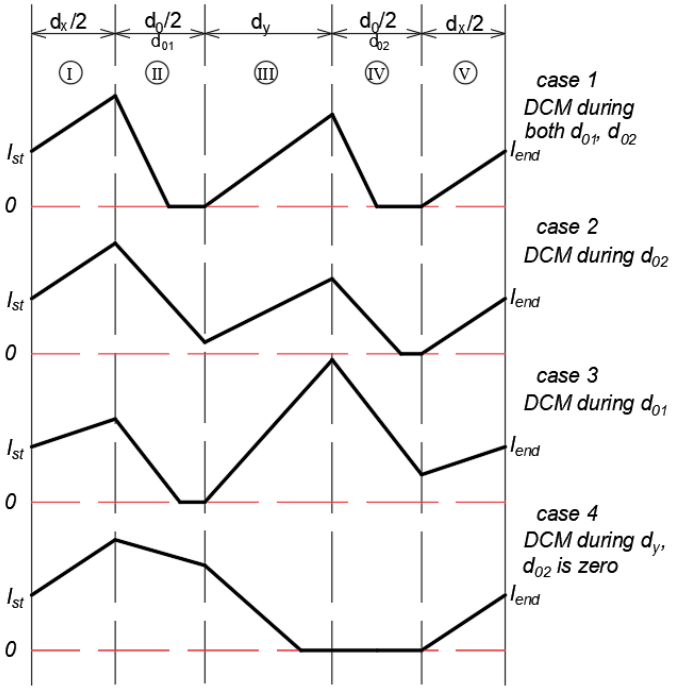

Figure 5.4: Possible current waveforms during DCM. Direct power flow

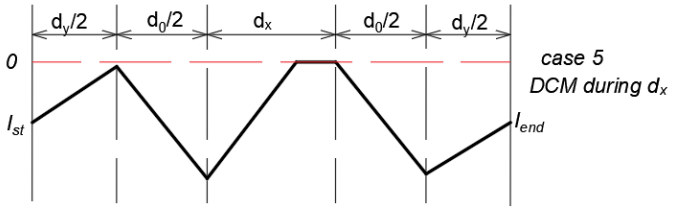

Figure 5.5: Possible current waveforms during DCM. Reverse power flow

The duty cycle that corresponds to the highest slope is applied first, according to Table 5.1. It is done to avoid DCM zones in the sections I and V. In the reverse power flow, the highest slope is applied second for the same reason, as shown in Fig. 5.5.

Not all current waveforms are possible for every voltage mode in direct power flow. In voltage modes 1, 2, 3, and 4, only output current waveforms 1, 2, and 3 can exist. In voltage modes 5, 6, 7, and 8, instead, only current waveforms 2 and 4 occur.

In general, when calculating duty cycles, the type of current waveform cannot be predicted in advance. So, after determining the voltage mode and power flow direction, the calculations have to be made for every possible admissible current waveform until the correct one is found. It should be noted that the CCM waveform has to be also checked. Steps to be performed each PWM period are shown in Algorithm 1.

The algorithm can be divided into three main steps: calculation of I^*, calculation of

d_x, d_y, and validation. Due to limited space, equations are derived only for one current waveform (case 1), assuming that active duty cycles are d_x and d_y (d_x is applied first). The derivation procedure for other waveform types and voltage modes is the same.

5.2.2.1 Calculation of I^*

The average current value in a PWM period can be calculated as

$$I_{av} = (I_I + I_V)\frac{d_x}{2} + (I_{II} + I_{IV})\frac{d_0}{2} + I_{III}d_y = I_{ref} \tag{5.15}$$

With reference to Fig. 5.4, I_k, $k \in [I..V]$, are the average currents during each section of the current waveform. They can be found as

$$\begin{aligned} I_I &= I^* + \frac{1}{2}k_{d_x}T_s\frac{d_x}{2} \\ I_{II} &= \frac{-(I^* + k_{d_x}T_s\frac{d_x}{2})^2}{k_{d_0}T_s d_0}, \\ I_{III} &= \frac{1}{2}k_{d_y}d_y T_s, \\ I_{IV} &= \frac{-(k_{d_y}T_s d_y)^2}{k_{d_0}T_s d_0}, \\ I_V &= \frac{1}{2}k_{d_x}T_s\frac{d_x}{2} \end{aligned} \tag{5.16}$$

In order to ensure that the value of the current is the same at the start and at the end of the PWM period and to provide a relation between I^* and duty cycles, the following condition has to be fulfilled

$$I^* = \frac{1}{2}k_{d_x}T_s d_x \tag{5.17}$$

I^* can be found by solving the system of three nonlinear equations

- (5.15), (5.16) that guarantee reference average current;
- (5.17) that provides $I_{st} = I_{end} = I^*$;
- (3.3), (3.4) that ensures sine wave input currents with unity input power factor.

Please note that only the I^* value is kept for the next steps. d_x and d_y are discarded and recalculated as explained in the following subsection.

Algorithm 1 Duty Cycles calculation in DCM

procedure
    Data acquisition $\leftarrow V_a, V_b, V_c, V_{cap}, I_{out}$
    Voltage mode and power flow direction determination
    $types \leftarrow$ array of possible current waveforms
    $i \leftarrow 0$
    $isValid \leftarrow false$
    repeat
        Calculate I^* for waveform $types(i)$
        Calculate d_x, d_y for waveform $types(i)$
        $isValid \leftarrow$ validation of d_x, d_y
        $i \leftarrow i + 1$
    until $isValid = true$ or all waveforms are checked
    if $isValid = true$ then
        Use calculated d_x, d_y in the next PWM period
    else
        Calculation error
    end if
end procedure

5.2.2.2 Calculation of d_x, d_y

Duty cycles d_x and d_y are calculated to guarantee that at the end of the PWM period the current reaches the I^* value. In this case, the system of two nonlinear equations (5.17), (3.3) and (3.4) has to be solved.

Equations are the same as for I^* calculation, but at the beginning of the PWM period, the current waveform starts not from I^*, but from the measured value I_{st}.

5.2.2.3 Validation of d_x, d_y

Calculated duty cycles d_x, d_y have to be verified. The following set of checks has to be done to ensure that the selected current waveform is feasible:

1. $d_x > 0$, $d_y > 0$;
2. $d_x + d_y \leq 1$;
3. Calculated current at the end of each section must be positive (or negative in reverse power flow);
4. In each section of the current waveform that has DCM mode, the time to reach zero current has to be smaller than the section itself.

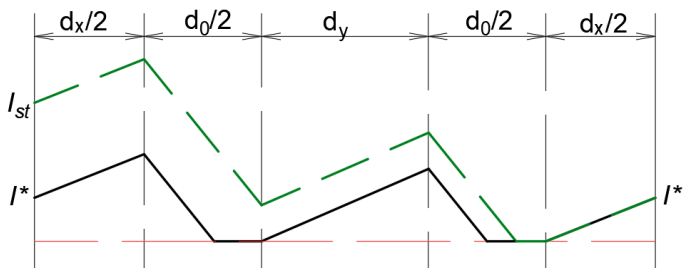

Figure 5.6: Fault tolerance capabilities during DCM operation: expected I_{out} (black), real I_{out} (green) given not expected I_{st}

If all checks are passed, calculated duty cycles can be used in the next PWM period. If not, the procedure must be repeated for the next current waveform.

5.2.3 Fault tolerance

Output current can still be controlled in DCM even if output current is not measured. It can be achieved if calculated duty cycles from the first step (Calculation of I^*) of the calculation sequence are preserved and the second step is skipped. In this case output current will converge naturally to DCM zone in both direct and reference power flow even if initial current value is not correct (Fig. 5.6). In transients input current THD is going to be higher, however in steady state performance has to be identical comparing to normal operation.

5.3 Capacitor voltage control

A PI voltage controller is adopted to regulate the output capacitor voltage. Diagram of the converter and control system is presented in Fig. 5.7. The controller equations are

$$\begin{aligned} I_{ref} &= K_p \widetilde{V}_{cap} + X_v \\ \dot{X}_v &= K_i \widetilde{V}_{cap} \end{aligned} \tag{5.18}$$

where $\widetilde{V}_{cap} = V_{ref} - V_{cap}$ is capacitor voltage error, V_{ref} is the capacitor voltage reference and K_p and K_i are proportional and integral gain respectively.

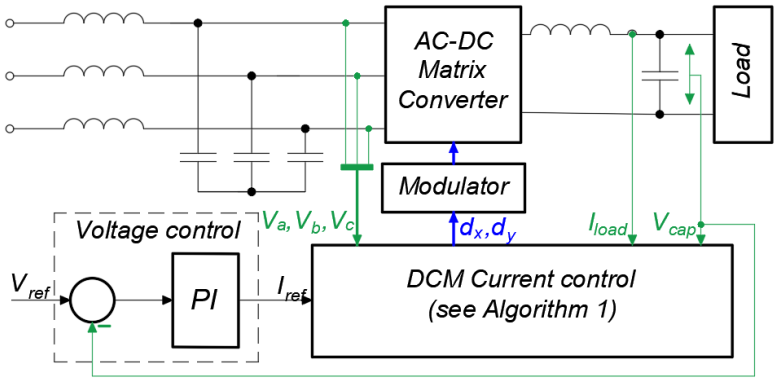

Figure 5.7: Diagram of the converter and control system

5.4 Inductance estimation

Inductance is the only parameter that the proposed algorithm uses for duty cycle calculation. It can be easily estimated online when working in DCM by minimizing a cost function

$$J = (L(f_{I^*}(d_x, d_y) - I_m))^2 \tag{5.19}$$

where $f_{I^*}(d_x, d_y)$ is a function that describes the output current shape after the last DCM zone up to the I_{end} value; I_m is the current measured at the start of the PWM cycle. The function is different for every current case. For current case 1, described in the subsections above, the function corresponds to (5.17).

After simplification and gradient calculation, the parameter estimation law for every current case is as follows.

$$\dot{\hat{L}} = \begin{cases} \gamma I_m(0.5\Delta V_x d_x T_s - I_m \hat{L}) & \text{if case} = 1, 2, 4 \\ \gamma I_m(\Delta V_y d_y T_s + 0.5\Delta V_0 d_0 T_s & \\ \quad +0.5\Delta V_x d_x T_s - I_m \hat{L}) & \text{if case} = 3 \\ \gamma I_m(0.5\Delta V_0 d_0 T_s & \\ \quad +0.5\Delta V_y d_y T_s - I_m \hat{L}) & \text{if case} = 5 \end{cases} \tag{5.20}$$

where γ is a tuning gain, $\Delta V_0, \Delta V_x, \Delta V_y$ are instant output voltages applied to the load

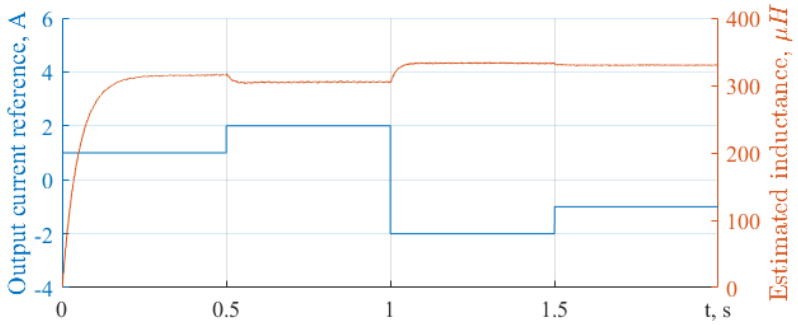

Figure 5.8: Experimental results for inductance estimation given presented output current trajectory

in one PWM cycle and are calculated as

$$\begin{aligned} \Delta V_1 &= V_a - V_b - V_{cap} \\ \Delta V_2 &= V_b - V_c - V_{cap} \\ \Delta V_3 &= V_a - V_c - V_{cap} \\ \Delta V_0 &= -V_{cap} \end{aligned} \tag{5.21}$$

In (5.20), duty cycles and current cases calculated for the previous cycle are used for computation. Higher values of γ results in a faster but noisier inductance estimation. The tuning has been performed by try and error in order to obtain the best compromise between dynamics and noise rejection. Experimental results for inductance estimation are presented in Fig. 5.8. The output current reference is presented in the figure. The slight variation in the estimated inductance shown in the figure is due to two main factors. The first is the presence of unmodeled imperfections such as dead times, switch voltage drops, and similar nonidealities. The second is the inductor core saturation, which increases with the current amplitude.

5.5 Experimental results

In this section, the converter performance using the designed current control DCM modulator is compared with the standard voltage control modulator experimentally. Experimental setup is the same as described in the previous chapter, but output inductance value is decreased to expand DCM zone. For all the tests below $L = 0.3mH$.

Modulator performances are compared in steady state in various operational points.

Input current THD, output current ripple and losses are compared. The proposed modulator performance during transients is examined.

A "4-step commutation" approach is used to control bidirectional switch commutations [4]. In DCM, the algorithm has been slightly modified in order to permit the current flowing in only one direction, according to the power flow.

5.5.1 Real time calculation of the duty cycles

The modulation approach presented in the previous section requires solving systems of nonlinear equations in real time. For this purpose, the Newton-Raphson algorithm is utilized. For realization of the algorithm in C language, the library [5] is used.

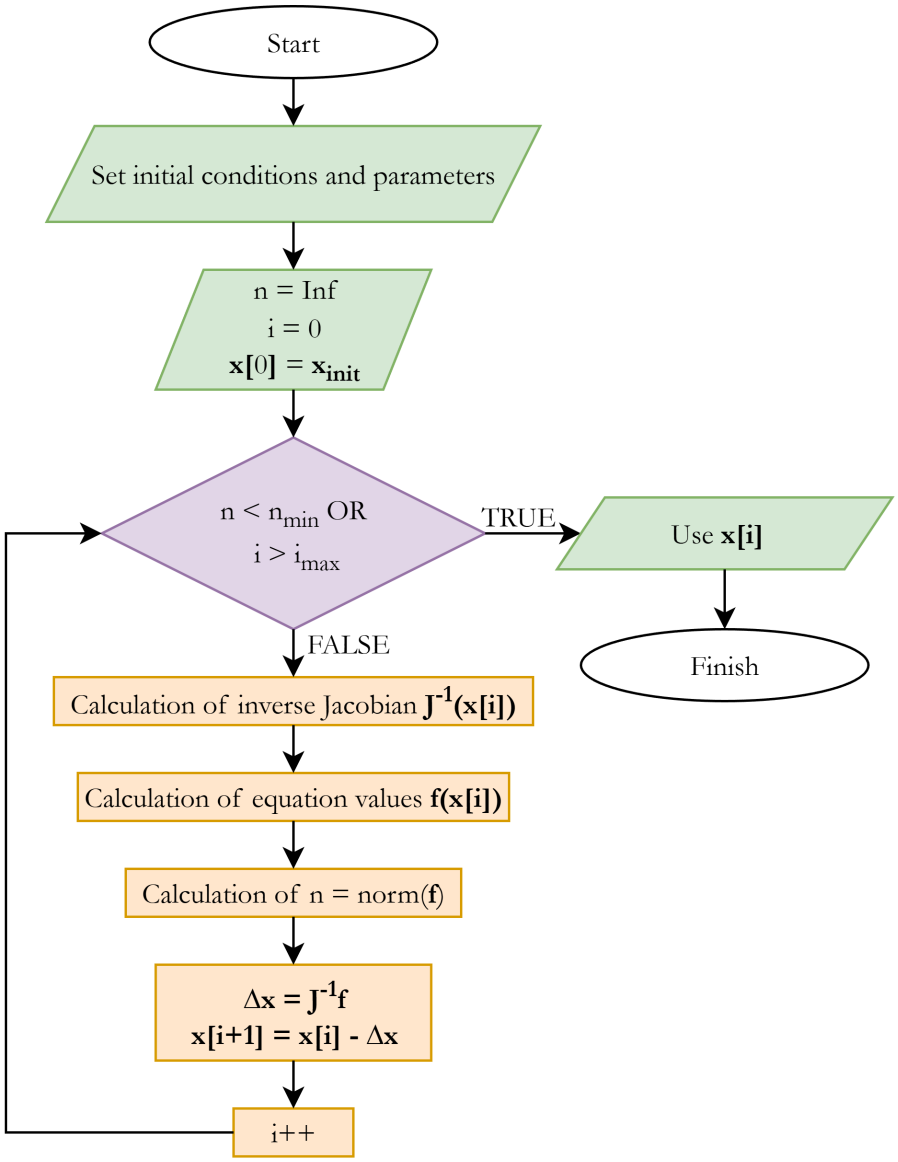

Figure 5.9: Block diagram of Newton-Raphson method

As was mentioned in the previous section, duty cycles are calculated in two stages: I^* calculation and d_x, d_y calculation. If presented equations are solved directly, when I^* calculation would require solving system of three equations, while d_x, d_y calculation - system of two equations. For real time operation, it is necessary to reduce amount of iterations as much as possible, and one of the most effective ways to do it is to reduce order of the systems of equations. Therefore, before translating equations to C, they are combined and simplified. For Case 1 of the waveform it is done by substituting (5.17) into (5.15), (5.16). After simplifications are made, I^* requires solving a system of two equations, d_x, d_y - one nonlinear equation.

Newton-Raphson algorithm requires also calculation of Jacobians of the equations. They are also preliminary calculated and inverted to ease computation burden. Block diagram of Newton-Raphson algorithm is presented in Fig. 5.9. Function $norm()$ in the diagram is L2 norm. Function $\boldsymbol{f}$ and Jacobian $\boldsymbol{J}$ are derived separately for each case and stage. After calculation, variable $\boldsymbol{x}$ is used to calculate d_x, d_y or I^* depending on the stage. Generally algorithm iteratively calculates $\boldsymbol{x}$ so that

$$\boldsymbol{f}(\mathrm{x}) = \begin{bmatrix} f_0(x_0, x_1, \ldots, x_n) \\ f_1(x_0, x_1, \ldots, x_n) \\ \vdots \\ f_n(x_0, x_1, \ldots, x_n) \end{bmatrix} = 0 \tag{5.22}$$

Jacobians are calculates as

$$\boldsymbol{J}(\boldsymbol{x}) = \frac{\partial \boldsymbol{f}(\boldsymbol{x})}{\partial \boldsymbol{x}} = \begin{bmatrix} \frac{\partial f_0}{\partial x_0} & \frac{\partial f_0}{\partial x_1} & \cdots & \frac{\partial f_0}{\partial x_n} \\ \frac{\partial f_1}{\partial x_0} & \frac{\partial f_1}{\partial x_1} & \cdots & \frac{\partial f_1}{\partial x_n} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial f_n}{\partial x_0} & \frac{\partial f_n}{\partial x_1} & \cdots & \frac{\partial f_n}{\partial x_n} \end{bmatrix} \tag{5.23}$$

Below details of implementation of the proposed algorithm using Newton-Raphson method are presented.

5.5.1.1 Stage 1. I^* calculation

The system of equations (5.17), (5.15), and (5.16) is simplified and solved for $\boldsymbol{x} = [d_x, d_y]$. The function is defined as $\boldsymbol{f} = [f_0, f_1]$. For the current Case 1, f_0 is given by

$$f_0(d_x, d_y) = -\frac{2I_{ref}\, k_{d_0} + d_x^2 k_{d_x}^2 T_s + d_y^2 k_{d_y}^2 T_s - d_x^2 k_{d_0} k_{d_x} T_s - d_y^2 k_{d_0} k_{d_y} T_s}{2k_{d_0}} \tag{5.24}$$

A complete generalization for d_x and d_y cannot be achieved in the calculation of f_1, since equations (3.3) and (3.4) depend directly on the input voltages. The basic form of the equation is

$$f_1(d_x, d_y) = V_a I_c - V_c I_a \tag{5.25}$$

The calculation of currents I_c and I_a depends on the pair of duty cycles used. This pair generally depends on the input voltage angle and the modulation index.

If $d_x = d_1, d_y = d_2$:

$$\begin{aligned} I_a &= I_x \\ I_c &= -I_y \end{aligned} \tag{5.26}$$

If $d_x = d_2, d_y = d_1$:

$$\begin{aligned} I_a &= I_y \\ I_c &= -I_x \end{aligned} \tag{5.27}$$

If $d_x = d_3, d_y = d_1$:

$$\begin{aligned} I_a &= I_x + I_y \\ I_c &= -I_x \end{aligned} \tag{5.28}$$

If $d_x = d_3, d_y = d_2$:

$$\begin{aligned} I_a &= I_x \\ I_c &= -I_x - I_y \end{aligned} \tag{5.29}$$

Currents I_x and I_y depend on the current waveform case. For current Case 1, they are calculated as

$$\begin{aligned} I_x &= \frac{1}{2} d_x^2 k_{d_x} T_s \\ I_y &= \frac{1}{2} d_y^2 k_{d_y} T_s \end{aligned} \tag{5.30}$$

Jacobian matrix is defiend as

$$\boldsymbol{J}(\boldsymbol{x}) = \frac{\partial \boldsymbol{f}(\boldsymbol{x})}{\partial \boldsymbol{x}} = \begin{bmatrix} \frac{\partial f_0}{\partial d_x} & \frac{\partial f_0}{\partial d_y} \\ \frac{\partial f_1}{\partial d_x} & \frac{\partial f_1}{\partial d_y} \end{bmatrix} \tag{5.31}$$

The derivatives $\frac{\partial f_0}{\partial d_x}$ and $\frac{\partial f_0}{\partial d_y}$ are derived directly from f_0. For current Case 1 they are

$$\begin{aligned} \frac{\partial f_0}{\partial d_x} &= \frac{d_x k_{d_x} (k_{d_0} - k_{d_x}) T_s}{k_{d_0}} \\ \frac{\partial f_0}{\partial d_y} &= \frac{d_y k_{d_y} (k_{d_0} - k_{d_y}) T_s}{k_{d_0}} \end{aligned} \tag{5.32}$$

The derivatives $\frac{\partial f_1}{\partial d_x}$ and $\frac{\partial f_1}{\partial d_y}$ are calculated based on (5.25):

$$\begin{aligned} \frac{\partial f_1}{\partial d_x} &= V_a \frac{\partial I_c}{\partial d_x} - V_c \frac{\partial I_a}{\partial d_x} \\ \frac{\partial f_1}{\partial d_y} &= V_a \frac{\partial I_c}{\partial d_y} - V_c \frac{\partial I_a}{\partial d_y} \end{aligned} \tag{5.33}$$

The derivatives $\frac{\partial I_c}{\partial d_x}$ and $\frac{\partial I_a}{\partial d_x}$ are calculated based on (5.26), (5.27), (5.28), and (5.29). The derivatives for each case are calculated below.

If $d_x = d_1, d_y = d_2$:

$$\begin{aligned}
\frac{\partial I_a}{\partial d_x} &= \frac{\partial I_x}{\partial d_x}, \\
\frac{\partial I_a}{\partial d_y} &= \frac{\partial I_x}{\partial d_y}, \\
\frac{\partial I_c}{\partial d_x} &= -\frac{\partial I_y}{\partial d_x}, \\
\frac{\partial I_c}{\partial d_y} &= -\frac{\partial I_y}{\partial d_y}
\end{aligned} \tag{5.34}$$

If $d_x = d_2, d_y = d_1$:

$$\begin{aligned}
\frac{\partial I_a}{\partial d_x} &= \frac{\partial I_y}{\partial d_x}, \\
\frac{\partial I_a}{\partial d_y} &= \frac{\partial I_y}{\partial d_y}, \\
\frac{\partial I_c}{\partial d_x} &= -\frac{\partial I_x}{\partial d_x}, \\
\frac{\partial I_c}{\partial d_y} &= -\frac{\partial I_x}{\partial d_y}
\end{aligned} \tag{5.35}$$

If $d_x = d_3, d_y = d_1$:

$$\begin{aligned}
\frac{\partial I_a}{\partial d_x} &= \frac{\partial (I_x + I_y)}{\partial d_x}, \\
\frac{\partial I_a}{\partial d_y} &= \frac{\partial (I_x + I_y)}{\partial d_y}, \\
\frac{\partial I_c}{\partial d_x} &= -\frac{\partial I_x}{\partial d_x}, \\
\frac{\partial I_c}{\partial d_y} &= -\frac{\partial I_x}{\partial d_y}
\end{aligned} \tag{5.36}$$

If $d_x = d_3, d_y = d_2$:

$$\begin{aligned}
\frac{\partial I_a}{\partial d_x} &= \frac{\partial I_x}{\partial d_x}, \\
\frac{\partial I_a}{\partial d_y} &= \frac{\partial I_x}{\partial d_y}, \\
\frac{\partial I_c}{\partial d_x} &= -\frac{\partial (I_x + I_y)}{\partial d_x}, \\
\frac{\partial I_c}{\partial d_y} &= -\frac{\partial (I_x + I_y)}{\partial d_y}
\end{aligned} \tag{5.37}$$

For current Case 1, $\frac{\partial I_x}{\partial d_x}$, $\frac{\partial I_x}{\partial d_y}$, $\frac{\partial I_y}{\partial d_x}$, $\frac{\partial I_y}{\partial d_y}$ are calculated from (5.30) as

$$\begin{aligned}
\frac{\partial I_x}{\partial d_x} &= d_x k_{d_x} T_s \\
\frac{\partial I_x}{\partial d_y} &= 0 \\
\frac{\partial I_y}{\partial d_x} &= 0 \\
\frac{\partial I_y}{\partial d_y} &= d_y k_{d_y} T_s
\end{aligned} \tag{5.38}$$

Inverse Jacobian is calculated as

$$\begin{aligned}
\boldsymbol{J}^{-1}(\boldsymbol{x}) &= \frac{1}{\det(\boldsymbol{J}(\boldsymbol{x}))} \begin{bmatrix} \frac{\partial f_1}{\partial d_y} & -\frac{\partial f_0}{\partial d_y} \\ -\frac{\partial f_1}{\partial d_x} & \frac{\partial f_0}{\partial d_x} \end{bmatrix}, \\
\det(\boldsymbol{J}(\boldsymbol{x})) &= \frac{\partial f_0}{\partial d_x}\frac{\partial f_1}{\partial d_y} - \frac{\partial f_0}{\partial d_y}\frac{\partial f_1}{\partial d_x}
\end{aligned} \tag{5.39}$$

Once $\boldsymbol{x} = [d_x, d_y]$ is calculated, I^* for current case 1 is derived as

$$I^* = \frac{1}{2} k_{d_x} d_x T_s \tag{5.40}$$

After I^* is calculated, the second stage can be started.

5.5.1.2 Stage 2. d_x, d_y calculation

After simplification, the calculation of d_x and d_y requires solving a single nonlinear equation. The vector of unknown variables is defined as $\boldsymbol{x} = d_y$. The value of d_x can be calculated directly. For current Case 1, the equation is given by

$$d_x = \frac{2I^*}{k_{d_x} T_s} \tag{5.41}$$

The function f_0 is calculated in the same way as $f_1(d_y)$ in Stage 1. Equations (5.25)-(5.29) are valid in this case. For Case 1, I_x and I_y are given by

$$
\begin{aligned}
I_x &= \frac{I^* \left(I_{st} + I^*\right)}{k_{d_x} T_s}, \\
I_y &= \frac{1}{2} d_y^2 k_{d_y} T_s
\end{aligned}
\tag{5.42}
$$

The Jacobian for f_0 is the same as $\frac{\partial f_1}{\partial d_y}$ in (5.33). The derivatives $\frac{\partial I_c}{\partial d_y}$ and $\frac{\partial I_a}{\partial d_y}$ are defined in (5.34)–(5.37), depending on the duty cycles used. The derivatives $\frac{\partial I_x}{\partial d_y}$ and $\frac{\partial I_y}{\partial d_y}$ are calculated from (5.42) as

$$
\begin{aligned}
\frac{\partial I_x}{\partial d_y} &= 0, \\
\frac{\partial I_y}{\partial d_y} &= d_y k_{d_y}
\end{aligned}
\tag{5.43}
$$

Inversion of Jacobian in this case is $J^{-1} = \frac{1}{J}$. Once $\boldsymbol{x} = d_y$ is determined, d_y is determined from (5.41).

Functions and its derivatives for other current cases are presented in Appendix B.

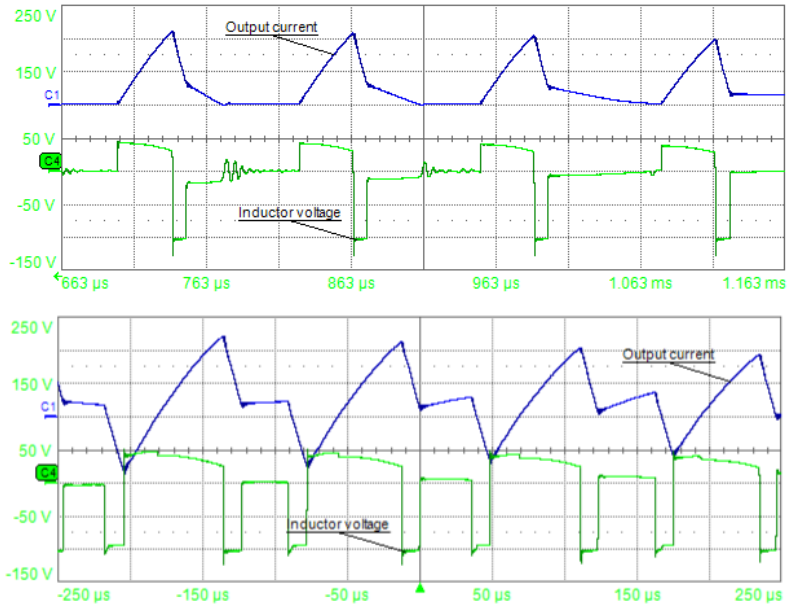

Figure 5.10: Experimental waveforms of inductor voltage in CCM and DCM

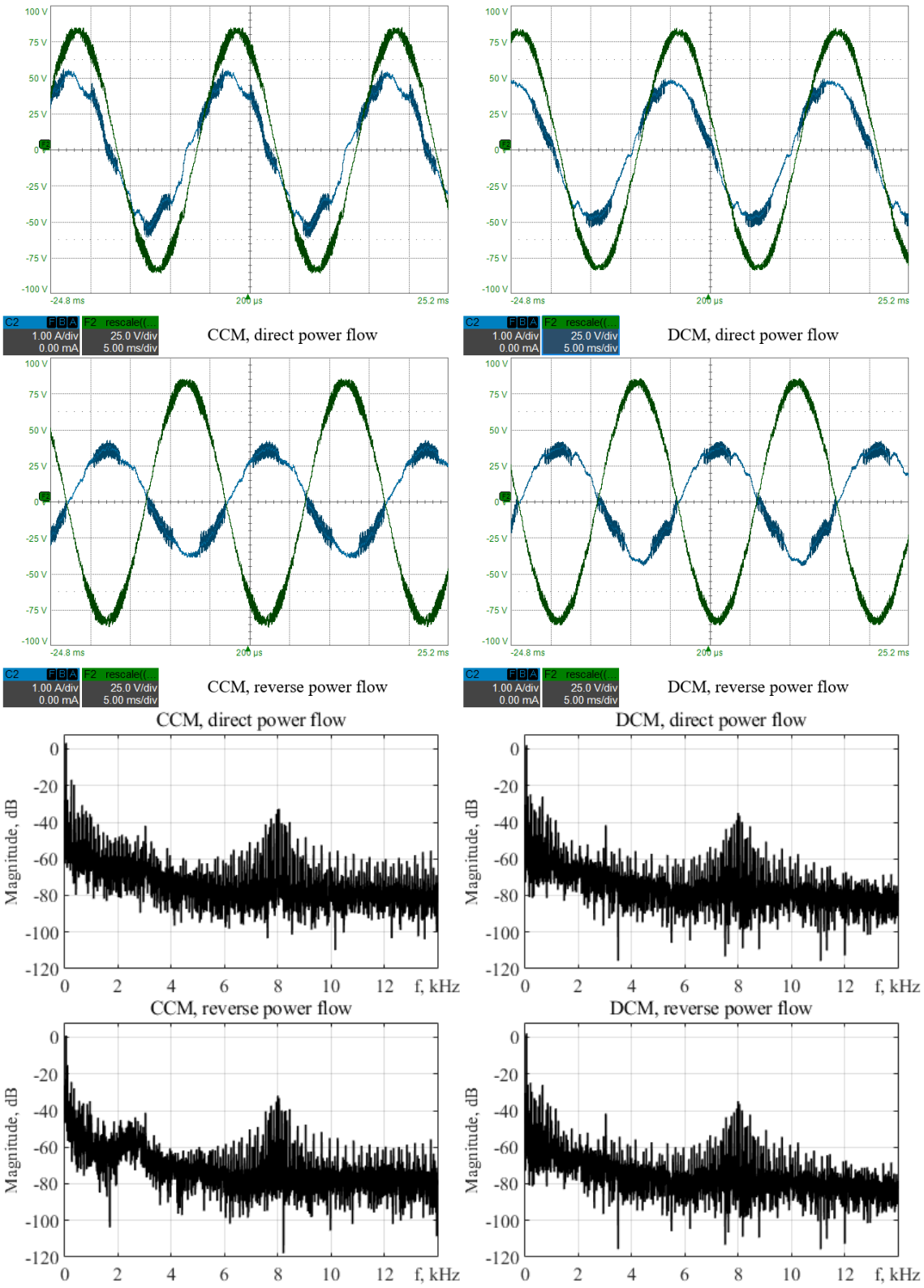

Figure 5.11: Input current and voltage in direct and reverse power flow, using proposed DCM modulation and standard CCM modulation.FFT for input current in each mode. Output current I_{out} is 2A

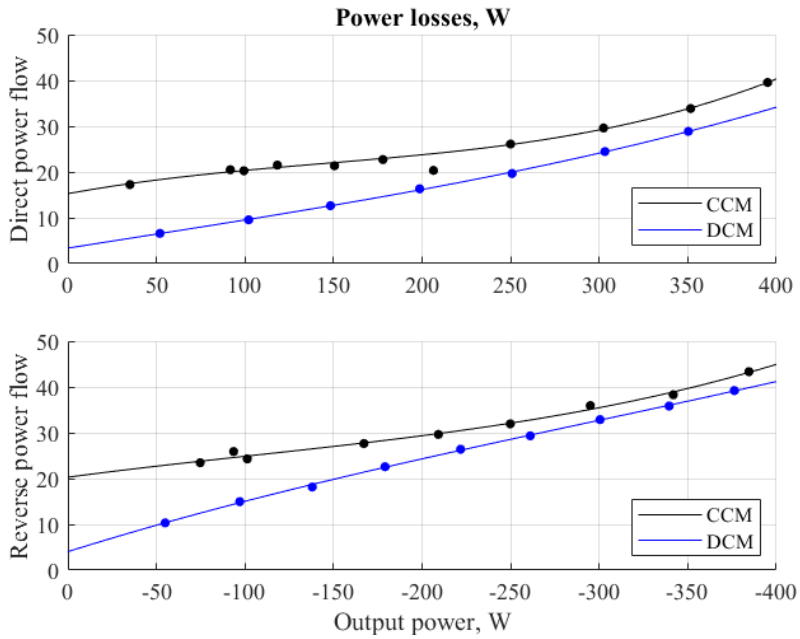

Figure 5.12: Experimental power losses comparison in CCM and DCM for various output power levels

5.5.2 Experiments description

Given a switching frequency of 8kHz, the real-time task computation time should not exceed 125μs. The average computation time of the proposed DCM algorithm is 23.5μs, which is well inside of the limit. While average computation time in CCM is 6μs. Computation is done by checking real-time timer value before and after execution of a real time task.

The power supply voltage is $100V$ for every test. In order to control the output current, a PI controller is used when the standard voltage modulator is used. Experimental waveforms of inductor voltage and output current (Fig. 5.1) are presented in Fig. 5.10.

Input phase current and voltage waveforms with the standard and DCM modulator are shown in Fig. 5.11. The output current is $2A$. The FFT of the input current for each operating mode is also shown. The capacitive behavior observed in the figures is caused by the input filter capacitor. At higher power levels, the power factor approaches unity. In this thesis, only unity power factor operation is considered, neglecting the influence of the input filter, whose effect is significant only in the low-power region. Losses comparison is presented in Fig. 5.12. Input power is calculated based on two input phase-to-phase voltages and two input phase current measurements. Output power is calculated based

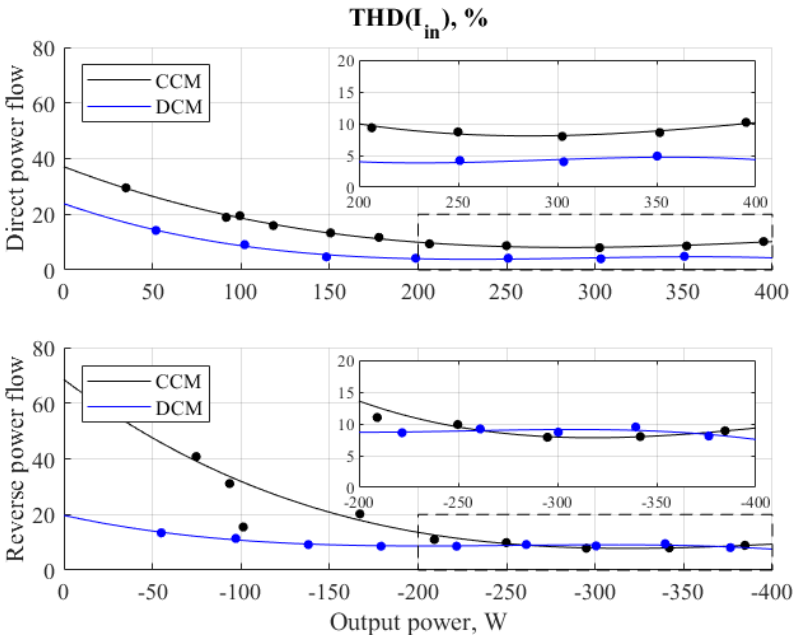

Figure 5.13: Experimental input current THD comparison in CCM and DCM for various output power levels

on I_{out} and V_{cap} measurements. All acquisitions are done with the oscilloscope. Benefits of the DCM modulator are much higher at lower power since the output current is constantly in the DCM zone. At higher power levels, the output current moves out of the DCM zone, and as a result the losses are approximately equal in both modulation methods. Input current THD comparison is presented in Fig. 5.13. The DCM modulator shows superior performance in both power flows, especially in the low power region. For power levels above $200W$ I_{in} THD is approximately 5% for DCM, and 10% for CCM in direct power flow. In reverse power flow THD is 10% for both modulation methods. It can be explained by the fact that the output current ripple in DCM is much lower, and as a result, influence of output inductance saturation on the THD is lower. THD of output current is also compared. It is computed in the following way:

$$THD_{DC}(I_{out}) = \frac{\sqrt{\sum_{n=1}^{120} I_n^2}}{I_{dc}} \tag{5.44}$$

where I_{dc} is a DC component of I_{out}. The maximum harmonic is the 120th ($6kHz$), since the goal is to evaluate the presence of low-frequency harmonics in I_{out}, but not switching harmonics.

Comparison results are presented in Fig. 5.14. Similarly to input THD, output current

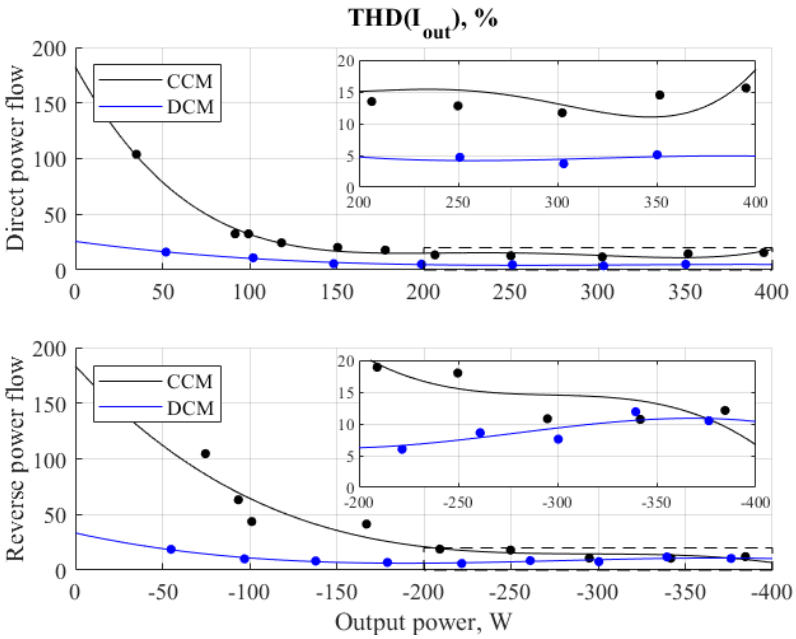

Figure 5.14: Experimental output current THD comparison in CCM and DCM for various output power levels

ripple in DCM in the low power zone is much smaller. In direct power flow, for power levels above $200W$ I_{in} THD is approximately 5% for DCM, and 12% for CCM. In reverse power flow, THD is 7% for DCM and 15% for CCM.

Figs. 5.15 and 5.16 present the performance of the proposed modulator under transient conditions. In the modulator, the current is expected to reach its reference in one switching cycle if (3.2) is fulfilled. Depending on the power flow direction and conduction mode, the 4-step switching sequence is different. The algorithm, in any point of operation, stays in one of three states: CCM operation, DCM direct power flow operation

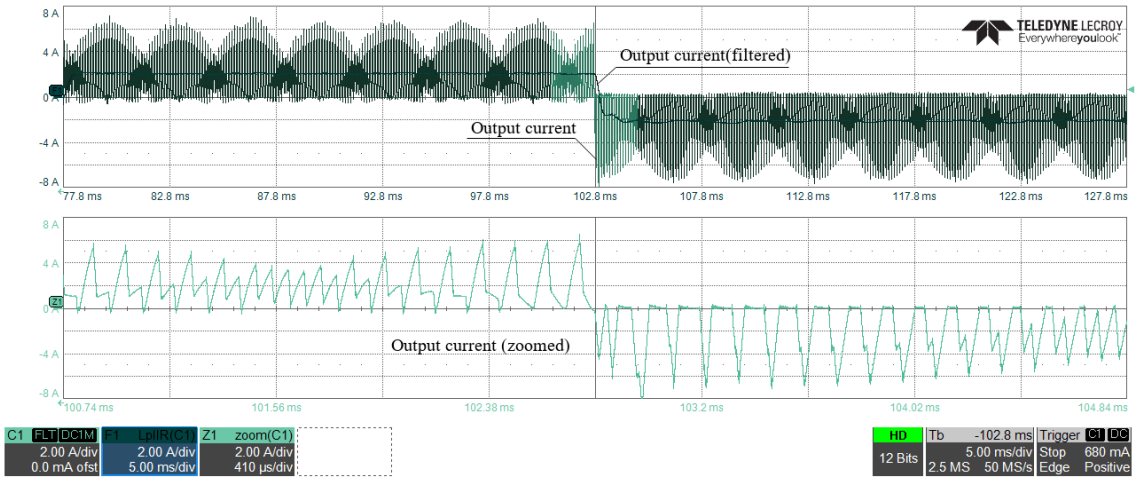

Figure 5.15: Transient in DCM. Output current, $I_{out} = 2 \rightarrow -2A$

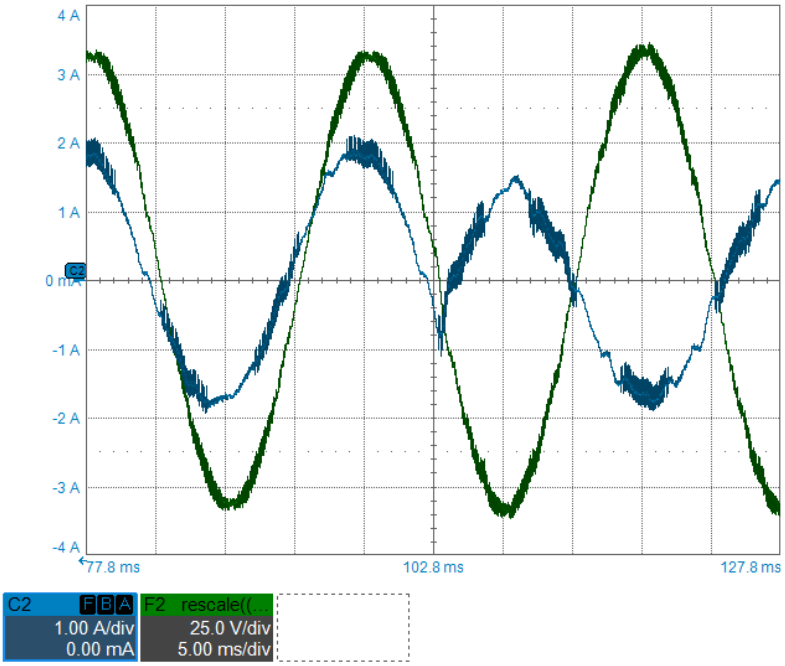

Figure 5.16: Transient in DCM. Input current and voltage, $I_{out} = 2 \rightarrow -2A$

(DCM1), and DCM reverse power flow operation (DCM2). Assuming that V_{cap} is always positive, the power flow direction is determined depending on the sign of I_{ref}. In Figs. 5.15 and 5.16, the converter initially operates in the DCM1 state. Once the sign of I_{ref} changes, the converter state changes to CCM. After one cycle, if (3.2) is fulfilled, the converter state changes to DCM2.

In order to test the performance of the system in capacitor voltage control mode, the following experimental test is proposed: at $t = 0$s, V_{ref} steps to 100V, and at $t = 0.06$s, V_{ref} steps to 75V. The voltage PI loop gains are set to $K_p = 0.2$ and $K_i = 16$. The test is performed with the output voltage supply disconnected from the load. The load resistance is set to 35Ω. Experimental results are presented in Fig. 5.17 and show a fast transient response.

5.6 Chapter Summary

This chapter presented a novel modulation scheme for the AC–DC matrix-based buck converter, enabling efficient operation in Discontinuous Conduction Mode (DCM). The proposed approach was investigated and compared against standard Continuous Conduction Mode (CCM) operation to evaluate its impact on power quality and converter

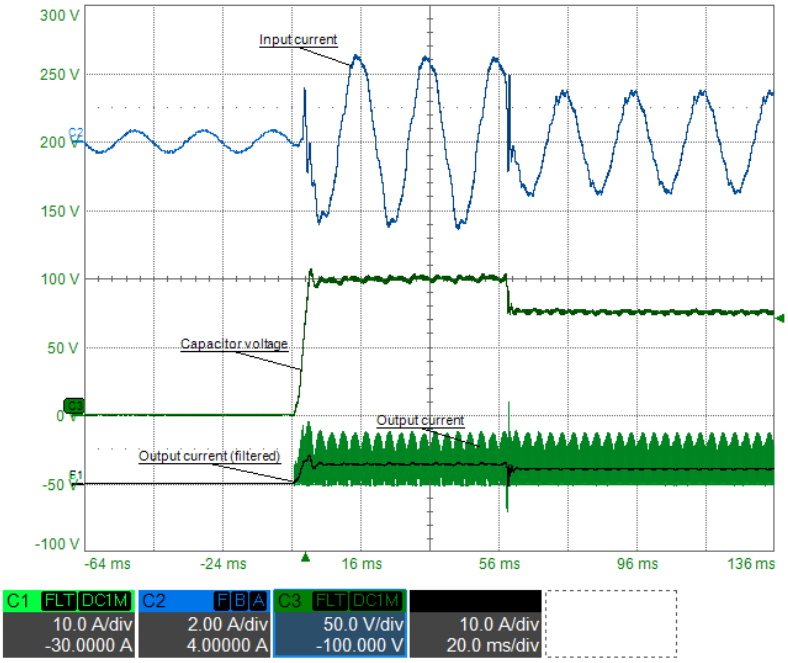

Figure 5.17: System performance in voltage control mode

efficiency.

The analysis and experimental results demonstrated that operating in DCM improves the Total Harmonic Distortion (THD) of both input and output currents. These improvements are primarily attributed to a reduction in current ripple during both direct and reverse power flow. Furthermore, the transition to DCM modulation was shown to reduce overall power losses. performance improvements come with increased computational effort compared to CCM.

Experimental findings showed that the advantages of DCM are dependent on the load characteristics, input voltage levels, and the specific operating point of the system. In particular, the systems requiring a wide output voltage range while operating at low output currents derive the most significant benefits from this modulation strategy.

References 5

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Chapter 6:

Conclusion

This thesis investigated modulation methods and switching pattern selection for AC–DC matrix converters. Existing research on matrix converter modulation either identifies a limited set of switching patterns with favorable performance or optimizes predefined patterns to reduce output current ripple. However, none of the previously published works has conducted a comprehensive and objective investigation aimed at identifying the globally optimal switching pattern in terms of minimizing output current ripple while considering the full set of feasible patterns. One of the main challenges of such an investigation is the extremely large number of possible patterns that satisfy the fundamental operational constraints. An additional challenge arises for patterns with four or more switching states per half cycle, where further optimization is possible but manual derivation of optimization equations becomes impractical.

This thesis addresses these challenges by proposing an automated procedure for systematic pattern generation and optimization. All feasible switching patterns are evaluated one by one in order to identify those that minimize output current ripple. Since patterns with a higher number of commutations per cycle inherently exhibit lower ripple but incur higher switching losses, switching losses were explicitly taken into account in the optimization process. Furthermore, even patterns with the same number of commutations can result in different switching losses per cycle. As a result, this research presents sets of switching patterns that achieve an optimal trade-off between output current ripple and switching losses.

For the selected optimal patterns, analytical optimization was derived to enable implementation in real-time control systems. The proposed modulation strategies were experimentally validated, and the measured results closely match the analytically derived characteristics, confirming the accuracy of the proposed models and optimization approach.

The comparison discussed above evaluates the maximum output current ripple over one input voltage period for each pattern. However, further ripple reduction can be achieved by switching between different patterns within a single input voltage period. Since continuous switching between patterns is not feasible in practical systems, an optimization was performed to determine the optimal selection of one, two, or three patterns that minimizes the total output current ripple over the entire operating range. The results of this optimization are presented in the form of maps that select the appropriate pattern group based on the input voltage angle and modulation index. The resulting output current ripple is compared with standard modulation methods, including SVM and DC-SVM, at different power factors. The results demonstrate superior performance of the optimized pattern sets compared to the conventional methods.

In the final part of the thesis, an alternative modulation approach based on discontinuous conduction mode (DCM) is presented for loss reduction and performance improvement. Compared to standard continuous conduction mode (CCM) modulation methods, DCM modulation enables improved efficiency and reduced input current total harmonic distortion at low output current levels. A new current-control-based modulation method is introduced, as the direct application of standard modulation techniques in the DCM region leads to significant input current distortion. Additionally, a method for estimating the output inductance is proposed, as it is the only parameter required by the new modulator, making the approach robust to parameter variations. The proposed DCM modulation and control strategy were experimentally validated and demonstrated superior steady-state and transient performance compared to standard CCM voltage control operation.

6.1 Future work

The methodology developed in this thesis can be extended to other types of power converters that feature a large number of feasible switching patterns. Similar systematic pattern optimization frameworks could be applied to these converters to objectively identify optimal modulation strategies under various performance criteria.

Furthermore, the proposed optimization approach is not limited to output current

ripple minimization. It can be generalized to optimize other performance metrics influenced by switching pattern selection, such as input current ripple, total harmonic distortion, switching losses. Multi-objective optimization frameworks could also be investigated to balance several performance indicators simultaneously.

One promising candidate for further research is the AC–AC matrix converter. Due to the structural and control similarities between AC–DC and AC–AC matrix converters, the proposed automated pattern generation and optimization procedure can be adapted with only minor modifications. This extension would allow a comprehensive evaluation of optimal switching patterns for AC–AC conversion across different operating conditions.

Appendix A

Appendix A presents optimized maps for 4- and 5-states patterns for different power factors and set number s.

A.1 Unity power factor

Maps of 4-state patterns for $s = 1$, $s = 2$, $s = 3$ are presented in Fig. A.1, Fig. A.2 and Fig. A.3. Corresponding patterns are shown in Table A.1.

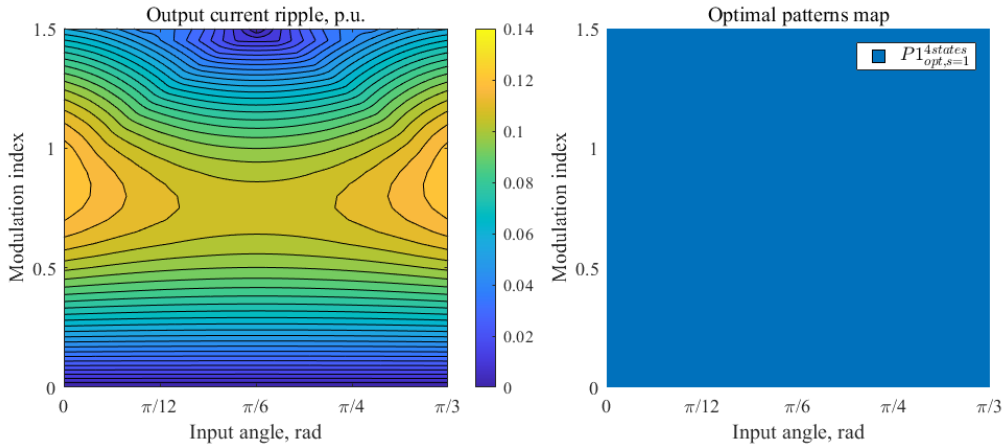

Figure A.1: Map of normalized current ripple for optimized set of 4-state patterns $s = 1$ for unity power factor

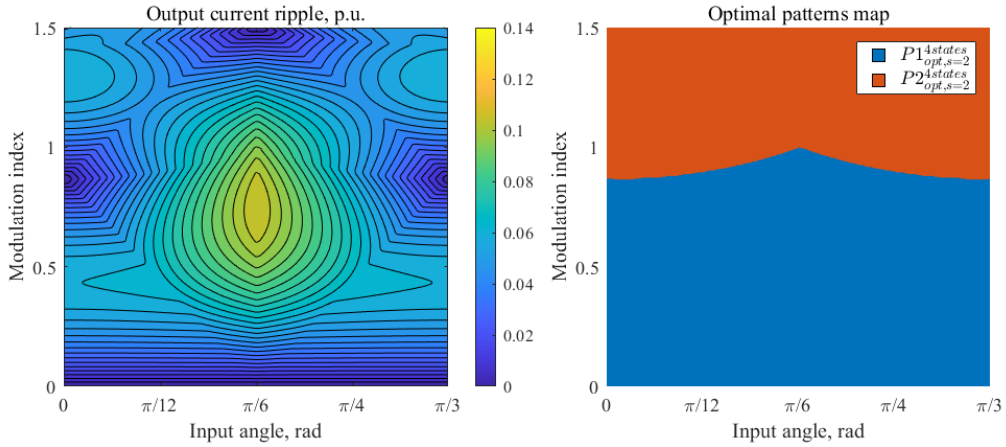

Figure A.2: Map of normalized current ripple for optimized set of 4-state patterns $s = 2$ for unity power factor

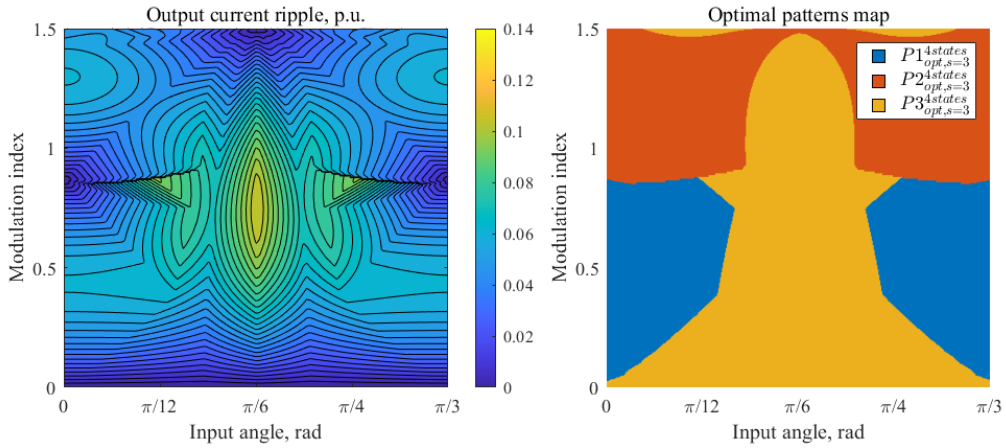

Figure A.3: Map of normalized current ripple for optimized set of 4-state patterns $s = 3$ for unity power factor

Table A.1: 4-state patterns used in optimized sets for different set number s

(a) $s = 1$

Group Number	Pattern
$P1^{4\ states}_{opt,s=1}$	$0mh0$, $m0h0$, $0hm0$ $0h0m$, $h0mh$, $h0hm$ $hm0h$, $mh0h$

(b) $s = 2$

Group Number	Patterns
$P1^{4\ states}_{opt,s=2}$	$m0lm$, $ml0m$
$P2^{4\ states}_{opt,s=2}$	$lmhl$, $lhml$, $mlhm$, $mhlm$

(c) $s = 3$

Group Number	Patterns
$P1^{4\ states}_{opt,s=3}$	$0lm0$, $l0m0$, $0ml0$ $0m0l$,$m0lm$, $m0ml$ $ml0m$, $lm0m$
$P2^{4\ states}_{opt,s=3}$	$lmhl$, $lhml$, $mlhm$, $mhlm$
$P3^{4\ states}_{opt,s=3}$	$0h0m$, $m0h0$

Maps of 5-state patterns for $s = 1$,$s = 2$,$s = 3$ are presented in Fig. A.4, Fig. A.5 and Fig. A.6. Corresponding patterns are shown in Table A.2.

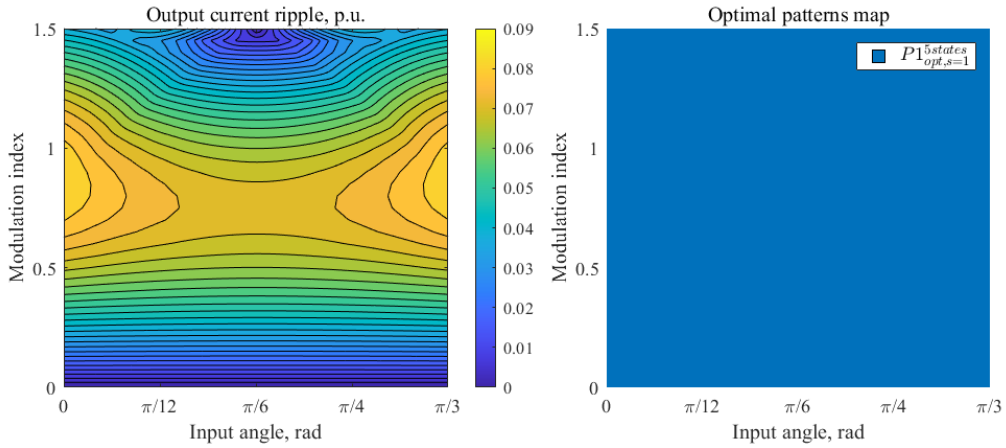

Figure A.4: Map of normalized current ripple for optimized set of 5-state patterns $s = 1$ for unity power factor

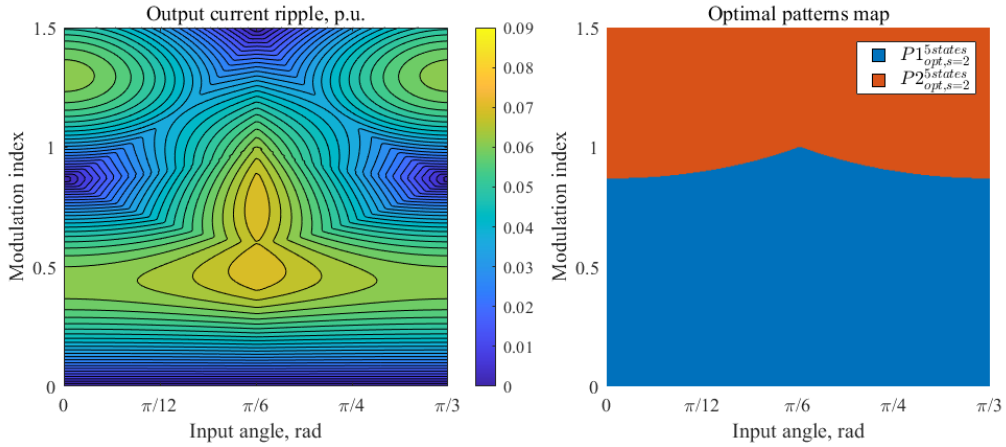

Figure A.5: Map of normalized current ripple for optimized set of 5-state patterns $s = 2$ for unity power factor

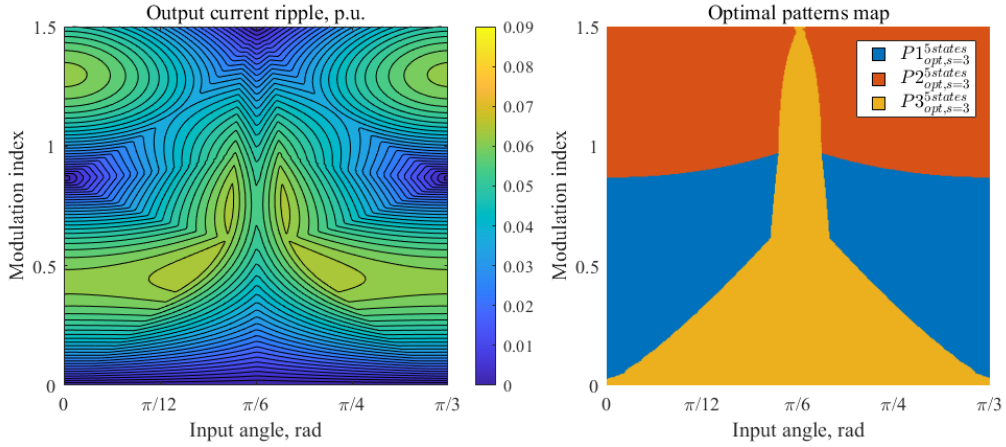

Figure A.6: Map of normalized current ripple for optimized set of 5-state patterns $s = 3$ for unity power factor

Table A.2: 4-state patterns used in optimized sets for different set number s

(a) $s = 1$

Group Number	Pattern
$P1^{5\ states}_{opt,s=1}$	$h0hm0$, $h0mh0$ $0hm0h$, $0mh0h$

(b) $s = 2$

Group Number	Patterns
$P1^{5\ states}_{opt,s=2}$	$lm0lm$, $lml0m$ $m0lml$, $ml0ml$
$P2^{5\ states}_{opt,s=2}$	$lmhlm$, $lhmlm$ $mlmhl$, $mlhml$

(c) $s = 3$

Group Number	Patterns
$P1^{5\ states}_{opt,s=3}$	$lm0lm$, $lml0m$ $m0lml$, $ml0ml$
$P2^{5\ states}_{opt,s=3}$	$lmhlm$, $lhmlm$ $mlmhl$, $mlhml$
$P3^{5\ states}_{opt,s=3}$	$h0m0h$, $m0h0m$ $0m0h0$, $0h0m0$

A.2 Power factor $\varphi = \frac{\pi}{8}\ rad$

Maps of 4-state patterns for SVM, $DC-SVM$, $s=2$, $s=3$ are presented in Fig. A.7, Fig. A.8, Fig. A.9 and Fig. A.10. Corresponding patterns are shown in Table A.3.

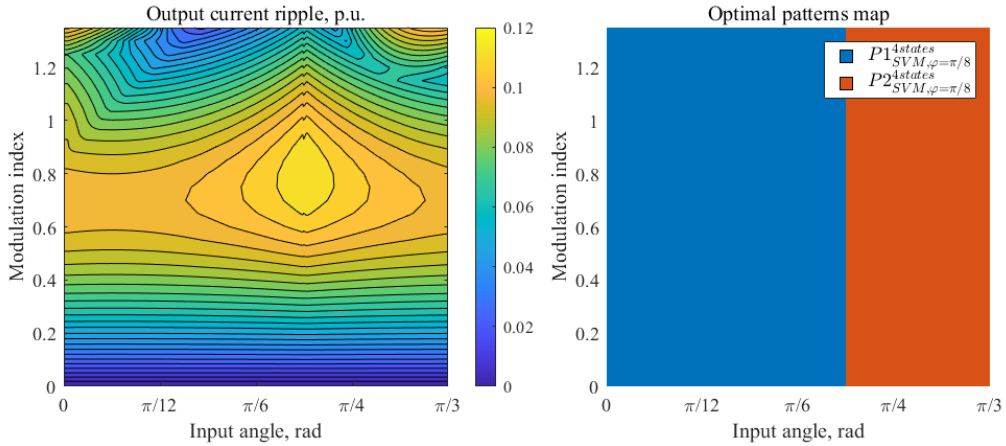

Figure A.7: Map of normalized current ripple using SVM for 4-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

Table A.3: 4-state patterns used in different modulation strategies for power factor $\varphi = \frac{\pi}{8}\ rad$

(a) SVM

Group Number	Pattern
$P1^{4\ states}_{SVM,\varphi=\pi/8}$	$0mh0$, $0hm0$
$P2^{4\ states}_{SVM,\varphi=\pi/8}$	$lh0h$, $h0hl$

(b) $DC-SVM$

Group Number	Patterns
$P1^{4\ states}_{DC-SVM,\varphi=\pi/8}$	$ml0m$, $m0lm$
$P2^{4\ states}_{DC-SVM,\varphi=\pi/8}$	$mlhm$, $mhlm$

(c) $s=2$

Group Number	Patterns
$P1^{4\ states}_{opt,s=2,\varphi=\pi/8}$	$0hm0$, $0mh0$
$P2^{4\ states}_{opt,s=2,\varphi=\pi/8}$	$lh0h$, $h0hl$

(d) $s=3$

Group Number	Patterns
$P1^{4\ states}_{opt,s=3,\varphi=\pi/8}$	$ml0m$, $m0lm$
$P2^{4\ states}_{opt,s=3,\varphi=\pi/8}$	$hmlm$, $mlmh$
$P3^{4\ states}_{opt,s=3,\varphi=\pi/8}$	$hmlh$, $hlmh$

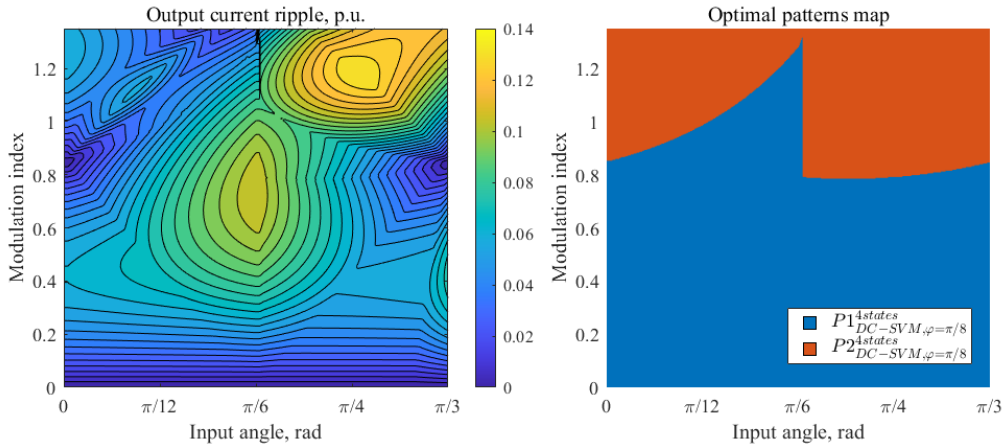

Figure A.8: Map of normalized current ripple using DC-SVM for 4-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

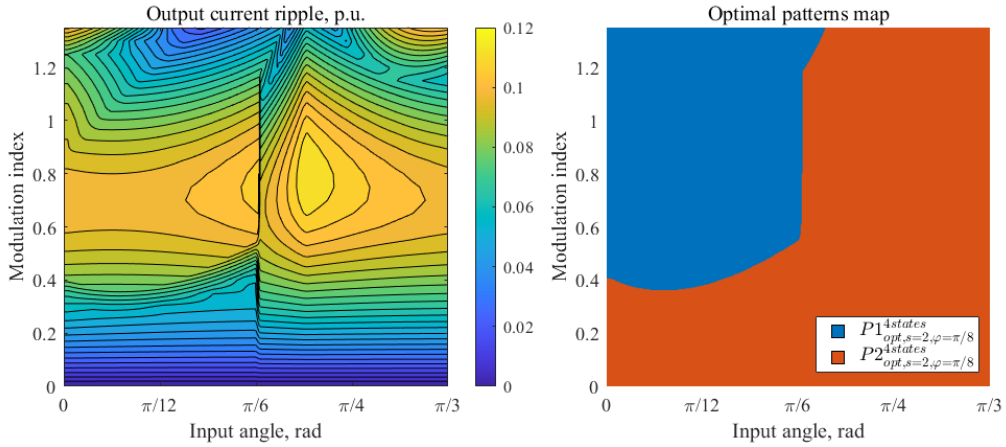

Figure A.9: Map of normalized current ripple using optimized set $s = 2$ for 4-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

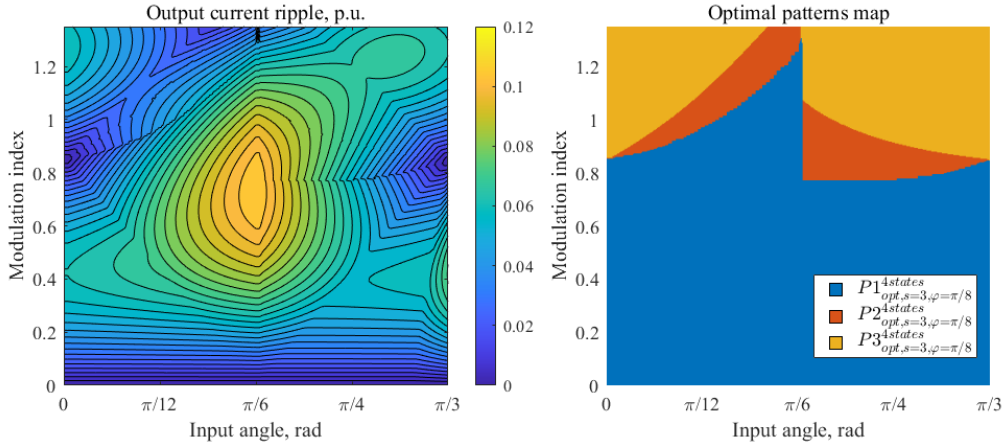

Figure A.10: Map of normalized current ripple using optimized set $s = 3$ for 4-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

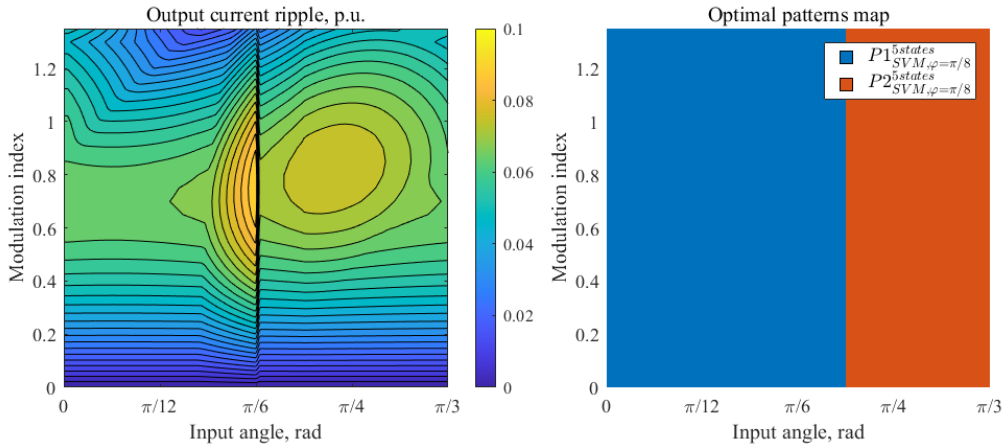

Figure A.11: Map of normalized current ripple using SVM for 5-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

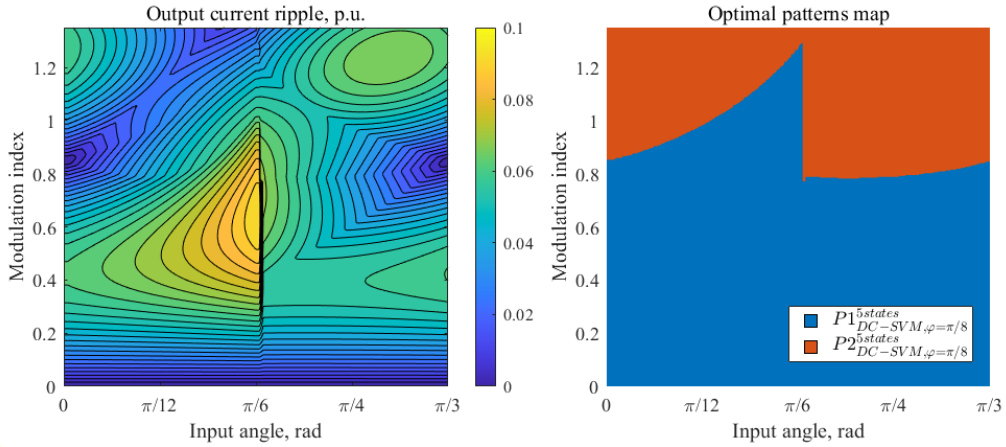

Figure A.12: Map of normalized current ripple using DC-SVM for 5-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

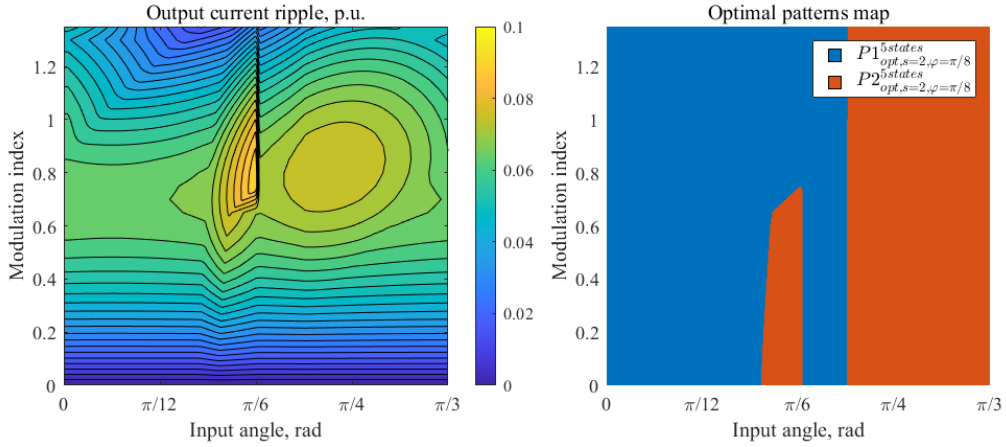

Figure A.13: Map of normalized current ripple using optimized set $s = 2$ for 5-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

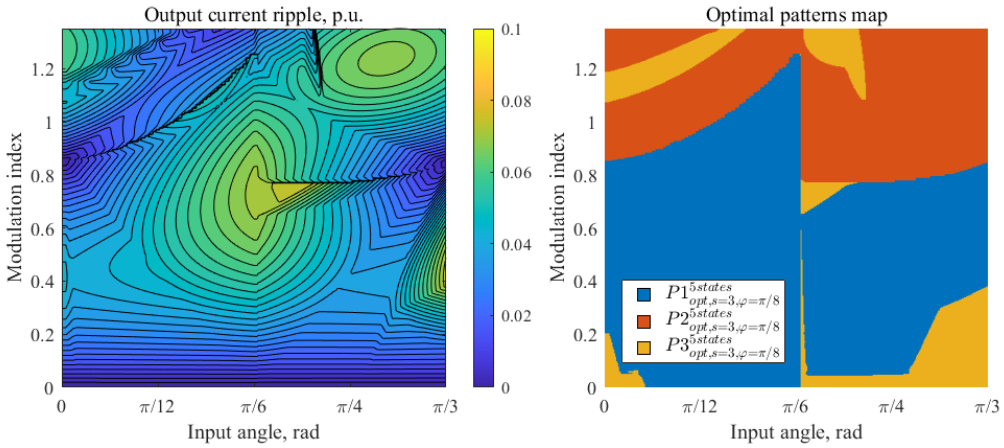

Figure A.14: Map of normalized current ripple using optimized set $s = 3$ for 5-state patterns for power factor $\varphi = \frac{\pi}{8}\ rad$

Table A.4: 5-state patterns used in different modulation strategies for power factor $\varphi = \frac{\pi}{8}\ rad$

(a) SVM

Group Number	Pattern
$P1^{5\ states}_{SVM,\varphi=\pi/8}$	$h0mh0$, $0hm0h$
$P2^{5\ states}_{SVM,\varphi=\pi/8}$	$0hl0h$, $0h0lh$ $h0lh0$, $hl0h0$

(b) $DC-SVM$

Group Number	Patterns
$P1^{5\ states}_{DC-SVM,\varphi=\pi/8}$	$lm0lm$, $lml0m$ $m0lml$, $ml0ml$
$P2^{5\ states}_{DC-SVM,\varphi=\pi/8}$	$mlhml$, $lmhlm$

(c) $s = 2$

Group Number	Patterns
$P1^{5\ states}_{opt,s=2,\varphi=\pi/8}$	$h0mh0$, $0hm0h$
$P2^{5\ states}_{opt,s=2,\varphi=\pi/8}$	$0hl0h$, $0h0lh$ $h0lh0$, $hl0h0$

(d) $s = 3$

Group Number	Patterns
$P1^{5\ states}_{opt,s=3,\varphi=\pi/8}$	$ml0m0$, $0m0lm$ $0ml0m$, $m0lm0$
$P2^{5\ states}_{opt,s=3,\varphi=\pi/8}$	$mlhml$, $lmhlm$
$P3^{5\ states}_{opt,s=3,\varphi=\pi/8}$	$0h0hm$, $mh0h0$

A.3 Power factor $\varphi = \frac{\pi}{4}\ rad$

Maps of 4-state patterns for SVM, $DC-SVM$, $s=2$, $s=3$ are presented in Fig. A.15, Fig. A.16, Fig. A.17 and Fig. A.18. Corresponding patterns are shown in Table A.5.

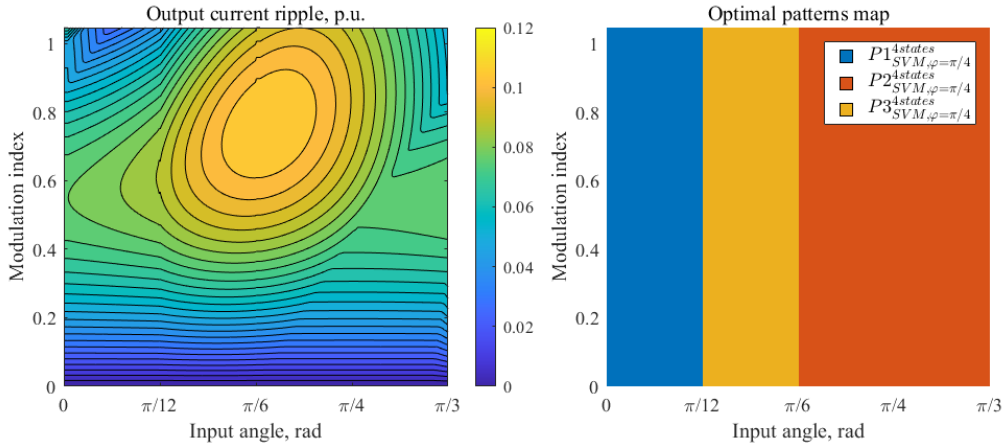

Figure A.15: Map of normalized current ripple using SVM for 4-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

Table A.5: 4-state patterns used in different modulation strategies for power factor $\varphi = \frac{\pi}{4}\ rad$

(a) SVM

Group Number	Pattern
$P1^{4\ states}_{SVM,\varphi=\pi/4}$	$0mh0$, $0m0h$, $0hm0$ $h0m0$, $m0hm$, $m0mh$ $mh0m$, $hm0m$
$P2^{4\ states}_{SVM,\varphi=\pi/4}$	$hl0h$, $h0lh$
$P3^{4\ states}_{SVM,\varphi=\pi/4}$	$m0lm$, $ml0m$

(b) $DC-SVM$

Group Number	Patterns
$P1^{4\ states}_{DC-SVM,\varphi=\pi/4}$	$l0ml$, $lm0l$
$P2^{4\ states}_{DC-SVM,\varphi=\pi/4}$	$lhml$, $lmhl$

(c) $s=2$

Group Number	Patterns
$P1^{4\ states}_{opt,s=2,\varphi=\pi/4}$	$ml0m$, $m0lm$
$P2^{4\ states}_{opt,s=2,\varphi=\pi/4}$	$lhml$, $lmhl$

(d) $s=3$

Group Number	Patterns
$P1^{4\ states}_{opt,s=3,\varphi=\pi/4}$	$ml0m$, $m0lm$
$P2^{4\ states}_{opt,s=3,\varphi=\pi/4}$	$lm0m$, $m0ml$
$P3^{4\ states}_{opt,s=3,\varphi=\pi/4}$	$lhml$, $lmhl$

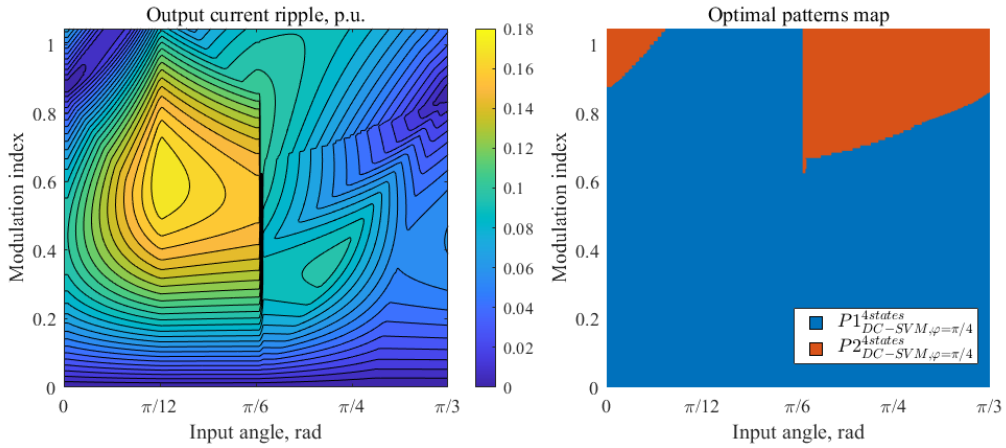

Figure A.16: Map of normalized current ripple using DC-SVM for 4-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

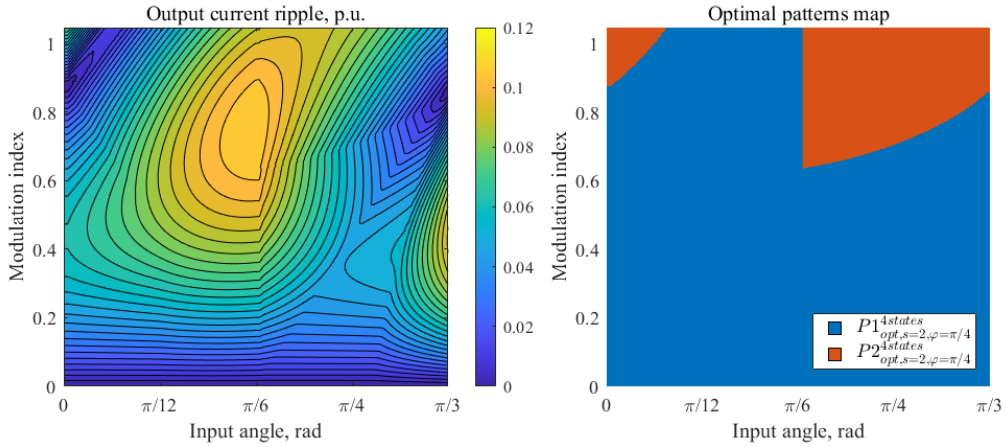

Figure A.17: Map of normalized current ripple using optimized set $s = 2$ for 4-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

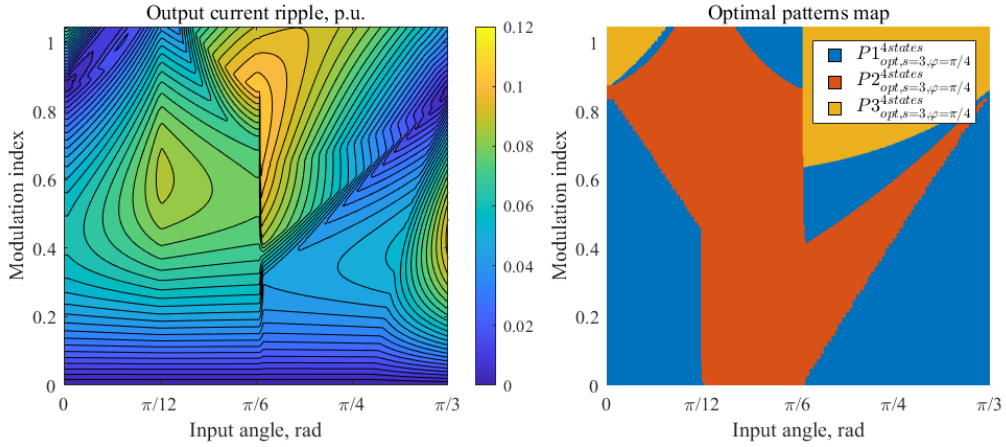

Figure A.18: Map of normalized current ripple using optimized set $s = 3$ for 4-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

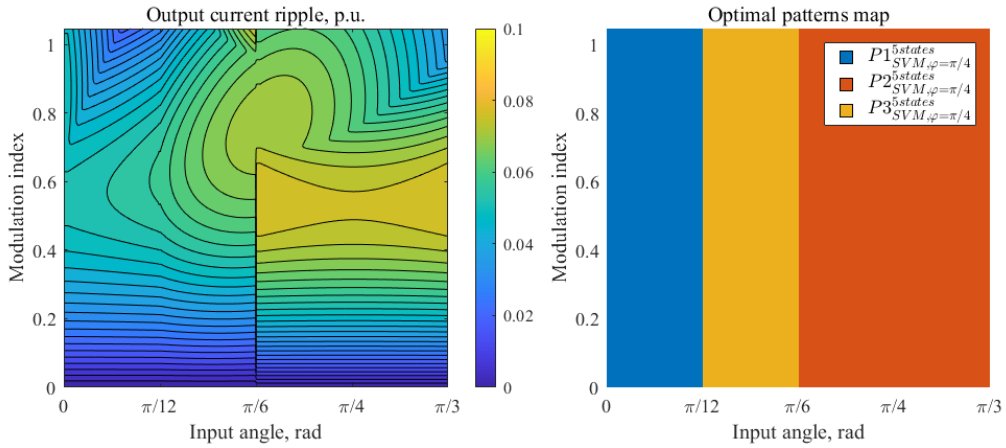

Figure A.19: Map of normalized current ripple using SVM for 5-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

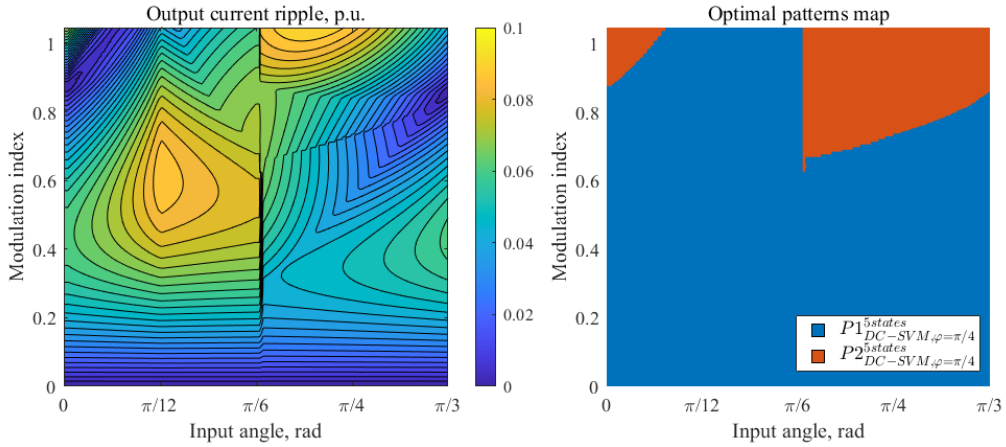

Figure A.20: Map of normalized current ripple using DC-SVM for 5-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

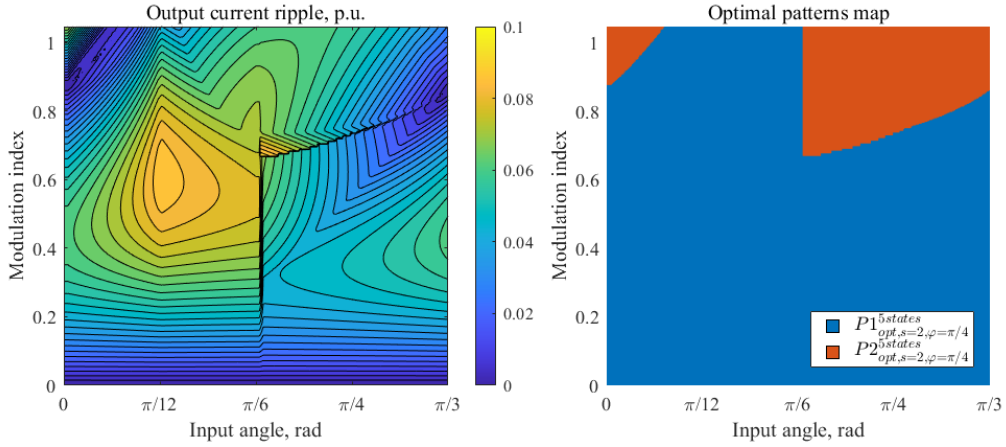

Figure A.21: Map of normalized current ripple using optimized set $s = 2$ for 5-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

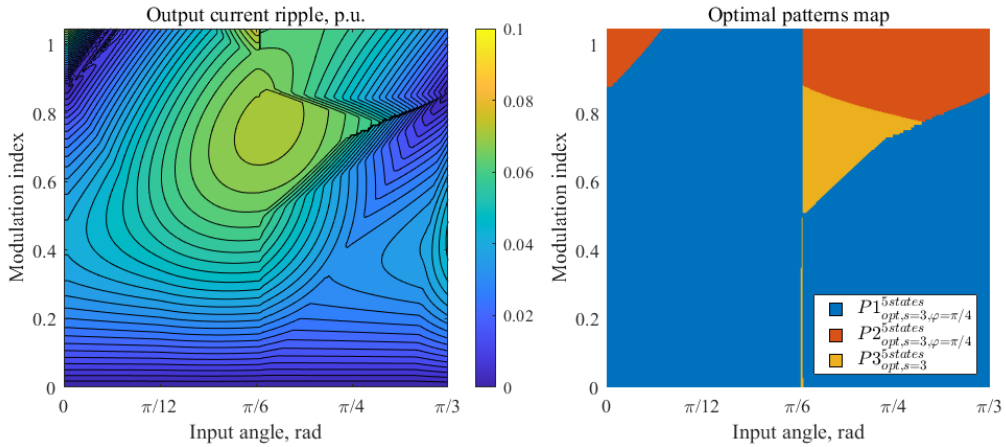

Figure A.22: Map of normalized current ripple using optimized set $s = 3$ for 5-state patterns for power factor $\varphi = \frac{\pi}{4}\ rad$

Table A.6: 5-state patterns used in different modulation strategies for power factor $\varphi = \frac{\pi}{4}\ rad$

(a) SVM

Group Number	Pattern
$P1^{5\ states}_{SVM,\varphi=\pi/4}$	$0mh0m$, $0hm0m$ $m0mh0$, $m0hm0$
$P2^{5\ states}_{SVM,\varphi=\pi/4}$	$lh0lh$, $lhl0h$ $hl0hl$, $h0lhl$
$P3^{5\ states}_{SVM,\varphi=\pi/4}$	$0ml0m$, $0m0lm$ $m0lm0$, $ml0m0$

(b) $DC-SVM$

Group Number	Patterns
$P1^{5\ states}_{DC-SVM,\varphi=\pi/4}$	$ml0ml$, $lm0lm$
$P2^{5\ states}_{DC-SVM,\varphi=\pi/4}$	$mlmhl$, $mlhml$ $lmhlm$, $lhmlm$

(c) $s = 2$

Group Number	Patterns
$P1^{5\ states}_{opt,s=2,\varphi=\pi/4}$	$ml0ml$, $lm0lm$
$P2^{5\ states}_{opt,s=2,\varphi=\pi/4}$	$hlhml$, $hlmhl$ $lhmlh$, $lmhlh$

(d) $s = 3$

Group Number	Patterns
$P1^{5\ states}_{opt,s=3,\varphi=\pi/4}$	$0ml0m$, $m0lm0$
$P2^{5\ states}_{opt,s=3,\varphi=\pi/4}$	$mhlhl$, $lhlhm$, $hlmhl$ $lhlmh$, $lhmlh$, $hmlhl$ $lmhlh$, $mlhlh$ $hlhlm$, $hlhml$
$P3^{5\ states}_{opt,s=3,\varphi=\pi/4}$	$hl0h0$, $0h0lh$ $0hl0h$, $h0lh0$

Appendix B

This appendix presents the equations used to calculate the duty cycle for each current waveform case. In the main body of the thesis, only the equations corresponding to Case 1 are provided. Equations for current waveform Cases 2–5 are included here for completeness. Most of Subsection 5.5.1 is applicable to every case; therefore, only the missing parts are shown.

B.1 Stage 1: I^* Calculation

The function f_0 for current Case 1 is given in (5.24).

For Current Case 2:

$$\begin{aligned} f_0(d_x, d_y) = & \frac{d_x^2 k_{d_x} T_s}{2} - I_{ref} \\ & + d_y \left(\frac{d_0 k_{d_0} T_s}{2} + d_x k_{d_x} T_s + \frac{d_y k_{d_y} T_s}{2} \right) \\ & + \frac{d_0}{2} \left(\frac{d_0 k_{d_0} T_s}{4} + d_x k_{d_x} T_s - \frac{\left(\frac{d_0 k_{d_0} T_s}{2} + d_x k_{d_x} T_s + d_y k_{d_y} T_s \right)^2}{d_0 k_{d_0} T_s} \right) \end{aligned} \tag{B.1}$$

For Current Case 3:

$$\begin{aligned} f_0(d_x, d_y) = & \frac{d_y^2 k_{d_y} T_s}{2} - I_{ref} \\ & + \frac{d_x}{2} \left(d_0 k_{d_0} T_s + d_x k_{d_x} T_s + 2 d_y k_{d_y} T_s \right) \\ & + \frac{d_0}{2} \left(\frac{d_0 k_{d_0} T_s}{4} + d_y k_{d_y} T_s - \frac{\left(\frac{d_0 k_{d_0} T_s}{2} + d_x k_{d_x} T_s + d_y k_{d_y} T_s \right)^2}{d_0 k_{d_0} T_s} \right) \end{aligned} \tag{B.2}$$

For Current Case 4:

$$\begin{aligned} f_0(d_x, d_y) = & -2 k_{d_y} T_s \left(I_{ref} - \frac{d_x^2 k_{d_x} T_s}{2} + \frac{\left(d_x k_{d_x} T_s - \frac{k_{d_0} T_s d_0}{4} \right) d_0}{2} \right) \\ & - \left(d_x k_{d_x} T_s - \frac{k_{d_0} T_s d_0}{2} \right)^2 \end{aligned} \tag{B.3}$$

For Current Case 5:

$$
\begin{aligned}
f_0(d_x, d_y) = & \frac{k_{d_0} T_s \, k_{d_x} T_s}{2} - I_{ref} \, k_{d_x} T_s + d_x (k_{d_0} T_s)^2 + d_y (k_{d_0} T_s)^2 \\
& - \frac{(k_{d_0} T_s)^2}{2} - \frac{(d_x k_{d_0} T_s)^2}{2} - \frac{(d_y k_{d_0} T_s)^2}{2} - \frac{(d_y k_{d_y} T_s)^2}{2} \\
& - d_x k_{d_0} T_s \, k_{d_x} T_s - \frac{d_y k_{d_0} T_s \, k_{d_x} T_s}{2} - d_y k_{d_0} T_s \, k_{d_y} T_s + \frac{d_y k_{d_x} T_s \, k_{d_y} T_s}{2} \\
& - d_x d_y (k_{d_0} T_s)^2 + \frac{d_x^2 k_{d_0} T_s \, k_{d_x} T_s}{2} + d_y^2 k_{d_0} T_s \, k_{d_y} T_s + \frac{d_x d_y k_{d_0} T_s \, k_{d_x} T_s}{2} \\
& + d_x d_y k_{d_0} T_s \, k_{d_y} T_s - \frac{d_x d_y k_{d_x} T_s \, k_{d_y} T_s}{2}
\end{aligned}
\tag{B.4}
$$

For calculation of f_1, I_x and I_y are necessary to calculate. For current Case 1, they are presented in (5.30).

For current Case 2:

$$
\begin{aligned}
I_x &= \frac{d_x^2 k_{d_x} T_s}{2} \\
I_y &= d_y \left(d_x k_{d_x} T_s + \frac{d_y k_{d_y} T_s}{2} - \frac{k_{d_0} T_s d_0}{2} \right)
\end{aligned}
\tag{B.5}
$$

For current Case 3:

$$
\begin{aligned}
I_x &= \frac{d_x \left(d_x k_{d_x} T_s + 2 d_y k_{d_y} T_s - k_{d_0} d_0 T_s \right)}{2} \\
I_y &= \frac{d_y^2 k_{d_y} T_s}{2}
\end{aligned}
\tag{B.6}
$$

For current Case 4:

$$
\begin{aligned}
I_x &= d_x^2 \, k_{d_x} T_s k_{d_y} \\
I_y &= - \left(d_x k_{d_x} T_s - \frac{k_{d_0} T_s (d_x + d_y - 1)}{2} \right)^2
\end{aligned}
\tag{B.7}
$$

For current Case 5:

$$
\begin{aligned}
I_x &= - \frac{\left(d_y k_{d_y} T_s - k_{d_0} T_s d_0 \right) \left(\frac{d_y k_{d_y} T_s}{2} - \frac{k_{d_0} T_s d_0}{2} \right)}{k_{d_x}} \\
I_y &= d_y \left(\frac{d_y k_{d_y} T_s}{2} - \frac{k_{d_0} T_s d_0}{2} \right)
\end{aligned}
\tag{B.8}
$$

Reference current I^* for current Case 1 is shown in 5.40. For other current cases it is

as follows.

For current Case 2:

$$I^* = \frac{1}{2} k_{d_x} d_x T_s \tag{B.9}$$

For current Case 3:

$$I^* = k_{d_y} T_s d_y + \frac{1}{2} k_{d_0} T_s d_0 + \frac{1}{2} k_{d_x} T_s d_x \tag{B.10}$$

For current Case 4:

$$I^* = \frac{1}{2} k_{d_x} d_x T_s \tag{B.11}$$

For current Case 5:

$$I^* = \frac{1}{2} d_0 k_{d_0} T_s + \frac{1}{2} d_y k_{d_y} T_s \tag{B.12}$$

Derivatives $\frac{\partial f_0}{\partial d_x}$, $\frac{\partial f_0}{\partial d_y}$ are shown in (5.32) for current Case 1.
For current Case 2:

$$\begin{aligned} \frac{\partial f_0}{\partial d_x} &= -\frac{2 d_x k_{d_x}^2 T_s + d_y k_{d_0}^2 T_s - 2 d_x k_{d_0} k_{d_x} T_s}{2 k_{d_0}}, \\ &\quad - \frac{-2 d_y k_{d_0} k_{d_x} T_s - d_y k_{d_0} k_{d_y} T_s + 2 d_y k_{d_x} k_{d_y} T_s}{2 k_{d_0}}, \\ \frac{\partial f_0}{\partial d_y} &= \frac{(k_{d_0} - k_{d_y})\big(k_{d_0} - d_x k_{d_0} + 2 d_x k_{d_x} - 2 d_y k_{d_0} + 2 d_y k_{d_y}\big) T_s}{2 k_{d_0}} \end{aligned} \tag{B.13}$$

For current Case 3:

$$\begin{aligned} \frac{\partial f_0}{\partial d_x} &= \frac{(k_{d_0} - k_{d_x})\big(k_{d_0} - 2 d_x k_{d_0} + 2 d_x k_{d_x} - d_y k_{d_0} + 2 d_y k_{d_y}\big) T_s}{2 k_{d_0}}, \\ \frac{\partial f_0}{\partial d_y} &= -\frac{d_x k_{d_0}^2 T_s + 2 d_y k_{d_y}^2 T_s - d_x k_{d_0} k_{d_x} T_s}{2 k_{d_0}} \\ &\quad - \frac{-2 d_x k_{d_0} k_{d_y} T_s + 2 d_x k_{d_x} k_{d_y} T_s - 2 d_y k_{d_0} k_{d_y} T_s}{2 k_{d_0}} \end{aligned} \tag{B.14}$$

For current Case 4:

$$\begin{aligned}\frac{\partial f_0}{\partial d_x} &= 2k_{d_y}T_s\left(\frac{d_x k_{d_x}}{2}+\frac{1}{2}\left(\frac{k_{d_0}}{4}-k_{d_x}\right)d_0+\frac{k_{d_0}d_0}{8}\right)T_s \\ &\quad + 2\left(d_x k_{d_x}-\frac{k_{d_0}d_0}{2}\right)\left(\frac{k_{d_0}}{2}-k_{d_x}\right)T_s^2, \\ \frac{\partial f_0}{\partial d_y} &= \frac{(k_{d_0}-k_{d_y})\big(k_{d_0}-d_x k_{d_0}+2d_x k_{d_x}-d_y k_{d_0}\big)T_s^2}{2}\end{aligned} \tag{B.15}$$

For current Case 5:

$$\begin{aligned}\frac{\partial f_0}{\partial d_x} &= k_{d_0}^2T_s^2-d_x k_{d_0}^2T_s^2-d_y k_{d_0}^2T_s^2-k_{d_0}k_{d_x}T_s^2+d_x k_{d_0}k_{d_x}T_s^2 \\ &\quad + \frac{d_y k_{d_0}k_{d_x}T_s^2}{2}+d_y k_{d_0}k_{d_y}T_s^2-\frac{d_y k_{d_x}k_{d_y}T_s^2}{2}, \\ \frac{\partial f_0}{\partial d_y} &= \frac{(k_{d_0}-k_{d_y})\big(2k_{d_0}-k_{d_x}-2d_x k_{d_0}+d_x k_{d_x}-2d_y k_{d_0}+2d_y k_{d_y}\big)T_s^2}{2}\end{aligned} \tag{B.16}$$

Derivatives $\frac{\partial I_x}{\partial d_x}$,$\frac{\partial I_y}{\partial d_x}$, $\frac{\partial I_x}{\partial d_y}$, $\frac{\partial I_y}{\partial d_y}$ for current Case 1 are shown in (5.38).
For current Case 2:

$$\begin{aligned}\frac{\partial I_x}{\partial d_x} &= d_x k_{d_x}T_s, \\ \frac{\partial I_y}{\partial d_x} &= -\frac{d_y\left(k_{d_0}T_s-2k_{d_x}T_s\right)}{2}, \\ \frac{\partial I_x}{\partial d_y} &= 0, \\ \frac{\partial I_y}{\partial d_y} &= \frac{k_{d_0}T_s}{2}-\frac{d_x k_{d_0}T_s}{2}+d_x k_{d_x}T_s-d_y k_{d_0}T_s+d_y k_{d_y}T_s\end{aligned} \tag{B.17}$$

For current Case 3:

$$\begin{aligned}\frac{\partial I_x}{\partial d_x} &= \frac{k_{d_0}T_s}{2}-d_x k_{d_0}T_s+d_x k_{d_x}-\frac{d_y k_{d_0}T_s}{2}+d_y k_{d_y}T_s \\ \frac{\partial I_y}{\partial d_x} &= 0 \\ \frac{\partial I_x}{\partial d_y} &= -\frac{d_x(k_{d_0}-2k_{d_y})T_s}{2} \\ \frac{\partial I_y}{\partial d_y} &= d_y k_{d_y}T_s\end{aligned} \tag{B.18}$$

For current Case 4:

$$\begin{aligned}
\frac{\partial I_x}{\partial d_x} &= 2 d_x k_{d_x} k_{d_y} T_s^2 \\
\frac{\partial I_y}{\partial d_x} &= 2 \left(d_x k_{d_x} T_s - \frac{k_{d_0} T_s d_0}{2} \right) \left(\frac{k_{d_0} T_s}{2} - k_{d_x} T_s \right) \\
\frac{\partial I_x}{\partial d_y} &= 0 \\
\frac{\partial I_y}{\partial d_y} &= k_{d_0} T_s \left(d_x k_{d_x} T_s - \frac{k_{d_0} T_s d_0}{2} \right)
\end{aligned} \tag{B.19}$$

For current Case 5:

$$\begin{aligned}
\frac{\partial I_x}{\partial d_x} &= \frac{k_{d_0} \left(k_{d_0} - d_x k_{d_0} - d_y k_{d_0} + d_y k_{d_y} \right) T_s}{k_{d_x}} \\
\frac{\partial I_y}{\partial d_x} &= -\frac{d_y k_{d_0} T_s}{2} \\
\frac{\partial I_x}{\partial d_y} &= \frac{\left(k_{d_0} - k_{d_y} \right) \left(k_{d_0} - d_x k_{d_0} - d_y k_{d_0} + d_y k_{d_y} \right) T_s}{k_{d_x}} \\
\frac{\partial I_y}{\partial d_y} &= \frac{k_{d_0} T_s}{2} - \frac{d_x k_{d_0} T_s}{2} - d_y k_{d_0} T_s + d_y k_{d_y} T_s
\end{aligned} \tag{B.20}$$

B.2 Stage 2. d_x, d_y calculation

Duty cycle d_x, current components I_x, I_y and derivatives $\frac{\partial I_x}{\partial d_y}$, $\frac{\partial I_y}{\partial d_y}$ for current Case 1 are shown in (5.41), (5.42), (5.43).

For current Case 2:

$$\begin{aligned}
d_x &= \frac{2 I^*}{k_{d_x} T_s}, \\
I_x &= \frac{I^* \left(I_{st} + I^* \right)}{k_{d_x} T_s} \\
I_y &= d_y \left(I_{st} + I^* - \frac{k_{d_0} T_s}{2} \left(d_y + \frac{2 I^*}{k_{d_x} T_s} - 1 \right) + \frac{d_y k_{d_y} T_s}{2} \right) \\
\frac{\partial I_x}{\partial d_y} &= 0 \\
\frac{\partial I_y}{\partial d_y} &= I_{st} + I^* - \frac{k_{d_0} T_s}{2} \left(d_y + \frac{2 I^*}{k_{d_x} T_s} - 1 \right) + \frac{d_y k_{d_y} T_s}{2} - d_y \left(\frac{k_{d_0} T_s}{2} - \frac{k_{d_y} T_s}{2} \right)
\end{aligned} \tag{B.21}$$

For current Case 3:

$$
\begin{aligned}
d_x &= -\frac{2I^* - k_{d_0}T_s + d_y k_{d_0}T_s - 2d_y k_{d_y}T_s}{k_{d_0}T_s - k_{d_x}T_s} \\
I_x &= -\frac{(I_{st} + I^*)\left(2I^* - k_{d_0}T_s + d_y k_{d_0}T_s - 2d_y k_{d_y}T_s\right)}{2(k_{d_0}T_s - k_{d_x}T_s)} \\
I_y &= \frac{1}{2}d_y^2 k_{d_y}T_s \\
\frac{\partial I_x}{\partial d_y} &= -\frac{(k_{d_0} - 2k_{d_y})(I_{st} + I^*)}{2(k_{d_0} - k_{d_x})} \\
\frac{\partial I_y}{\partial d_y} &= d_y k_{d_y}T_s
\end{aligned}
\tag{B.22}
$$

For current Case 4:

$$
\begin{aligned}
d_x &= \frac{2I^*}{k_{d_x}T_s} \\
I_x &= \frac{2I^* k_{d_y}(I_{st} + I^*)}{k_{d_x}} \\
I_y &= -\left(I_{st} + I^* - \frac{k_{d_0}T_s}{2}\left(d_y + \frac{2I^*}{k_{d_x}T_s} - 1\right)\right)^2 \\
\frac{\partial I_x}{\partial d_y} &= 0 \\
\frac{\partial I_y}{\partial d_y} &= k_{d_0}T_s\left(I_{st} + I^* - \frac{k_{d_0}T_s}{2}\left(d_y + \frac{2I^*}{k_{d_x}T_s} - 1\right)\right)
\end{aligned}
\tag{B.23}
$$

For current Case 5:

$$
\begin{aligned}
d_x &= -\frac{2I^* - k_{d_0}T_s + d_y k_{d_0}T_s - d_y k_{d_y}T_s}{k_{d_0}T_s} \\
I_x &= -\frac{2(I^*)^2}{k_{d_x}T_s} \\
I_y &= d_y\left(\frac{I_{st}}{2} + \frac{I^*}{2}\right) \\
\frac{\partial I_x}{\partial d_y} &= 0 \\
\frac{\partial I_y}{\partial d_y} &= \frac{I_{st}}{2} + \frac{I^*}{2}
\end{aligned}
\tag{B.24}
$$