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Efficiency Performance of 7-Level Multilevel Multiplexed and 3-level NPC Converters

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Abstract

Multilevel converters play a vital role in medium-voltage AC drive system and grid connected system applications, as they provide a high conversion efficiency while substantially reducing total harmonic distortion (THD) in the output voltages and currents, thereby enhancing overall power quality and performance of the system. This thesis presents a comprehensive study of the efficiency, power losses, and THD characteristics of the three-phase multiplexed multilevel converter in comparison with the conventional three-phase three-level neutral-point-clamped (NPC) converter. Simulation models are designed using MATLAB®Simulink (R2024b), leveraging its advanced electro-thermal semiconductor models to accurately compute conduction and switching losses for both topologies under various operating conditions. Although the three-level NPC converter offers advantages such as simpler topology, fewer semiconductor components, and lower implementation cost, it exhibits inferior output voltage quality due to higher THD and high dv/dt stress. In contrast, the multiplexed multilevel converter achieves superior power quality and reduced harmonic content. The simulation results validate the THD for NPC converter is 54% higher, at medium load 75% higher and at lower load 57% higher, power losses in semiconductors are for NPC converter are: 13% higher at higher load, 18% higher at medium load, 39% higher and efficiency metrics for both, three-phase three-level NPC converter and the three-phase multiplexed multilevel converter, enabling a detailed comparative evaluation of their performance.

Abbreviations

RES	Renewable Energy Source
DC	Direct Current
AC	Alternating Current
UPS	Uninterruptible Power Supplies
EV	Electrical Vehicles
SiC	Silicon Carbide
GaN	Gallium Nitride
THD	Total Harmonic Distortion
CHB	Cascaded H-Bridge
PDPWM	Phase Disposition Pulse Width Modulation
PODPWM	Phase Opposite Disposition Pulse Width Modulation
APODPWM	Alternate Phase Opposite Disposition Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
EMI	Electromagnetic Interference
NPC	Neutral Point Clamped Converter
FC	Flying Capacitor
$3\phi 7LM_LM_X$	3-phase 7-levels multilevel Multiplexed
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
FC	Flying capacitor
IGBT	Insulated Gate Bipolar Transistor

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Chapter 1:

Introduction

1.1 Literature Review and Thesis Objectives

The multilevel converters are widely used in applications likes: DC and AC power transmissions [1], motor drives [2], renewable energy systems (RESs) integrations [3], energy storage system [4], uninterruptible power supplies (UPS) [5], power chargers [6], and electric vehicles (EVs) [7]. The 2-level converter has simple topology and modulation scheme; however, it suffers from high switching losses at higher switching frequencies [8, 9]. To cope with this issue, the engineers proposed two solutions. One way is to use advanced silicon carbide (SiC) and gallium nitride (GaN) switches, which have high switching frequency, but there are some operating constraints, and the cost of the system will increase [10]. The second way is to use multilevel converter topologies based on conventional semiconductor switches [11]. The multilevel converters have the advantages of better power quality, lower voltage ratings of semiconductors, lower filter size, and low redundancy in the system. In the last few decades, several topologies of multilevel converters have been introduced in the literature [12].

The increased demand for multilevel converters in medium voltage applications is pushing the advancements and the state of the art in their design, notably in terms of improving efficiency and reductions in THD [13]. Traditional H-bridge two-level converters in medium and high-power applications are frequently restricted by the voltage limitations of commercially available power switches. When these switching devices do not fulfill the voltage rating requirements then series-connected switches are used to increase the voltage stress requirement of the converter. However, this strategy creates many issues in terms of dynamic voltage sharing between the switches [14]. To solve the above problems, multilevel converters were designed and developed [15, 16], offering several advantages over conventional H-bridge two-level converters, including:

- The characteristic waveforms of multilevel converters have lower harmonic contents at lower switching frequencies, which reduces the need for expensive filters [17].
- They can handle medium and high-voltage applications using ordinary commercial power devices and they eliminate the need for series-connected switches that are used in conventional 2-level converters and the associated dynamic voltage-sharing problem [18].
- Multilevel converters can operate at lower switching frequencies because of many level in the voltage and current waveforms, which will minimize the power losses in the semiconductors and maintain higher power efficiency of the converter [19].

Because of the many advantages of multilevel converters, these converters are the preferred choice for medium- and high-voltage applications [20, 21]. Recently, in [22, 23, 24, 25, 26] the most widely used multilevel converter structures and their advantages have been reviewed with a focus on evaluating their efficiency and THD. It is essential to choose the appropriate conversion topology and technology to improve the THDs of the output currents, output voltages, efficiency, power losses, and other attributes of multilevel converters [27, 28]. The fundamental properties of multilevel converters like DC bus neutral point voltage balancing and flying capacitor (FC) voltage balancing techniques that influence the performance of multilevel converters are discussed by the authors in [29, 30]. Recent developments have introduced new multilevel converter topologies [31], specifically designed for medium-voltage applications. Modular multilevel converters (MMCs) have been extensively reviewed in [32], highlighting their unique capabilities, operational principles, and advantages in high-power and high-voltage applications. These converters are widely recognized for their scalability, modularity, and ability to deliver superior power quality with reduced harmonic distortion. The practical application of MMCs in medium-voltage electric drives has been demonstrated in [33], showing their effectiveness in industrial and commercial applications. A comprehensive analysis of the FCs architecture, specifically tailored for MMCs, is provided in [34]. This study delves into the operational nuances of FCs, emphasizing their role in ensuring proper voltage balancing across the FCs. One of the major challenges associated with MMCs is the

charging or discharging of FCs to keep the voltage balanced, a critical issue that can impact both the performance and stability of the converters. This challenge has been effectively addressed through innovative and cost-efficient methods, as outlined in [35]. These methods not only simplify the capacitor charging/discharging process but also integrate seamlessly with various converter topologies. Furthermore, the exploration of multilevel converter topologies has extended beyond AC applications to include DC-DC applications, as detailed in [36, 37].

Power electronics research is heavily reliant on the development of novel multilevel converters topologies, and many new topologies have been developed to meet requirement of the variety of applications. Regarding the new topologies the common and basic questions of are discussed in [38] from where the new topologies are developing, from a generic topology of multilevel converters, or is there a common way to derive a new topology from basic multilevel converter topologies. There are three main types of multilevel converters topologies that are used in industry: cascaded H-bridge (CHB) converter, FC converter, and neutral point clamped (NPC) converter. The NPC converter does not have any FC and separate DC voltage supply compared with other two basic topologies of multilevel converters, so it can be best choice among other two topologies. The $3\phi 3L$ NPC converter, which consists of two conventional two-level converters [39], is configured with the first inverter one above the other converter and two diodes are clamped in series between the upper and lower inverters at the neutral point (N). Over the past thirty years, these inverters have been widely used in industrial applications requiring approximately 6 kV. The FC converter represents another type of multilevel converters [40, 41]. Unlike other multilevel converter topologies such as the NPC converter, the FC converter does not require any clamping diode. The FC converter is implemented by connecting a series of capacitors to a clamped switching cell, allowing these capacitors to facilitate voltage division across the semiconductors in a phase leg. This division enables the delivery of smaller, discrete, and required voltage levels to semiconductors, ensuring smoother operation and overall improved performance. Two FC converters and one NPC converter are employed in the three-phase seven-level multilevel multiplexed ($3\phi 7LM_LM_X$) converter described in [42] to achieve seven voltage levels. In this architecture, the positive and negative half-cycles of the output waveform are generated by

the FC converters stage, while the NPC converter combines these half-cycles to produce a continuous sinusoidal output.

It is noteworthy that the NPC stage of the $3\Phi 7LM_LM_X$ converter shares the same structural topology as the conventional $3\Phi 3L$ NPC converter. Furthermore, the voltage stress on the IGBTs remain identical in NPC stage of $3\Phi 7LM_LM_X$ converter and conventional $3\Phi 3L$ NPC converter. As a matter of fact, even if the $3\Phi 7LM_LM_X$ converter is a seven-level converter, the voltage stress on the switches of the NPC stage is $V_{dc}/2$. From this point of view, it seems that the $3\Phi 7LM_LM_X$ converter appears inferior converter compared to the conventional $3\Phi 3L$ NPC converter, as it has additional switches (the switches of upper FC converter stage and lower FC converter stage) without reducing the voltage stress on the NPC stage of $3\Phi 7LM_LM_X$ converter. The comparison of both converters is shown in Table 1.1.

Table 1.1: Comparison table of multilevel converters.

Converter Topology	Number of Semiconductors	Number of power semiconductors with 1/6 V_{dc}	Number of power semiconductors with 1/2 V_{dc}
3ϕ3L NPC converter	12 + 6 clamping diodes	-	12 + 6 clamping diodes
3ϕ7L FC converter	36	36	-
3ϕ7LM_LM$_X$ converter	24 + 6 clamping diodes	12	12 + 6 clamping diodes

However, with the use of the upper FC converter and lower FC converter can lead to advantages in terms of THD and efficiency of the $3\Phi 7LM_LM_X$ converter. The aim of this thesis is to deeply compare the $3\Phi 7LM_LM_X$ converter and the $3\Phi 3L$ NPC converter from an efficiency and THD point of view, in order to evaluate and quantify the benefits of the $3\Phi 7LM_LM_X$ converter. One also has to note that the voltage stress on the switches of the both FC converters stages is $V_{dc}/6$ across all the switches; therefore, even if the $3\Phi 7LM_LM_X$ converter has additional switches compared to a conventional NPC converter, the additional cost and complexity associated with FC converter stages remain relatively minor and therefore $3\Phi 7LM_LM_X$ converter could be a promising converter comparatively.

In this thesis, two types of multilevel converters are designed, and compared for

better efficiency and THD performances. The one is $3\phi 3L$ NPC converter and other is $3\phi 7LM_LM_X$ converter. The $3\phi 7LM_LM_X$ converter derived from two basic topologies of multilevel converters and has two stages. The first stage has two FC converters and second stage has one NPC converter as shown in the Figure 1.

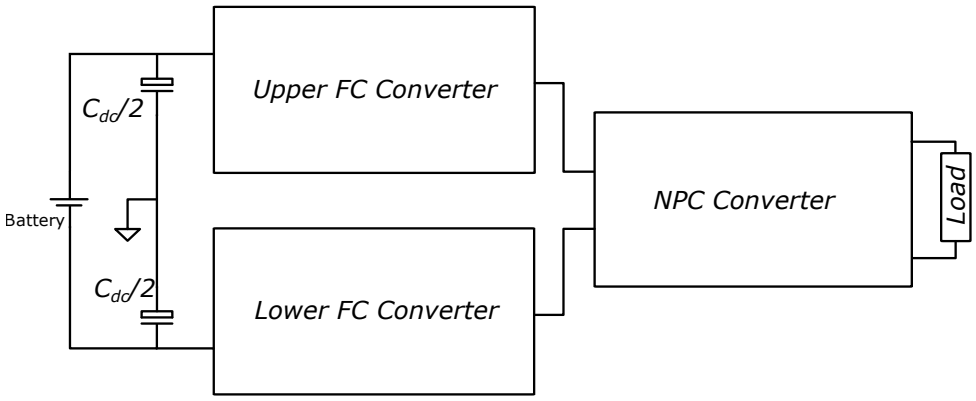

Figure 1.1: Schematic diagram of $3\phi 7LM_LM_X$ converter

A brief introduction to the modulation schemes of $3\phi 7LM_LM_X$ converter and $3\phi 3L$ NPC converter, following the objectives of thesis, are show in below sections.

1.2 Modulation Techniques for Multilevel Converters

All the multilevel converters operate in switching mode, meaning each semiconductor device within a converter repeatedly has to turn on and turn off. This action of switching ensuring lower switching and conduction losses. For controlling the on and off switching of the converter, various modulation techniques are used. There are many types of modulations used for different topologies of the converter. Also, their mutual interaction can be used to enhance the performance of the converter in terms of switching losses, distortion, harmonic content, and complexity of the algorithm used. There are 3 PWM techniques that can be used for multilevel converters. (1) Programmed PWM, (2) Carrier-Based PWM, and (3) Space Vector PWM.

1.2.1 Programmed Pulse Width Modulation

This type of modulation technique is being called the off-line modulation. Which means, that turning-on and turning-off points of PWM for the switches are already programmed. The result of such calculations is just a set of switching instants. Such early

calculations of switching instants can help, properly removing the harmonic contents from output voltage or current. As a results of these properly computed switching instants, two useful criteria of the modulation exists: (1) Harmonic Elimination PWM (2) Minimum Harmonic Distortion PWM Additionally, H-bridge type multilevel inverters are only employed with programmed PWM.

1.2.2 Pulse Width Modulation Techniques for Multilevel Converters

The widely used Pulse Width Modulation (PWM) technique for controlling the multilevel converters is Sinusoidal Pulse Width Modulation (SPWM). In this modulation technique, the carrier signal with the frequency that of switching frequency of the converter compared with the modulation/control signal and generate a PWM signal. When a control signal is higher than the carrier signal it generate high PWM signal and whenever the control signal is lower than the carrier signal it generates zero PWM signal. The SPWM control approach was introduced with the primary goal of reducing switching losses. This technique also improved multilevel converter's performance. There are various SPWM techniques based arrangement of carrier signal for multilevel converters. For this technique, there are 3 SPWM techniques.

1.2.2.1 Phase Disposition PWM (PDPWM)

With this method, all carrier signals have the same frequency and amplitude and are synced in phase; the only differences are in the vertical level shifts. PDPWM is beneficial because it allows for the use of higher switching frequencies and provides effective control over neutral point voltage. The PDPWM is used in $3\phi 3L$ NPC converter and $3\phi 7LM_LM_X$ converter because It provides reference voltage levels for converter to follow.

1.2.2.2 Phase Opposition Disposition PWM (PODPWM)

In PODPWM, all the carrier waveforms above the zero axis, should have zero phase difference with same F_{SW} and amplitude. While, carrier signal below zero axis should also have same F_{SW} and amplitude. Overall, carrier signals above and below the zero axis should have 180° phase difference between each other. As shown in Figure 1.3.

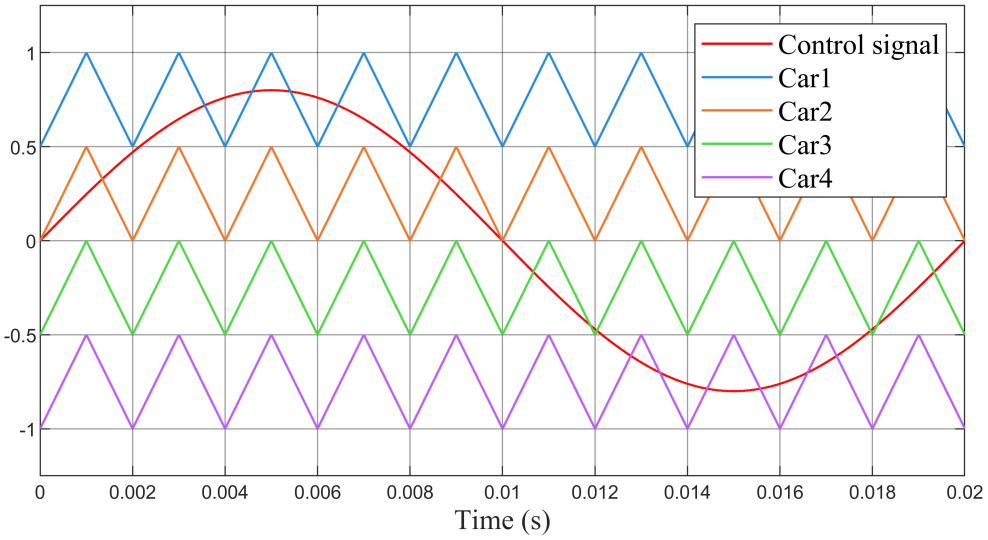

Figure 1.2: Phase disposition pulse width modulation for multilevel converters.

1.2.2.3 Alternate Phase Opposition Disposition PWM (APODPWM)

In APODPWM, every adjacent carrier waveforms should have 180° phase difference as shown in Figure 1.4. The frequency and amplitude will be same among all carrier waveforms.

1.2.3 Space vector Pulse width Modulation

Space vector pulse width modulation (SVPWM) is a form of PWM modulation. It is also only being called space vector modulation (SVM) or carrier less PWM. The main advantage of SVM over carrier based PWM is that explicit identification of pulses placements. The principle of SVM can easily be understand using 2-level or 3-level H-bridge inverter. Because it contains only eight switching vectors which are easily and simple to understand implement. The six switching vectors are active vectors and remaining two are null vectors Actually these vectors are the phase voltages of the phases transformed in alpha and beta as shown in Figure 1.5. For $3\phi 7LM_LM_X$ converter the the SVPWM will more complicated because it need more switching vectors than 3 level converter.

1.3 Objectives of Thesis

The primary objective of this thesis is to investigate and compare the efficiency performance of advanced multilevel converter topologies for medium-voltage AC applica-

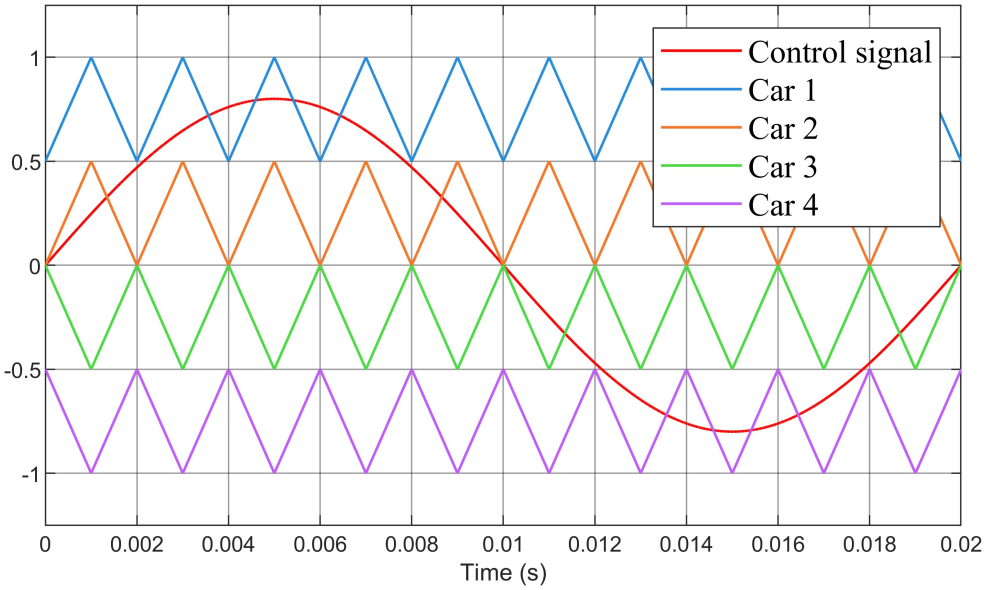

Figure 1.3: Phase opposite disposition pulse width modulation technique for multilevel converters.

tions, with a focus on enhancing power quality, reducing power losses, and optimizing system design. It is worth noting that the NPC stage of the $3\phi 7LM_LM_X$ converter shares the same structure as the $3\phi 3L$ NPC converter. Furthermore, the voltage stress on the switches is identical in both cases. Indeed, although the $3\phi 7LM_LM_X$ converter is a seven-level converter, the voltage stress on the switches of the NPC stage remains $Vdc/2$. From this perspective, the $3\phi 7LM_LM_X$ converter may appear inferior to the standard NPC, since it introduces additional switches in the FCC stages without reducing the voltage stress on the NPC stage. However, the inclusion of the FCC stages offers potential advantages in terms of THD and converter efficiency. Therefore, the aim of this thesis is to rigorously compare the $3\phi 7LM_LM_X$ and $3\phi 3L$ NPC converters from an efficiency and THD standpoint, in order to evaluate and quantify the benefits of the $3\phi 7LM_LM_X$ topology. To achieve this, the following specific objectives are pursued:

- To conduct a comprehensive comparative analysis: Perform detailed simulations using MATLAB® Simulink 2024b to calculate switching and conduction losses, THD in output voltages and currents, and overall efficiency for both the $3\phi 7LM_LM_X$ converter and $3\phi 3L$ NPC converter under low voltage, medium-voltage and high-voltage conditions.

- To assess topological advantages: Examine the structural integration in the $3\phi 7LM_LM_X$

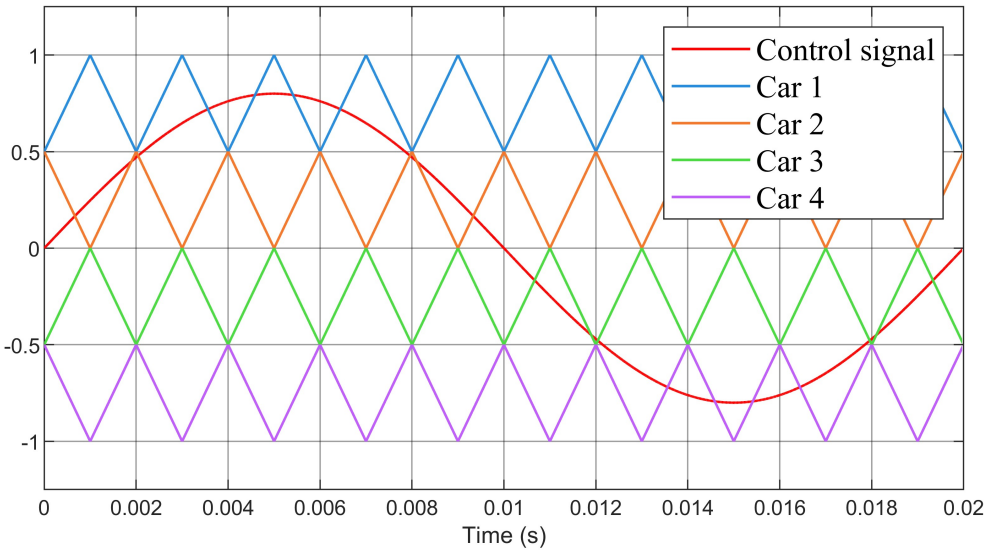

Figure 1.4: Alternate phase opposite disposition pulse width modulation technique for multilevel converters.

converter, which combines two four-level FC converter with a three-level NPC converter stage to generate seven levels of voltage ($\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$, and 0), and compare it to the simpler $3\phi 3L$ NPC design, highlighting benefits such as reduced harmonic content at lower switching frequencies, elimination of series-connected switches, despite the increased component count (24 switches plus 6 clamping diodes versus 12 switches plus 6 clamping diodes).

- To validate control strategies: Implement and analyze flying capacitor voltage balancing control techniques for the FC converter stages of the $3\phi 7LM_LM_X$ converter using cost function minimization based on redundant switching states, alongside carrier-based pulse-width modulation (PWM) strategies to ensure stable operation, voltage regulation, and minimal deviation from reference values.

- Quantify performance metrics: Validate simulation results to demonstrate how the $3\phi 7LM_LM_X$ converter achieves superior THD reduction and efficiency improvements over the $3\phi 3L$ NPC converter, while addressing challenges like capacitor voltage imbalance, system complexity, and cost-effectiveness, thereby providing evidence-based recommendations for the adoption of multiplexed topologies in high-power, medium-voltage applications.

Through these objectives, this thesis contributes to the advancement of multilevel con-

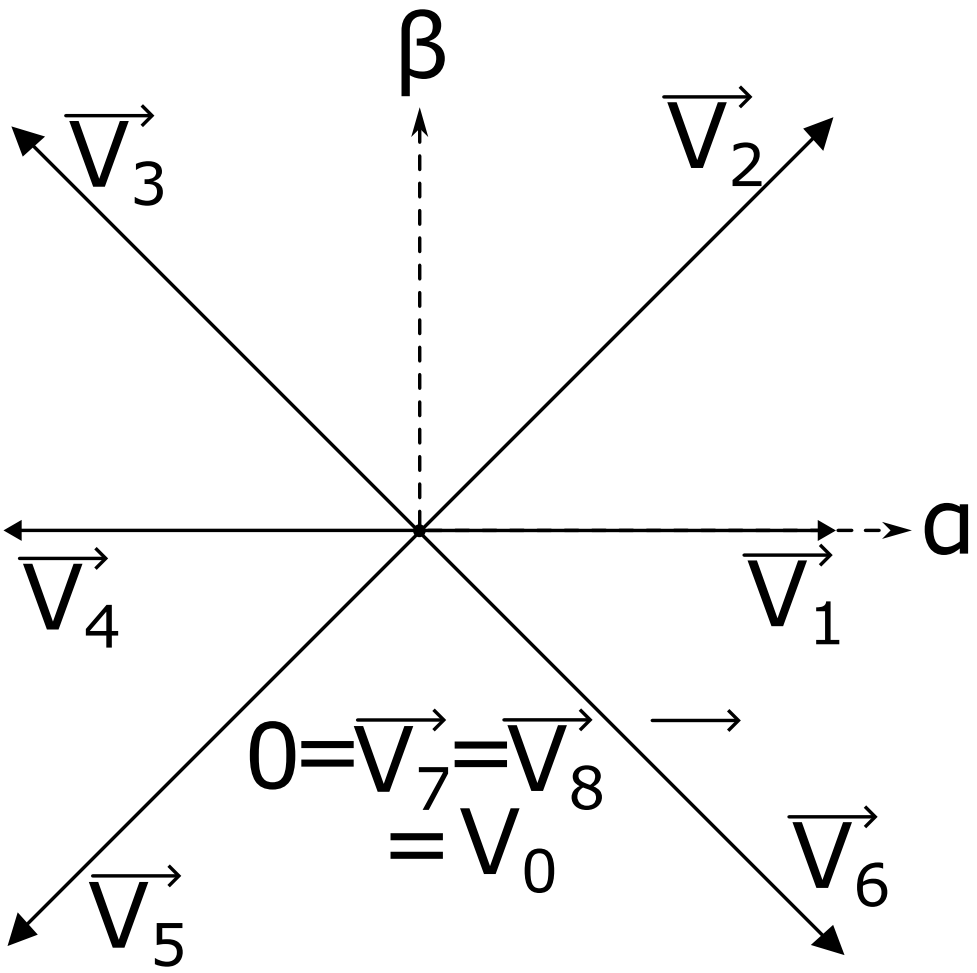

Figure 1.5: Space vector pulse width modulation technique for multilevel converters.

verter technologies by offering substantiated insights into design optimizations that balance efficiency, power quality, and practical implementation feasibility.

1.4 Thesis outline

This thesis is organized into six chapters that sequentially address the key elements of the research topic, as detailed below.

Chapter 2: It discusses the different types of multilevel converters and explains their working principles in detail. This chapter compares the required number of switches for each topology and also their switching operation. It also examines the number of FCs units, role and quantity for clamping diodes used. Voltage levels across each FCs are analyzed for each stage of multilevel converters. The voltage stress across insulated-gate bipolar transistors (IGBTs) is also compared. This analysis highlights the trade-offs

between different converter designs.

Chapter 3: Flying capacitors voltage balancing can be achieved using different methods. One approach is redundant switching state selection, where appropriate states are chosen to maintain voltage across the FCs. Another method relies on feedback control loops that continuously regulate capacitor voltages. Predictive control techniques are also applied to forecast voltage deviations and correct them in advance. Hysteresis-based balancing can be used to keep capacitor voltages within predefined limits. Cost function–based optimization is another effective strategy, often employed in model predictive control. Hybrid approaches combine two or more of these methods to improve performance. The choice of method depends on the converter topology, control complexity, and desired efficiency.

Chapter 4: In this chapter, the results obtained from $3\phi 3L$NPC converter and $3\phi 7LM_LM_X$ converter are presented and discussed. The performance of each converter is evaluated under the same operating conditions. Comparative analysis is carried out to highlight similarities and differences in their behavior. The power losses, efficiency and THD are interpreted to demonstrate the strengths and limitations of each topology. This discussion provides a basis for assessing the efficiency and THD suitability of the converters for practical applications.

Chapter 5: In this chapter, the conclusion of the thesis is presented.

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Chapter 2:

Multilevel Converters Topologies

This chapter introduce, describe, and analyse the principal topologies of multilevel converters comprehensively. Over recent decades, multilevel converter technology has gained significant attention due to its advantages in high-power and medium-voltage applications. These benefits include reduced electromagnetic interference (EMI), improved waveform quality, and reduced voltage stress on semiconductor switches. As a result, multilevel converters work well with a range of commercial, industrial, and RESs.

The three most popular multilevel converter topologies— NPC converter, FC converter and Multiplexed multilevel converter—are the subject of this chapter. Each of these topologies has distinct operating principles, performance trade-offs, and structural features. Notably, the multiplexed multilevel converter topology is presented as an emerging configuration, attracting interest for its increased flexibility and modularity in large-scale applications.

This chapter provides an in-depth overview of circuit construction, switching strategies, operation, and the benefits and drawbacks of each topology. The purpose of this comprehensive comparison study is to compare the NPC converter topology and multiplexed multilevel converter topology in terms of operation, complexity, number of switches and how to choose and best suit each topology for specific application needs.

2.1 Flying Capacitor Multilevel Converter

The FC converter was initially proposed by the author of [1, 2]. It is named after the structure that relies on multiple FCs to achieve higher output voltages [3]. This topology can be derived from a general topology. FC converter can perform similarly to NPC converter but it has no clamping diode. These converters can used in applicatiosn where high power density and reduced harmonic distortion are required commonly used in

electric vehicle (EV) applications and battery management system (BMS) [4]. In order to ensure proper operation of the FC converter, the voltages at FCs must be carefully regulated to minimize voltage stress on each switching device during every commutation step [4]. In each phase leg of three-phase FC converter, the FCs undergoes rapid charging and discharging to maintain voltage balancing across each FCs of the FC converter. Its charging and discharging processes must typically be kept constant within a single switching period [5].

An N-level FC converter consists of multiple power cells connected in series, with each cell contributing one voltage level to the output. Each cell consists of pair of an IGBT and a FC, except for first cell which is directly connected to the DC supply terminals. For example, the first cell typically includes the switching devices first IGBT and last IGBT, along with the first FC. The same structural arrangement is applied to the remaining cells, with each cell responsible for generating or regulating one of the intermediate voltage steps required to synthesis the desired multilevel output voltage waveform.

To generate a seven-level output voltage waveform, six power cells are required, including one for the zero-voltage level. Thus, as the number of output voltage levels increases, the total number of cells and associated FCs increases proportionally. This modular structure enables the converter to produce good-quality waveforms with reduced harmonic distortion, thereby improving performance of multilevel converters in medium- and high-voltage applications. In each phase leg of an N-level FC converter, there are N–2N FCs that works as clamping elements to maintain required voltage levels. These FCs are essential in forming the voltage across the multilevel converters as staircase levels and serve as voltage buffers between switching states. The voltage across each FCs must be appropriately regulated based on its location in the multilevel converter, since each supplies a distinct proportion of the overall DC-link voltage [5]. The following is an expression for calculating the FCs voltage levels:

$$V_{cxn} = k\frac{V_{dc}}{n-1}, \mathrm{x} \in \{\mathrm{a},\ \mathrm{b}\}, \mathrm{k} = 1 \ldots \mathrm{n}-2 \tag{2.1}$$

Where x is the phase of FC converter, n is the number of voltage levels, V_{dc} is supplied DC voltage and V_{cxn} is voltage of the FC. The current flowing through FC Cxn depends on the neighboring switching states of the capacitor and direction of current which can be

either a positive current or a negative current.

The $3\phi 7L$ FC converter requires a total of 36 switches and 15 FCs for three-phase system. Compared to other multilevel converter topologies, this results in a significantly higher component count, increased complexity, many challenges in balancing the voltages across the FCs, and overall high complexity in implementation.

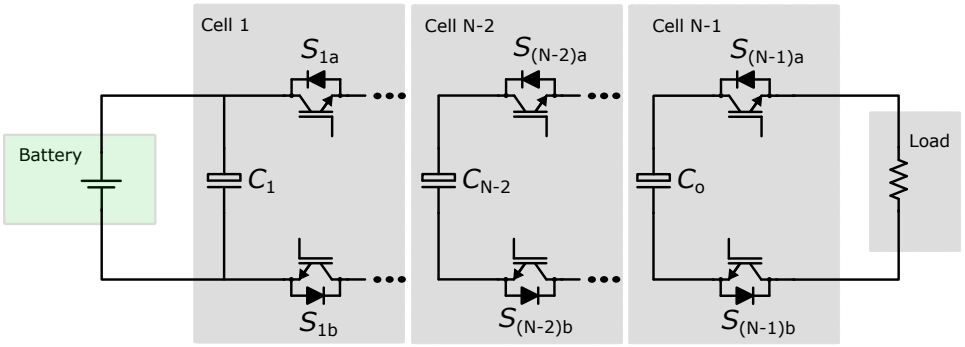

Figure 2.1: Basic topology of N-Levels FC converter.

The FC converter used in this thesis is four-level FC converter as top FC converter and bottom Fc converter. The converter leg structure is composed of three cascaded power cells. Each cell contains a pair of complementary switching devices along with a FC, resulting in a total of three FC distributed throughout the phase leg. These FCs establish the intermediate voltage steps required to synthesis the multilevel converter output waveform. The operating principle of the four-level FC converter relies on the controlled charging and discharging of each FC in a switching period. By properly sequencing the switching states, the converter can generate discrete levels of output voltage at its output terminal. The voltages across the FCs must remain proportional to the overall DC-link voltage and balanced to ensure proper operation. Maintaining this equilibrium prevents excessive stress on power semiconductor devices and ensures symmetrical output waveforms with low harmonic distortion during proper converter operation. Under dynamic operating conditions, including sudden load variations and transient phenomena, maintaining proper voltage balance across the FCs is highly critical. If the FC voltages deviate from their target values, the resulting output voltage levels become distorted. This leads to increased switching power losses, diminished efficiency, and increases thermal stress on the switching devices. Consequently, various modulation and control strategies—such as redundant switching-state selection and capacitor-charge feedback regulation—are commonly implemented to stabilize the FC voltage levels. The balanced voltages across

the inner FCs can be represented as follows:

$$V_{FC1} = V_{dc}/3 \quad \text{and} \quad V_{FC2} = 2V_{dc}/3 \tag{2.2}$$

The converter is capable of generating four distinct voltage levels between phase terminal and the neutral point. Table 2.1 presents the output voltage levels of the 4-level FC converter along with the corresponding switching states.

State of IGBTs								V_o	Level
S_1	S_{p2}	S_3	S_4	S_{p5}	S_6	C_{F1}	C_{F2}		
1	1	1	0	0	0	N	N	V_{dc}	3
1	1	0	1	0	0	C $(i>0)$ D $(i<0)$	N	$\frac{2V_{dc}}{3}$	2
1	0	1	0	1	0	D $(i>0)$ C $(i<0)$	C $(i>0)$ D $(i<0)$		
0	1	1	0	0	1	N	D $(i>0)$ C $(i<0)$		
0	0	1	0	1	1	D $(i>0)$ C $(i<0)$	N	$\frac{V_{dc}}{3}$	1
0	1	0	1	0	1	C $(i>0)$ D $(i<0)$	D $(i>0)$ C $(i<0)$		
1	0	0	1	1	0	N	C $(i>0)$ D $(i<0)$		
0	0	0	1	1	1	N	N	0	0
C: Charging D: Discharging N: No Change									

Table 2.1: Switching states and output voltage levels of 4L FC converter

The sub-circuits during each switching state of 4-L FC converter are discussed in below subsections.

2.1.1 State 1

State 1 represents a first switching configuration from the Table 2.1 of the FC converter. The topology for this converter consists of 6 switches from S_1 through S_6 in a leg clamped though the FCs C_{F1} and C_{F2}. The voltage across the FCs is distributed precisely, where upper FC has maintain a voltage of $2/3V_{dc}$, while lower FC maintain a voltage $1/3V_{dc}$ of the total DC-link voltage. This voltage division of total DC-link voltage is very essential to achieve levels of the total output voltage. In this state of converter a particular combination of the switches is activated by PWM creating a defined conduction conduction

path through the converter. During the first state of voltage level switches S_1, S_2, and S_3 are turned on that causes the current flow from V_{dc} to output of FC converter. During this state of FC converter, no FC is being charged or discharged and there is no redundant switching state of the converter. Due the the conduction of switches the voltage across the load is full supplied. The switches that are turned-off during this state are S_4, S_5 and S_6 and have voltage stress of $V_{dc}/3$. The Figure 2.2 illustrates the first switching state of FC converter.

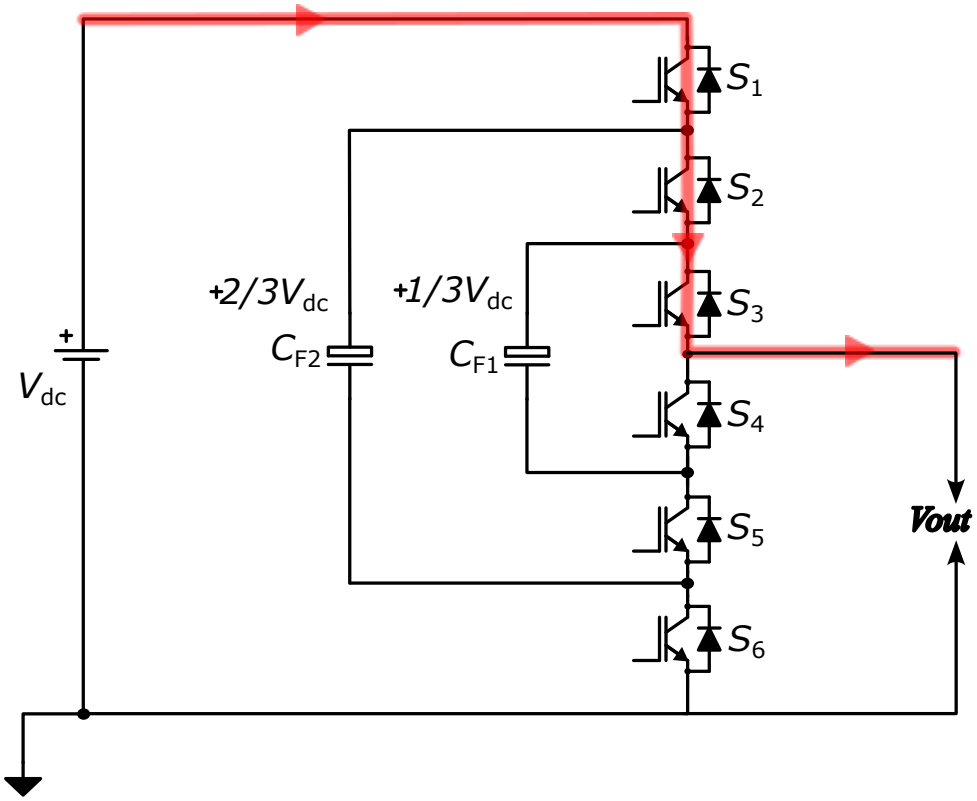

Figure 2.2: First switching state operation of $4L$ FC converter.

2.1.2 State 2

During this switching state of FC converter, an IGBT S_1 remain turned off, while only IGBTs S_2 and S_3 are turned on. In this state FC C_{F2} gets discharged into the load and there is no effect on the FC C_{F1}. The current follow the path from C_{F2} through $S2$ and S_3 to the load. The other complementary IGBTs perform switching as per the operation of these IGBTs. Because of the conduction of S_2 and S_3 the load the voltage remains at level of $2V_{dc}/3$. The switches that are turned-off during in this state are S_1, S_4 and S_5 and have voltage stress of $V_{dc}/3$.

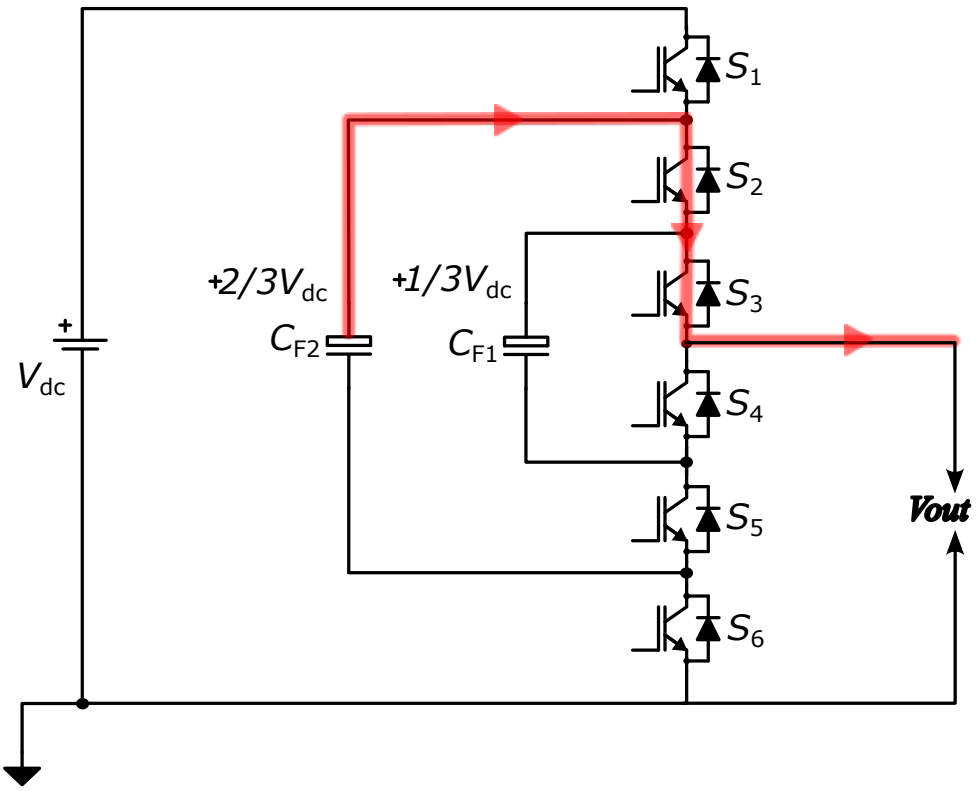

Figure 2.3: second switching state operation of $4L$ FC converter.

2.1.3 State 3

State 3 represents a specific switching configuration of the FC converter, as illustrated in Figure 2.4. The topology for this converter consists of 6 switches from S_1 through S_6 in a leg clamped though the FCs C_{F1} and C_{F2}. The voltage across the FCs is distributed precisely, where upper FC has maintain a voltage of $2/3V_{dc}$, while lower FC maintain a voltage $1/3V_{dc}$ of the total DC-link voltage. This voltage division of total DC-link voltage is very essential to achieve levels of the total output voltage. In this state of converter a particular combination of the switches is activated by PWM creating a defined conduction conduction path through the converter. In this switching state of FC converter, the IGBTs S_1, S_5 and S_3 remain turned on, while other remaining IGBTs will be complementary to these IGBTs. In this state FC C_{F2} gets charged from the battery and C_{F1} will be discharged into the load. The current follow the path from battery, to C_{F2} to C_{F1} and the to the load. The other complementary IGBTs perform switching as per the operation of these IGBTs. Because of the conduction of S_1 and S_3 the load the voltage remains at level of $2V_{dc}/3$ the same as that of state 2 but this state is the redundant of second state. The switches

that are turned-off during this state are S_2, S_4 and S_6 and each have voltage stress of $V_{dc}/3$.

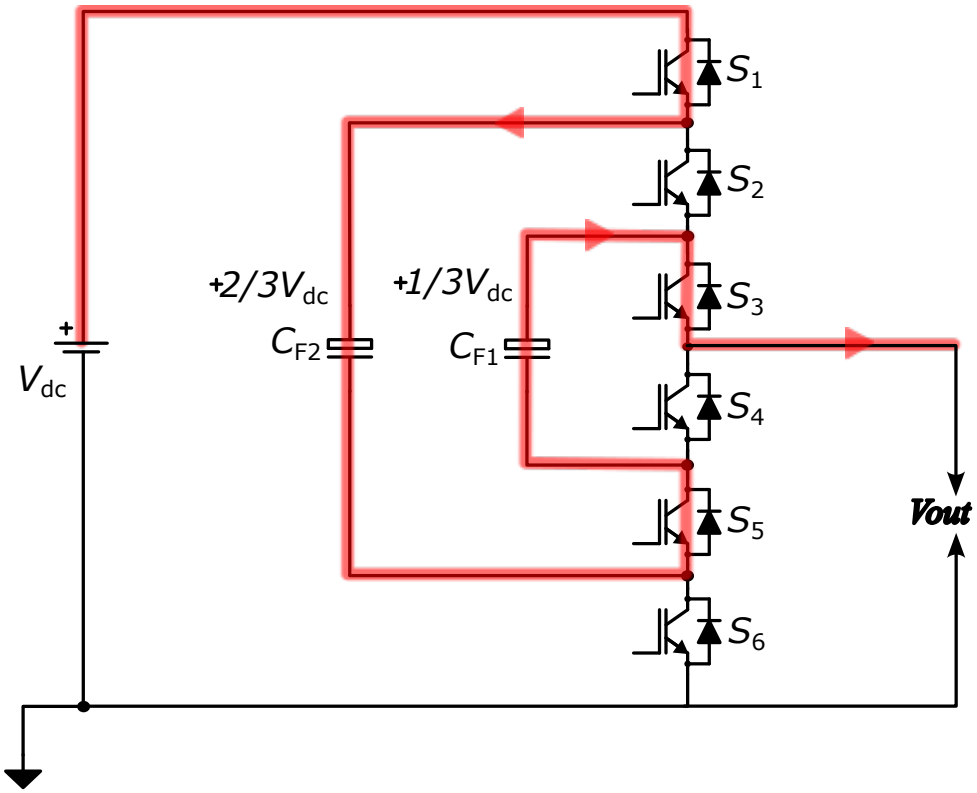

Figure 2.4: third switching state operation of $4L$ FC converter.

2.1.4 State 4

State 4 represents a specific switching configuration of the FC converter, as illustrated in Figure 2.5. The topology for this converter consists of 6 switches from S_1 through S_6 in a leg clamped though the FCs C_{F1} and C_{F2}. The voltage across the FCs is distributed precisely, where upper FC has maintain a voltage of $2/3V_{dc}$, while lower FC maintain a voltage $1/3V_{dc}$ of the total DC-link voltage. This voltage division of total DC-link voltage is very essential to achieve levels of the total output voltage. In this state of converter a particular combination of the switches is activated by PWM creating a defined conduction conduction path through the converter. While following the path, the IGBTs $S1$, S_2 and S_4 will be turned on to get the required output voltage during this state, while other remaining IGBTs will be complementary to these IGBTs. In this state only, FC CF1 gets charged from the battery and CF2 will have no effect of charging discharging into the load. The current follow the path from battery, to CF1 and then to the load. Because of

the conduction of S_1, S_2 and S_4 the load the voltage remains at level of $2V_{dc}/3$ again is the redundant of the state 2. The switches that are turned-off during this state are S_3, S_5 and S_6 and have voltage stress of $V_{dc}/3$.

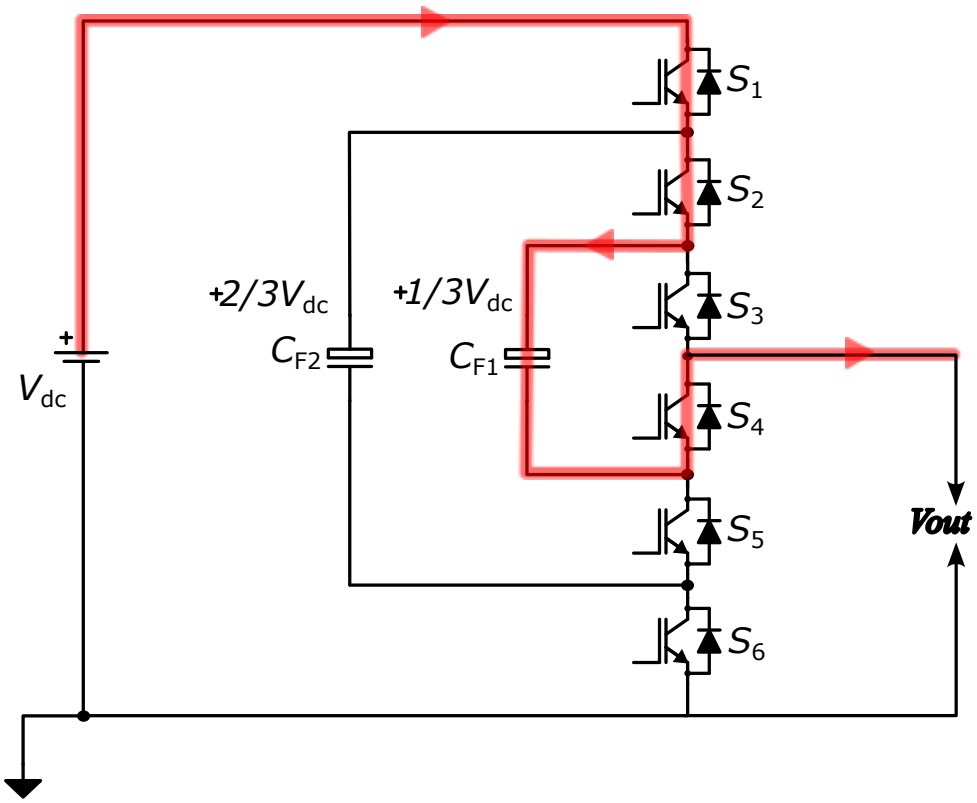

Figure 2.5: fourth switching state operation of $4L$ FC converter.

2.1.5 State 5

In this switching state of FC converter, the IGBTs S_1, S_4 and S_5 will be turned on to get the required output voltage during this state, while other remaining IGBTs will be complementary to these IGBTs. In this state only, FC C_{F2} gets charged from the battery and C_{F1} will have no effect of charging discharging into the load. The current follow the path from battery, to C_{F1} and then to the load. Because of the conduction of S_1, S_5 and S_4 the load the voltage remains at level of $V_{dc}/3$. The switches that are turned-off during this state are S_2, S_3 and S_6 and each have maximum voltage stress of $V_{dc}/3$.

2.1.6 State 6

In this switching state of FC converter, the IGBT S_3, S_5 and S_6 will be turned on to get the required output voltage during this state, while other remaining IGBTs will be

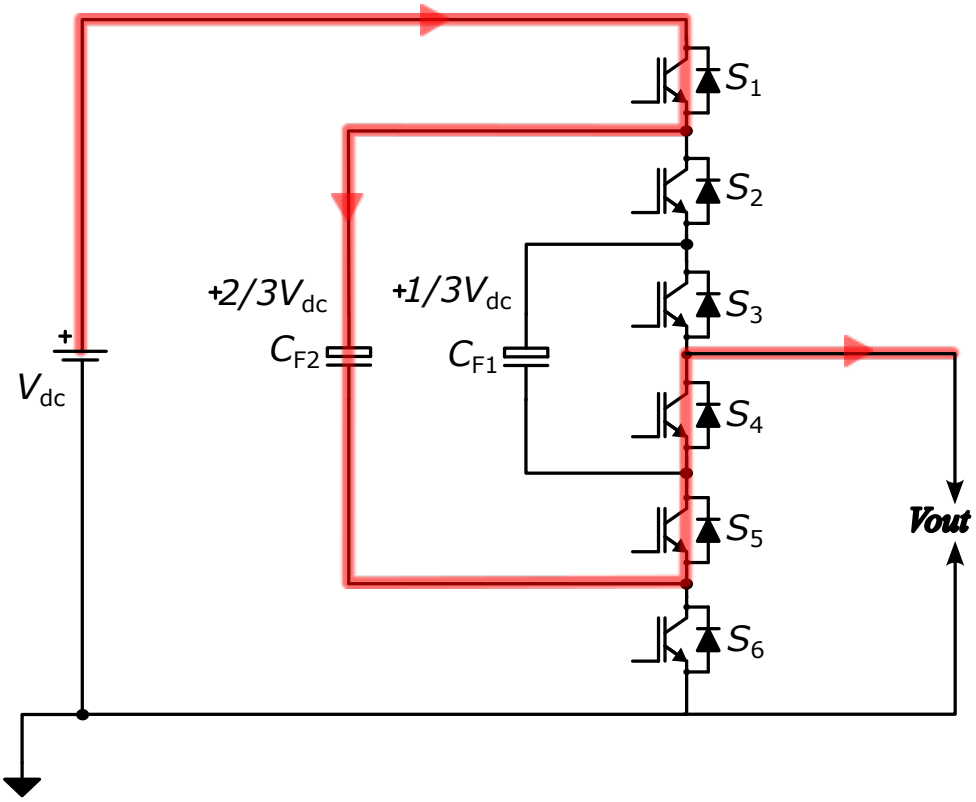

Figure 2.6: fifth switching state operation of $4L$ FC converter.

complementary to these IGBTs. In this state only, FC C_{F1} gets discharged and C_{F2} will have no effect of charging or discharging into the load. The current follow the path from battery, to C_{F1} and then to the load. Because of the conduction of S_3 , S_5 and S_6 the load the voltage remains at level of $V_{dc}/3$. The switches that are turned-off during this state are S_1, S_2 and S_4 and each have maximum voltage stress of $V_{dc}/3$.

2.1.7 State 7

In this switching state of FC converter, the IGBT S_2, S_4 and S_6 will be turned on to get the required output voltage during this state, while other remaining IGBTs will be complementary to these IGBTs. In this state only, FC C_{F1} gets charged and C_{F2} will be discharging. The current follow the path from battery, to C_{F2} and then to the load. Because of the conduction of S_2, S_4 and S_6 the load the voltage remains at level of $V_{dc}/3$. The switches that are turned-off during this state are S_1, S_3 and S_5 and each have maximum voltage stress of $V_{dc}/3$.

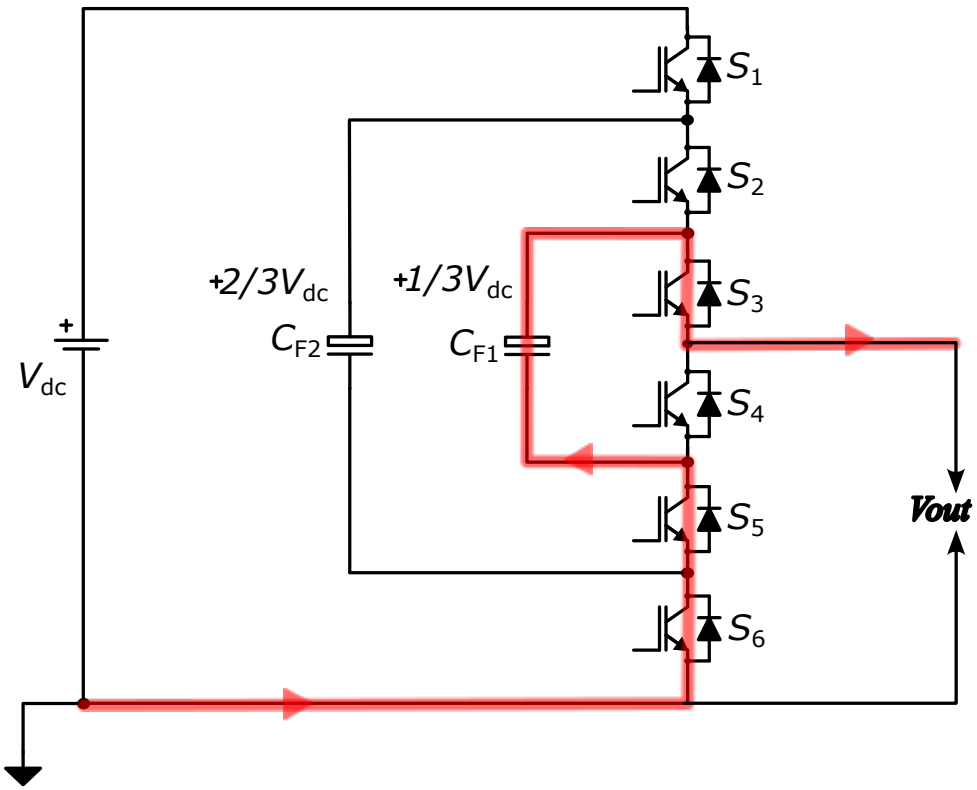

Figure 2.7: sixth switching state operation of $4L$ FC converter.

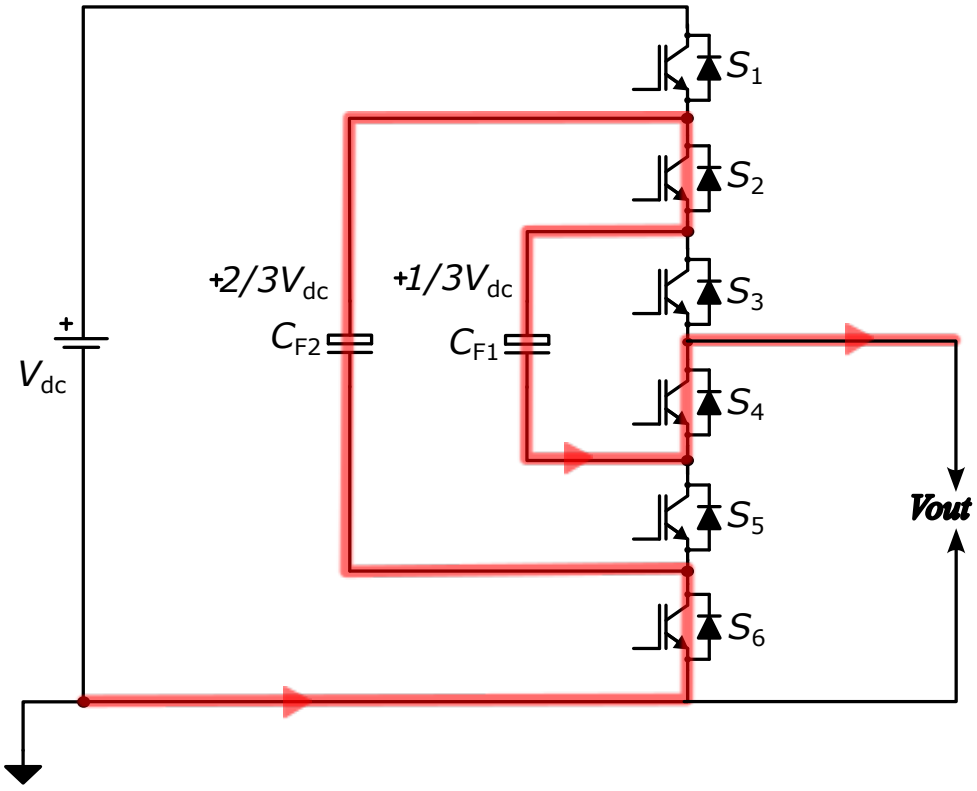

Figure 2.8: seventh switching state operation of $4L$ FC converter.

2.1.8 State 8

This switching state is the total complementay to the first state because it gives same but negative voltage as that of the first state of FC converter. The IGBT S_4, S_5 and S_6 will be turned on to get the required output voltage during this state, while upper 3 IGBTs will be complementary to these IGBTs. In this state only, the FC C_{F1} and C_{F2} will have no effect of charging or discharging into the load and negative peak voltage appears across the load. The current follow the path from batter to the load directly through turned on IGBTs. Because of the conduction of S_4, S_5 and S_6 the load the voltage remains at level of $0V$. The switches that are turned-off during this state are S_1, S_2 and S_3 and each have maximum voltage stress of $V_{dc}/3$.

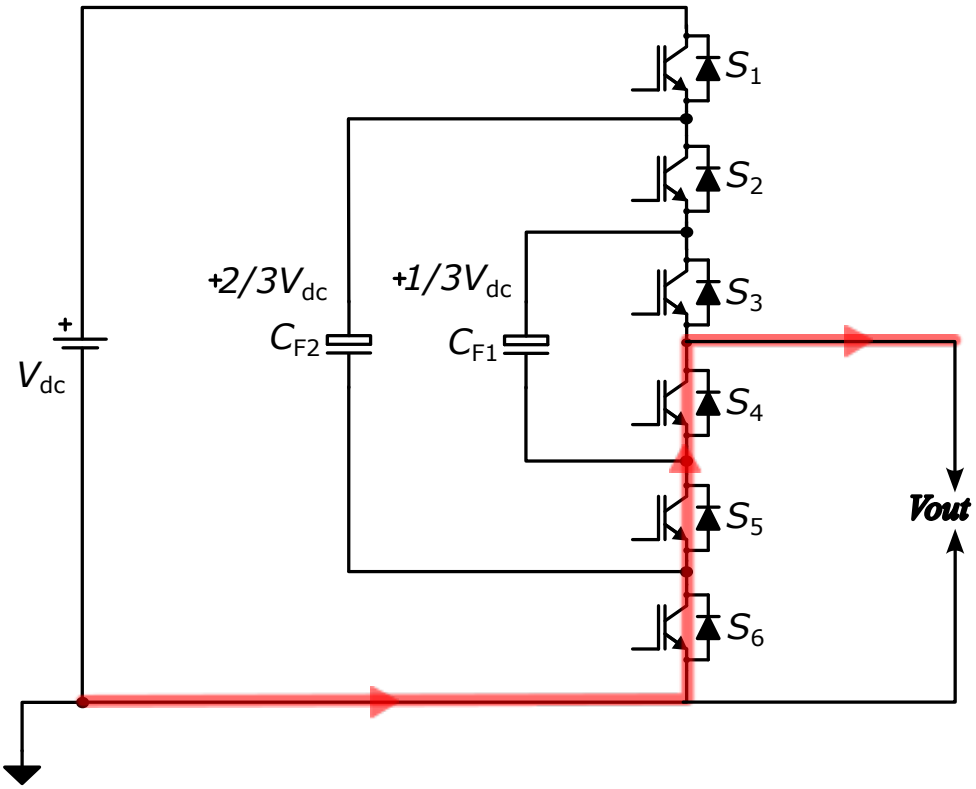

Figure 2.9: Eighth switching state operation of $4L$ FC converter.

2.2 Neutral-Point Clamped Multilevel Converter

The diode clamped multilevel converter was proposed earlier than other multilevel converter topologies in 1981 and can be used in applications like motor drives where

lower voltage ripple THD are required and in integrating the RESs with the gird [6]. The Figure 2.10 shows the circuit diagram of 3-phase 3-level NPC converter. The two DC-link capacitors connected at input of a NPC converter split the DC input voltage (V_{dc}) and get the mid of supplied voltage. The common point of the DC-link capacitors is connected to the ground, therefore the converter is named after that, is neutral point clamped converter. In order to obtain the different levels of voltage in NPC converter, the clamping diodes D_{1x} and D_{2x} are used. There are three operating modes of this topology. The first

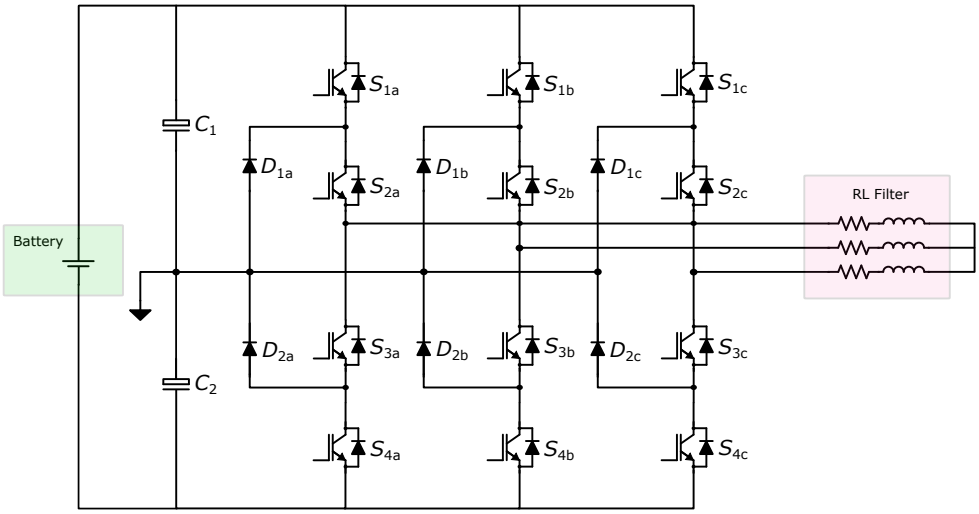

Figure 2.10: Basic topology of $3\phi 3L$ NPC converter.

operating mode produce the positive half of voltage, second operating mode creates zero or no voltage and third operating mode creates negative half of voltage. The each operating mode of the 3-level converter has current flowing either in positive of negative direction.

2.2.1 State 1

In this state of the converter, each leg comprises four active switches (S_{1a}, S_{2a}, S_{3a}, S_{4a}) arranged in series, each with an anti-parallel freewheeling diode. These switches, typically maybe IGBTs or MOSFETs, control the voltage level at the output terminal. Two clamping diodes (D_{1a} and D_{2a}) connect the circuit to the neutral point and are fundamental to the NPC topology, enabling access to the intermediate voltage level while ensuring that each switch experiences only half the DC-link voltage stress. The DC-link consists of two series-connected capacitors (C_1 and C_2) that divide the voltage V_{dc} equally, with their junction forming the neutral point at potential $V_{dc}/2$. In the Figure 2.11 switch-

ing state, switches S_{1a} and S_{2a} are turned on, connecting the output terminal to the positive DC rail. The current path, highlighted in red, shows positive current $I > 0$ flowing from the positive DC rail through the closed switches S_{1a} and S_{2a} to the output terminal. This configuration produces an output voltage of $+V_{dc}/2$ with respect to the negative DC rail. In this state, switches S_{3a} and S_{4a} remain off, and the clamping diodes are reverse-biased and do not conduct. Each of the inactive switches (S_{3a} and S_{4a}) blocks a voltage of $V_{dc}/2$, demonstrating the voltage-sharing characteristic of the NPC topology.

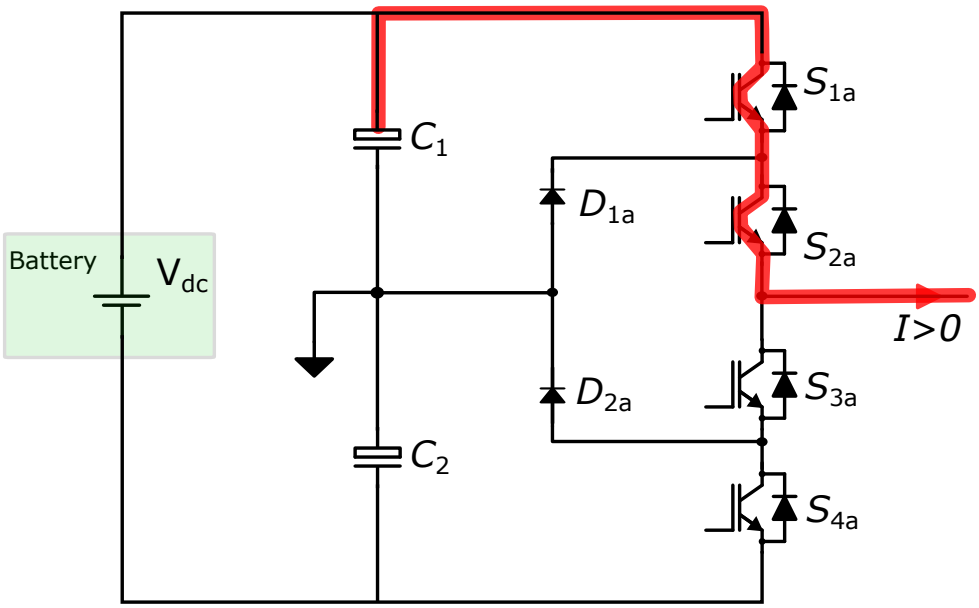

Figure 2.11: Per phase sub circuit of $3\phi 3L$ NPC converter during $+V_{dc}/2$ and $I > 0$.

2.2.2 State 2

In this state of the converter, two clamping diodes (D_{1a} and D_{2a}) provide the essential connection to the neutral point formed by the junction of two series-connected DC-link capacitors (C_1 and C_2). These clamping diodes are fundamental to the NPC topology, allowing the output to access the midpoint voltage while ensuring that each switch experiences only half the DC-link voltage stress during blocking states. In the depicted switching state, the inner switches S_{2a} or S_{3a} are turned on while the outer switches S_{1a} and S_{4a} remain off. The current path, highlighted in red, shows positive current I>0 flowing from the neutral point through clamping diode D_{1a} and closed switch S_{2a} to the output terminal. This configuration produces an output voltage of zero ($0V$) with respect to the neutral point, or equivalently $V_{dc}/2$ with respect to the negative DC rail. The posi-

tive current direction determines that D_{1a} conducts to provide the path from the upper capacitor C_1 to the output, while D_{2a} remains reverse-biased. During this state, switch S_{1a} blocks voltage $V_{dc}/2$ from capacitor C_1, and switch S_{4a} blocks voltage $V_{dc}/2$ from capacitor C_2.

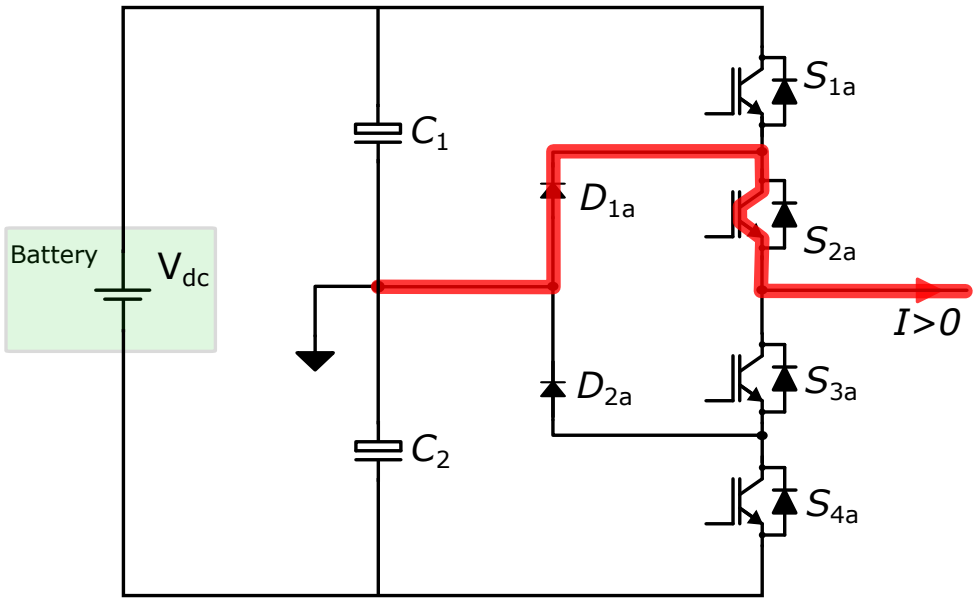

Figure 2.12: Per phase sub circuit of $3\phi 3L$ NPC converter during $0V$ and $I > 0$.

2.2.3 State 3

All active switches of this converter are arranged in series, each with an anti-parallel freewheeling diode. Two clamping diodes (D_{1a} and D_{2a}) provide connection to the neutral point formed by the junction of two series-connected DC-link capacitors (C_1 and C_2). These capacitors divide the voltage V_{dc} equally, with their midpoint serving as the reference for the intermediate voltage level that characterizes the NPC topology. In the depicted switching state, the lower switches S_{3a} and S_{4a} are turned on while the upper switches S_{1a} and S_{2a} remain off. The current path, highlighted in red, shows positive current $I > 0$ flowing from the output terminal through closed switches S_{3a} and S_{4a} to the negative DC rail, and returning through the lower capacitor C_2 to complete the circuit. This configuration produces an output voltage of -$V_{dc}/2$ with respect to the neutral point, or equivalently $0V$ with respect to the negative DC rail. In this state, the clamping diodes D_{1a} and D_{2a} are reverse-biased and do not conduct. The inactive upper switches S_{1a} and S_{2a} block voltages from the DC-link, with S_{1a} blocking the full voltage across C_1 and

S_{2a} blocking the combined voltage contribution from its position in the series string.

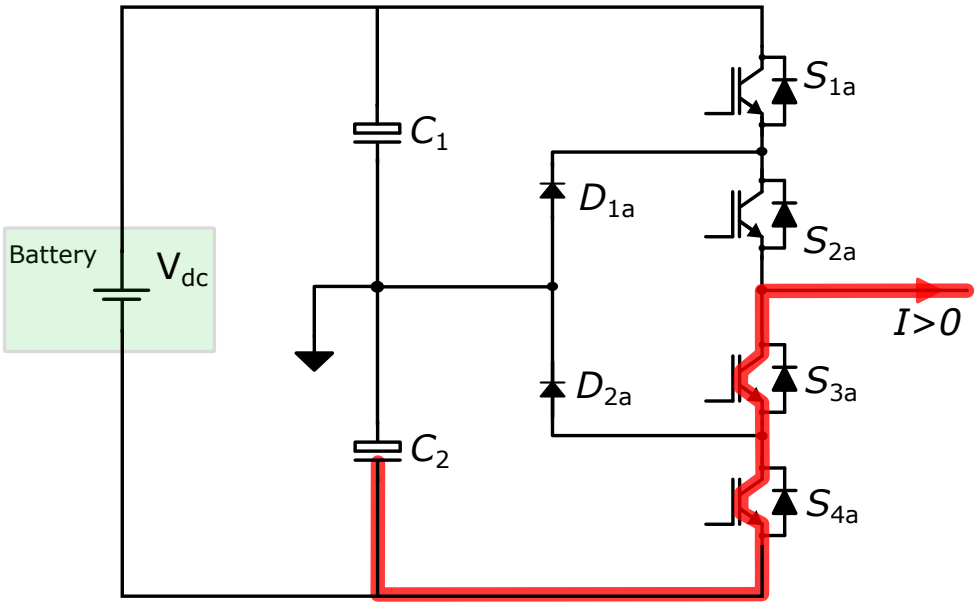

Figure 2.13: Per phase sub circuit of $3\phi 3L$ NPC converter during $-V_{dc}/2$ and $I > 0$.

A Table 2.2 is created to represent the switching states, output voltage and current flowing through the semiconductors for 3-level NPC converter.

	V_{AO}	S_1	D_1	S_2	D_2	S_3	D_3	S_4	D_4	D_5	D_6
$i >= 0$	$V_{dc}/2$	1		1							
i >= 0	0			1						1	
$i >= 0$	$-V_{dc}/2$						1		1		

Table 2.2: Switching of semiconductors, current and load voltage during operation of $3\phi 3LNPC$ converter

2.2.4 State 4

The converter leg comprises four active switches arranged in series, each with an anti-parallel freewheeling diode. Two clamping diodes (D_{1a} and D_{2a}) provide connection to the neutral point formed by the junction of two series-connected DC-link capacitors (C_1 and C_2). These capacitors divide the voltage V_{dc} equally, with their midpoint serving as the reference for the intermediate voltage level that characterizes the NPC topology. In the depicted switching state, switches S_{1a} and S_{2a} are turned on while switches S_{3a} and S_{4a} remain off. However, unlike the positive current case, the current direction is now reversed with $I < 0$, meaning current flows into the output terminal rather than out of

it. The current path, highlighted in red, shows negative current flowing from the output terminal through the anti-parallel freewheeling diodes of switches S_{2a} and S_{1a} to the positive DC rail, and then returning through upper capacitor C_1 to complete the circuit. Despite the switches S_{1a} and S_{2a} being in the on-state, the actual current conduction occurs through their body diodes due to the reverse current direction. This configuration still produces an output voltage of $+V_{dc}/2$ with respect to the negative DC rail, maintaining the same voltage level as in the positive current case with the same switching state.

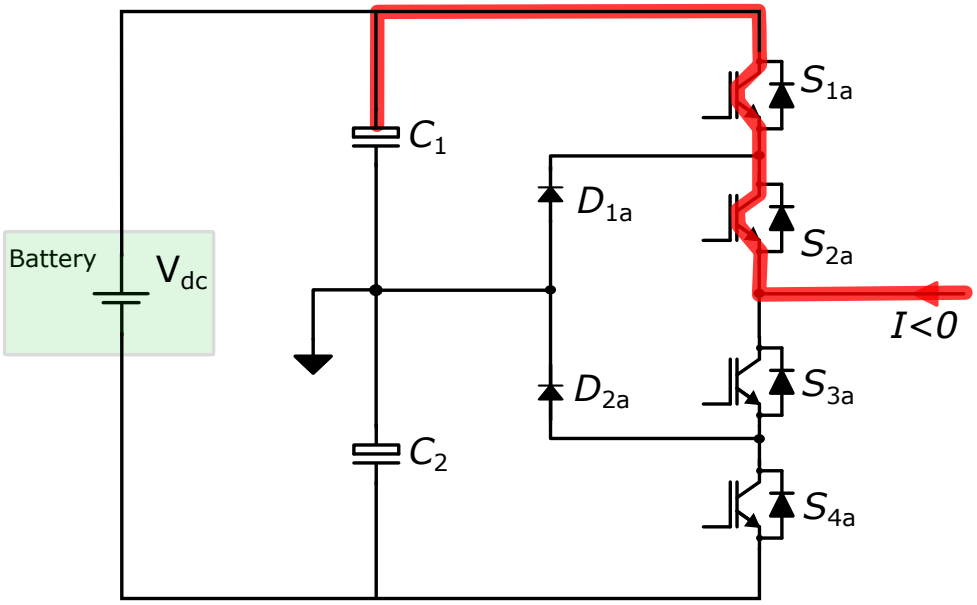

Figure 2.14: Per phase sub circuit of $3\phi 3L$ NPC converter during $+V_{dc}/2$ and $I < 0$.

2.2.5 State 5

The converter leg comprises four active switches arranged in series, each with an anti-parallel freewheeling diode. Two clamping diodes (D_{1a} and D_{2a}) provide the essential connection to the neutral point formed by the junction of two series-connected DC-link capacitors (C_1 and C_2). These clamping diodes enable access to the intermediate voltage level, and their conduction behavior is inherently dependent on the direction of current flow through the converter.In the depicted switching state, the inner switches S_{2a} and S_{3a} are turned on while the outer switches S_{1a} and S_{4a} remain off. With negative current $I < 0$ flowing into the output terminal, the current path, highlighted in red, shows current entering from the output terminal, flowing through the anti-parallel freewheeling diode

of switch S_{3a}, then through clamping diode D_{2a} to reach the neutral point, and finally returning through lower capacitor C_2 to complete the circuit. This configuration produces an output voltage of zero ($0V$) with respect to the neutral point. The negative current direction determines that D_{2a} conducts to provide the path to the neutral point, while D_{1a} remains reverse-biased and does not conduct.

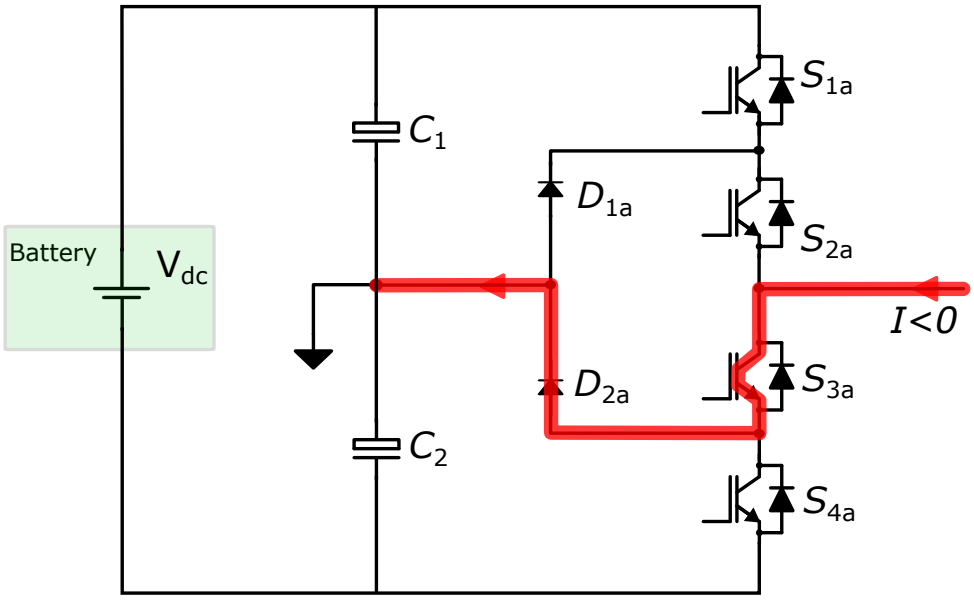

Figure 2.15: Per phase sub circuit of $3\phi 3L$ NPC converter during $0V$ and $I < 0$.

2.2.6 State 6

The converter leg comprises four active switches arranged in series, each with an anti-parallel freewheeling diode. Two clamping diodes (D_{1a} and D_{2a}) provide connection to the neutral point formed by the junction of two series-connected DC-link capacitors (C_1 and C_2). These capacitors divide the voltage V_{dc} equally, maintaining the voltage levels necessary for three-level operation. In the depicted switching state, the lower switches S_{3a} and S_{4a} are turned on while the upper switches S_{1a} and S_{2a} remain off. However, with negative current $I < 0$ flowing into the output terminal, the current path, highlighted in red, shows current entering from the output terminal and flowing through the anti-parallel freewheeling diodes of switches S_{3a} and S_{3a} to the negative DC rail, then returning through lower capacitor C_2 to complete the circuit. Despite switches S_{3a} and S_{4a} being commanded on, the actual current conduction occurs through their body diodes due to the reverse current direction. This configuration produces an output voltage of

$-V_{dc}/2$ with respect to the neutral point, maintaining the same negative voltage level as would occur with positive current through the same switching state.

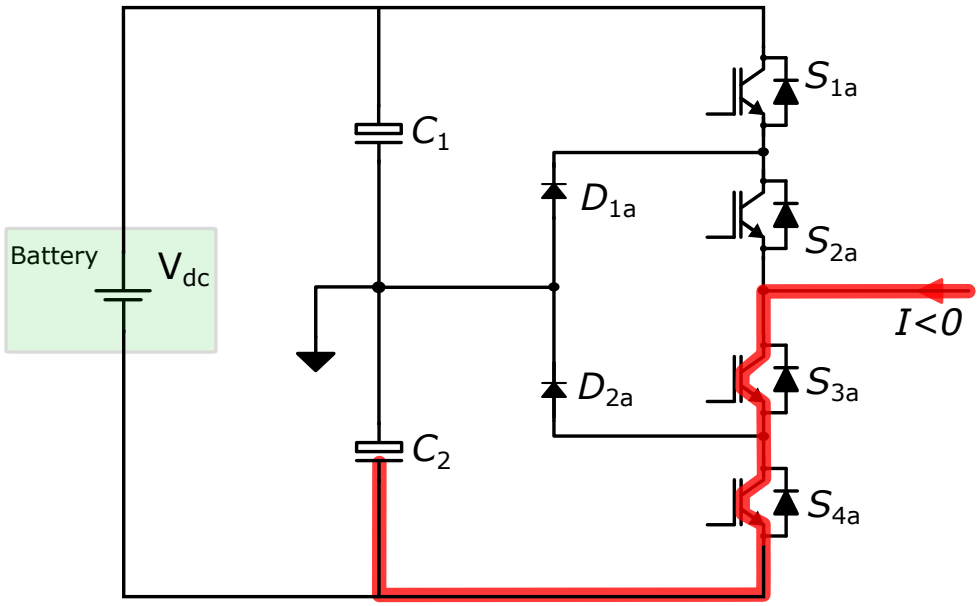

Figure 2.16: Per phase sub circuit of $3\phi 3L$ NPC converter during $-V_{dc}/2$ and $I < 0$.

	V_{AO}	S_1	D_1	S_2	D_2	S_3	D_3	S_4	D_4	D_5	D_6
$i < 0$	$V_d/2$		on		on						
$i < 0$	0					on					on
$i < 0$	$-V_d/2$					on		on			

Table 2.3: Switching of semiconductors, current and load voltage during per phase operation of $3\phi 3LNPC$ converter

The number of output voltage levels depends on number of DC-link capacitors, clamping diodes, and IGBTs of the topologies. An additional pair of complementary IGBTs with DC-link capacitor and clamping diodes increases with an increase of one extra level of output voltage. The main issue here in this converter is the cost and the high voltage ratings of the clamping diodes and balancing of voltage across each DC-link capacitor [7]. For a 3-level NPC converter, only two IGBTs will be turned on instantaneously and other two will remain turned off to get the three levels of output voltage. If 7-level NPC converter compared with $3\phi 7LM_LM_X$ converter and 7-level FC converter, the 7-level NPC converter has series of 6 DC-link capacitors, and maintaining balanced voltages between them gets progressively challenging at higher levels. In contrast, the FC architecture benefits from redundant switching states, which allow for more natural or self-balancing of

its FCs, making it easier to handle without additional hardware.

2.3 Multiplexed Multilevel Converter

The $3\phi 7LM_LM_X$ converter is used for medium voltage application like motor drives, integrating RESs with the grid and is presented in [8], incorporates two $3\phi 4L$ FC converters and one $3\phi 3L$ NPC converter to achieve seven voltage levels. In this topology, the two $3\phi 4L$ FC converters generate the positive and negative half cycles of the waveform, while the $3\phi 3L$ NPC converter combines these half cycles to produce a continuous sinusoidal output. The $3\phi 7LM_LM_X$ converter has 24 switches, which are the combination of a $3\phi 3L$ NPC converter and two $3\phi 4L$ FC converter topologies. The first $3\phi 4L$ FC converter on top manages the voltage on the top side of the power converter, while the second $3\phi 4L$ FC converter on the bottom manages the voltage on the lower side of the converter as shown in Figure 2.17.

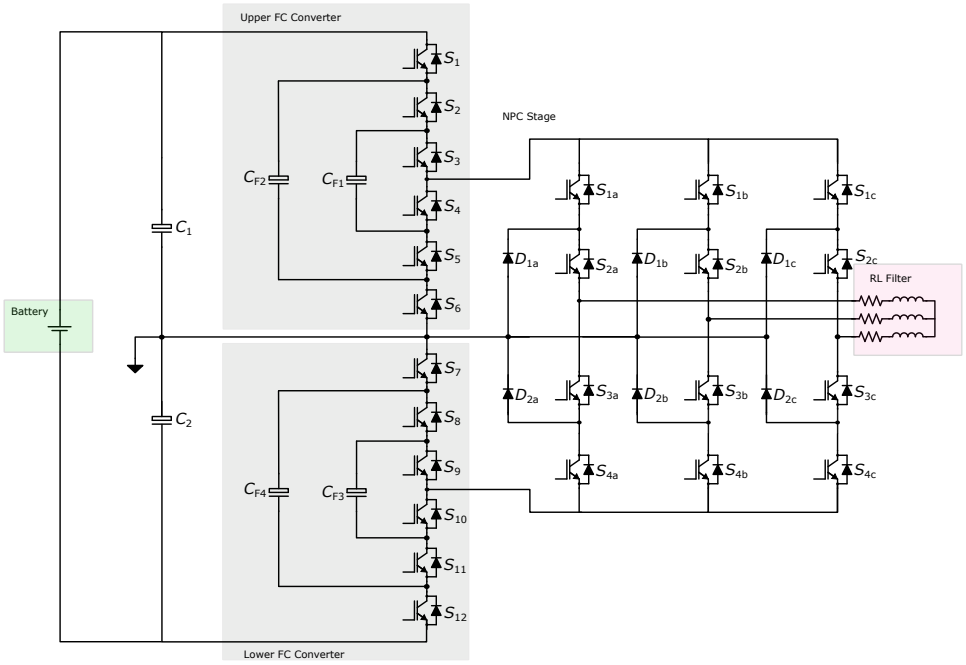

Figure 2.17: Topology of $3\phi 7LM_LM_X$ converter.

Consequently, the top side FC converter and bottom side FC converter of $3\phi 7LM_LM_X$ converter, generate positive and negative half-cycles of output AC voltage, respectively. The NPC stage of $3\phi 7LM_LM_X$ functions as a multiplexer to generate the complete AC sine wave by combining positive and negative half cycles generated from FCC stages, giving

rise to the term multiplexed multilevel converter. Four voltage levels are offered by both top and bottom FCs for the $3\phi 4L$ FC converters. The FCs for $3\phi 4L$ FC converter generates voltage levels of: 0, $1/2\text{V}_{dc}$, $1/3\text{V}_{dc}$, and $1/6\text{V}_{dc}$, which generate the same levels of voltages at the output of upper FCC which are: 0, $1/2\text{V}_{dc}$, $1/3\text{V}_{dc}$, and $1/6\text{V}_{dc}$, and negative voltage levels 0, $-1/2\text{V}_{dc}$, $-1/3\text{V}_{dc}$, and $-1/6\text{V}_{dc}$ on the bottom side of FC converter. As a result, the 3ϕ NPC converter will generate 7-levels of output voltage (0, $\pm 1/2\text{V}_{dc}$, $\pm 1/3\text{V}_{dc}$, and $\pm 1/6\text{V}_{dc}$). The main advantage of this topology is the absence large number of DC-link capacitors (C_1 and C_2) between the FC converter stage and NPC stage.

2.3.1 Operation of Multiplexed Multilevel Converter

The operation of the $3\phi 7LM_LM_X$ converter can be understood by examining the direction of current flow in different switching states, particularly during specific modulation sectors of the converter. There are 10 switching sectors are selected for $3\phi 7LM_LM_X$ converter depending on the transitions of the switching voltages in each phase of the converter. In following subsection the all ten switching sectors of $3\phi 7LM_LM_X$ converter are explained and illustrated with Figures. These diagrams help explain how the converter synthesizes the required output voltages and ensures smooth commutation between switching states while minimizing switching losses. The three positive levels of output voltages are produced at the output of upper FC converter, while three negative levels of output voltage levels are produced at the output of the lower FC converter stage, $3\phi 3L$ NPC multiplexed the positive and negative three level voltages of both upper and lower FC converters and generates an output of seven levels of voltage.

2.3.1.1 Sector 1 of $3\phi 7LM_LM_X$ converter

In this sector, the reference voltage of Phase A is near zero and begins to increase positively, while Phase B and Phase C are in negative and positive regions, respectively. The instantaneous switching voltages are:

$$\begin{aligned} V_A(sw) &= 0 \rightarrow +\frac{1}{6}V_{dc} \\ V_B(sw) &= -\frac{1}{3}V_{dc} \rightarrow -\frac{1}{2}V_{dc} \\ V_C(sw) &= +\frac{1}{3}V_{dc} \rightarrow +\frac{1}{6}V_{dc} \end{aligned} \tag{2.3}$$

This sector represents the initial region of the positive half-cycle for Phase A, where its voltage begins to rise from zero. Two main current flow conditions are identified in this sector:

At this instant, the output of Phase A is maintained at zero volts. The NPC leg of Phase A is clamped to the neutral point through the lower clamping diode, so the phase current of Phase A flows through this diode and returns to the neutral point of the converter. Although the top FC stage of converter sustains a voltage of $+\frac{1}{3}V_{BUS}$ and feeds the phase of the NPC stage, this voltage is not applied to the load because of the clamped condition. Across the phase B a negative voltage of approximately $-\frac{1}{3}V_{dc}$ appears and its current therefore flows from the load back into the converter, through the lower FC stage and NPC lower leg, to the negative DC bus. Conversely, Phase C delivers a positive voltage of $+\frac{1}{3}V_{dc}$ and its current flows from the positive DC bus, through the upper FC stage and upper NPC switches, and out to the load. Thus, in this switching state of the converters, Phase C acts as the source supplying the current to the load side, Phase B acts as the sink returning current to the lower DC bus, and Phase A remains in the neutral clamped state completing the current loop through its clamped diodes as shown in Figure 2.18.

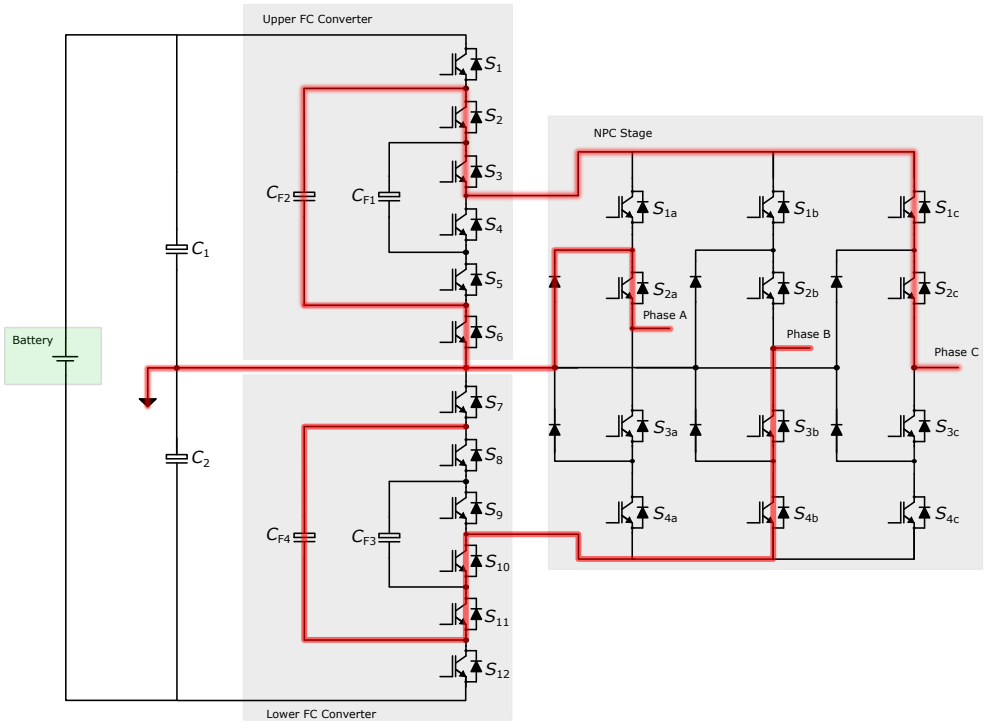

Figure 2.18: Switching operation of $3\phi 3L$ NPC converter during sector 1a.

As the modulation reference of Phase A increases, the switch (S_{1a}) of the NPC stage

turn on, connecting the output of phase A to the intermediate voltage of $+\frac{1}{6}V_{dc}$. The current of Phase A now flows from the positive of C_{F2} and upper NPC switches (S_{1a} and S_{2a}) to the phase of load. In this state, Phase C continues to operate at $+\frac{1}{3}V_{dc}$ it still delivers current from the positive DC bus, while Phase B remains at $-\frac{1}{2}V_{dc}$ it receives the returning current through its lower FC converter. Consequently, the three phases together form a balanced current path from the upper DC bus (through Phases A and C) to the lower DC bus (through Phase B). The commutation of current in Phase A from the clamping diode to the conducting switches occurs under low-current conditions, thereby minimizing switching losses and ensuring smooth transition between voltage levels. The switching circuit is shown in Figure 2.19

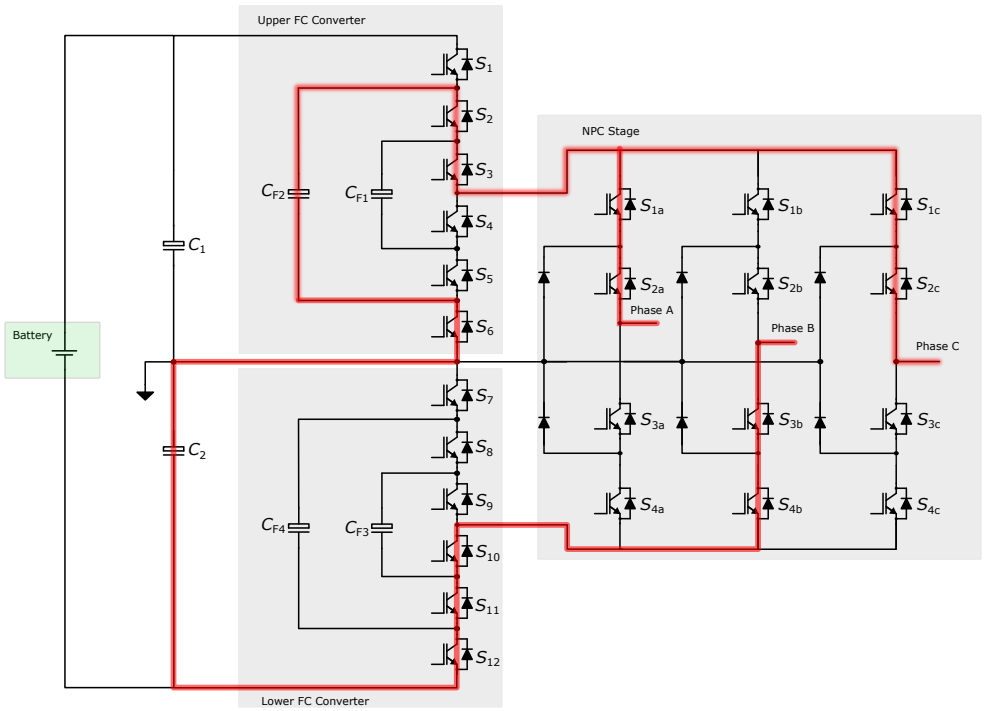

Figure 2.19: Switching operation of $3\phi 3L$ NPC converter during sector 1b.

2.3.1.2 Sector 2 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= +\frac{1}{6}V_{dc} \rightarrow +\frac{1}{3}V_{dc} \\ V_B(sw) &= -\frac{1}{6}V_{dc} \rightarrow -\frac{1}{3}V_{dc} \\ V_C(sw) &= +\frac{1}{6}V_{dc} \rightarrow 0 \end{aligned} \tag{2.4}$$

In sector 2 of the $3\phi 7LM_LM_X$ converter, as illustrated in Figures below, the system operates within the reference voltage window corresponding to a transition from the one voltage of converter up to the other positive level of output voltage of Phase A, while Phases B and C occupy distinct roles in each state. This sector features two fundamental switching states, each impacting current flow and capacitor utilization differently:

State 1:

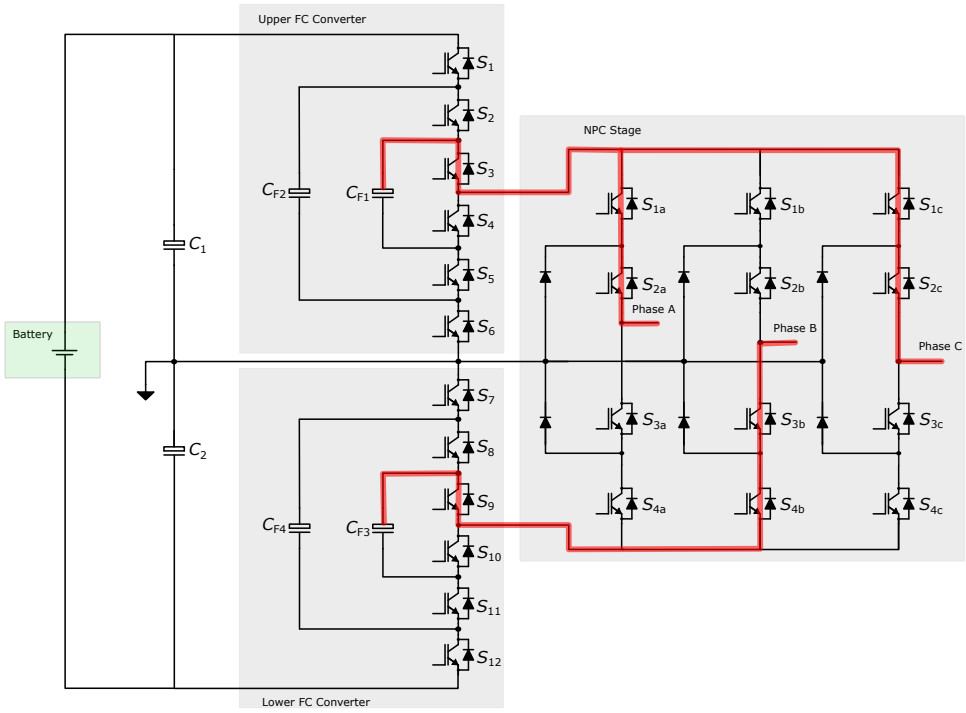

Figure 2.20: Switching operation of $3\phi 3L$ NPC converter during sector 2a.

The switching operation of first state of Sector 2 is shown in Figure 2.20. Phase A is progressing towards its positive peak as the voltage is rise from zero towards the peak voltage. The phase current from A comes from the the upper FC converter stage and holds a voltage of $+\frac{1}{6}V_{dc}$, though it is not directly delivered to the load. At the same time, Phase B is sending return current from the load to a negative output of FC with voltage stress of $-\frac{1}{6}V_{dc}$ by returning current to the negative DC bus via its lower FC converter stage. Phase C, on the other hand, delivers a positive output at $+\frac{1}{6}V_{dc}$, with current sourced from the positive DC bus and conducted through its FCs of upper FC stage and NPC switches (S_{1c} and S_{2c}) to the phase C of the load. Thus, in this first state, the converter ensures smooth supply of positive and negative voltages to the load while maintaining FCs voltages balanced.

State 2:

During the second state of Sector 2, by Phase A make a transition from one voltage level to another, releasing its switch and enabling the FCs of top FC's stage output to be synthesized at the load. This allows Phase A to rise from $+\frac{1}{6}V_{dc}$ up to $+\frac{1}{3}V_{dc}$, with the phase current now flows through the upper FC converter stage and corresponding phase switches of NPC stage to reach at the load. The phase voltage at the output is thus rise from $+\frac{1}{6}V_{dc}$ to $+\frac{1}{3}V_{dc}$ and delivered to the load, actively engaging the FCs in charge or discharge dynamics for voltage balancing across the FCs. Meanwhile, Phase B continues as before with rise of negative output voltage of $-\frac{1}{6}V_{dc}$ to $-\frac{1}{3}V_{dc}$, and Phase C clamped to the neutral point of $3\phi 7LM_XM_L$ converter and has zero output voltage at the load side as shown in Figure 2.21.

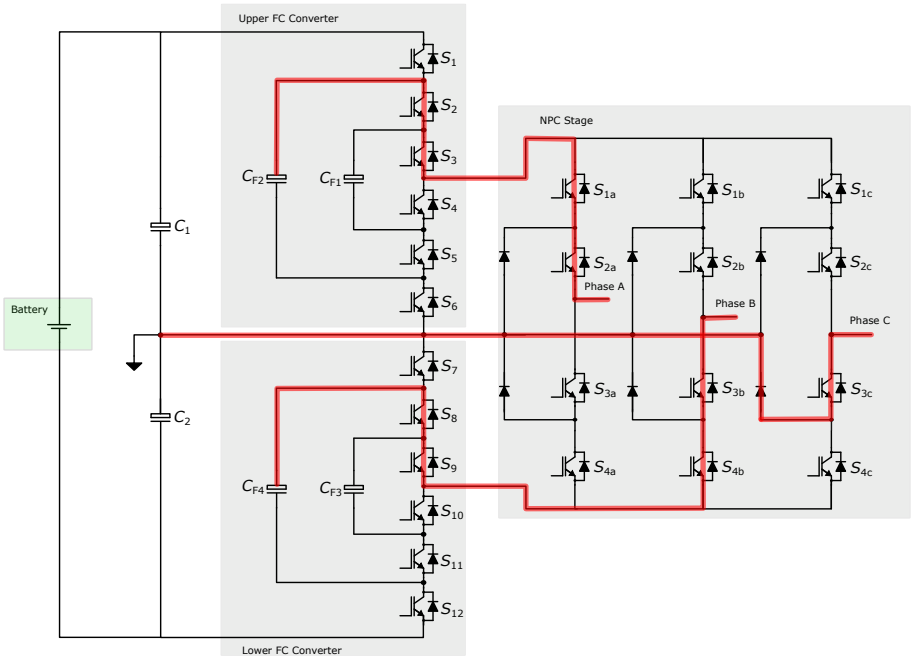

Figure 2.21: Switching operation of $3\phi 3L$ NPC converter during sector 2b.

2.3.1.3 Sector 3 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= +\frac{1}{3}V_{dc} \rightarrow +\frac{1}{2}V_{dc} \\ V_B(sw) &= -\frac{1}{6}V_{dc} \rightarrow 0 \\ V_C(sw) &= -\frac{1}{6}V_{dc} \rightarrow 0 \end{aligned} \tag{2.5}$$

State 1:

With Phase A's reference between $+\frac{1}{3}V_{dc}$, one FC that is C_{F2} in upper FC stage with S_2, S_3 switches and first leg of NPC stage with switches S_{1a} and S_{2a} are engaged to synthesize $+\frac{1}{3}V_{dc}$ at the output. For phase B and C both have the same voltage of $-\frac{1}{6}V_{dc}$ by turning on the switch S_{10} from lower FC converter stage and switches S_{3b}, S_{4b}, S_{3c} and S_{4c} in NPC stage. The current flow direction follows the paths of switches that are turned on during the operation as shown in Figure 2.22.

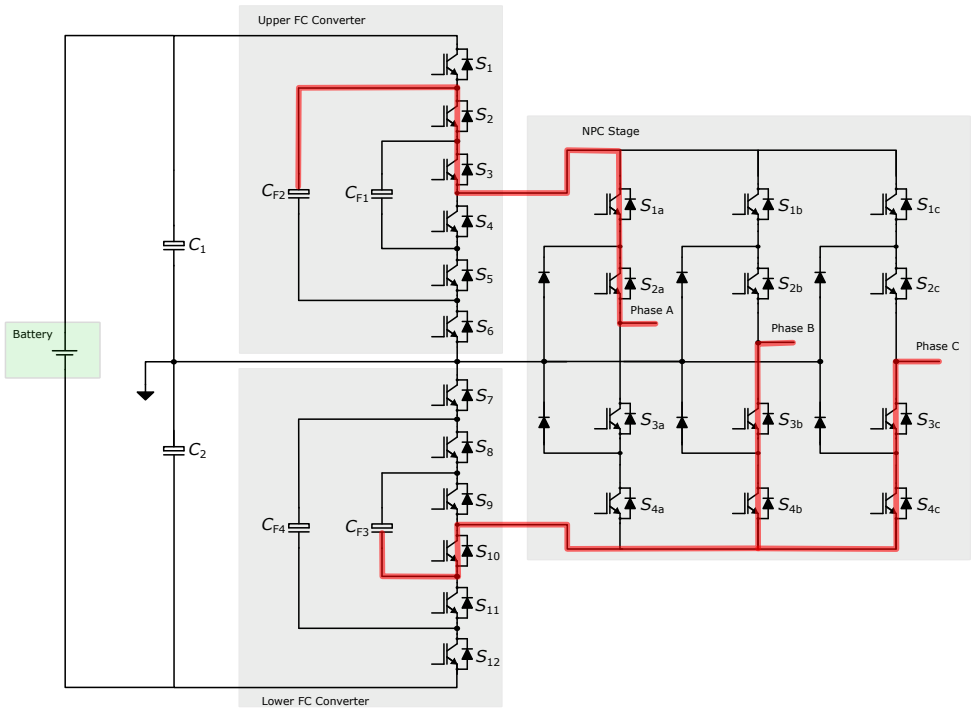

Figure 2.22: Switching operation of $3\phi 3L$ NPC converter during sector 3a.

State 2: In phase A, during second switching state in sector 3 output voltage is changed from $+\frac{1}{3}V_{dc}$ to $+\frac{1}{2}V_{dc}$ by turning on a S_1 switch from upper FC converter stage. Phase B and Phase C make a transition from $-\frac{1}{6}V_{dc}$ to $0V$ by clamping to neutral point of the converter through specific clamping diodes as illustrated in Figure 2.23. A brief redundant state may be present as the output transitions from FC conduction to NPC clamping approaching zero crossing. Modulation toggles specific FC and NPC switches to establish a safe transfer to the next sector.

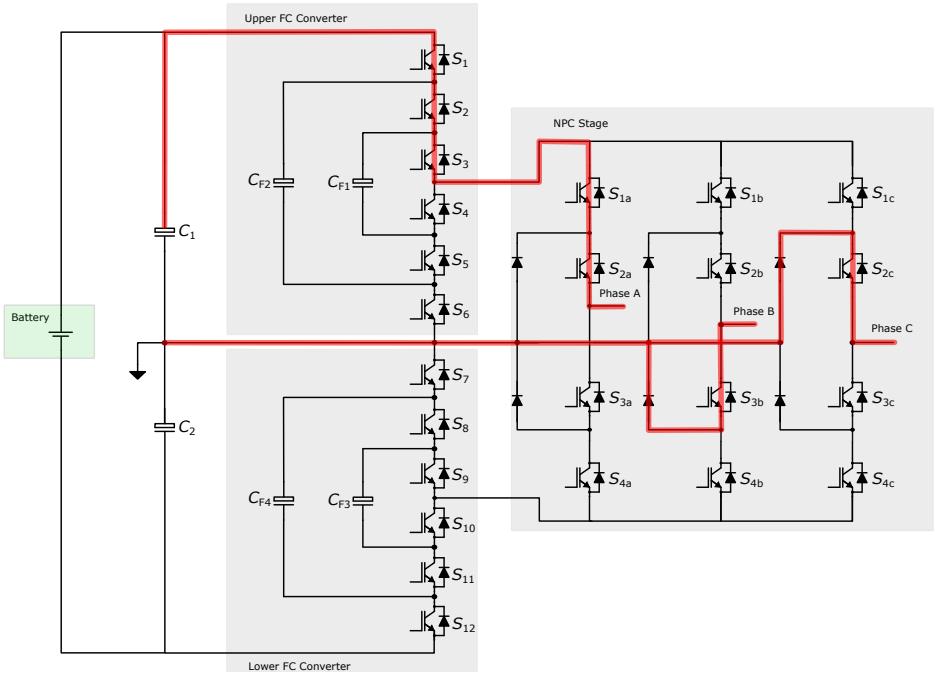

Figure 2.23: Switching operation of $3\phi 3L$ NPC converter during sector 3b.

2.3.1.4 Sector 4 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= +\frac{1}{3}V_{dc} \rightarrow +\frac{1}{6}V_{dc} \\ V_B(sw) &= 0 \rightarrow +\frac{1}{6}V_{dc} \\ V_C(sw) &= -\frac{1}{3}V_{dc} \rightarrow -\frac{1}{6}V_{dc} \end{aligned} \tag{2.6}$$

State 1:

During the state 1 of sector 4 for phase A, the switches S_2, S_3 from upper FC stage and switches S_1, S_{2a} from NPC stage, are turned on which help to appear voltage of $+\frac{1}{3}V_{dc}$ across the phase A. The phase has $0V$ since its connected with neutral point through a clamping diode, which helps the load current to flow from load to the neutral point of the $3\phi 7LM_XM_L$ converter. Phase C has voltage of $-\frac{1}{3}V_{dc}$ when switches S_{10}, S_{11} from lower FC stage and switches S_{3a}, S_{4a} from NPC stage, are turned on. FCs are fully bypassed for the clamped phase, while the two other phases provide their respective positive and negative output voltages. This neutral clamping is essential for minimizing common-mode voltage and enabling waveform symmetry.

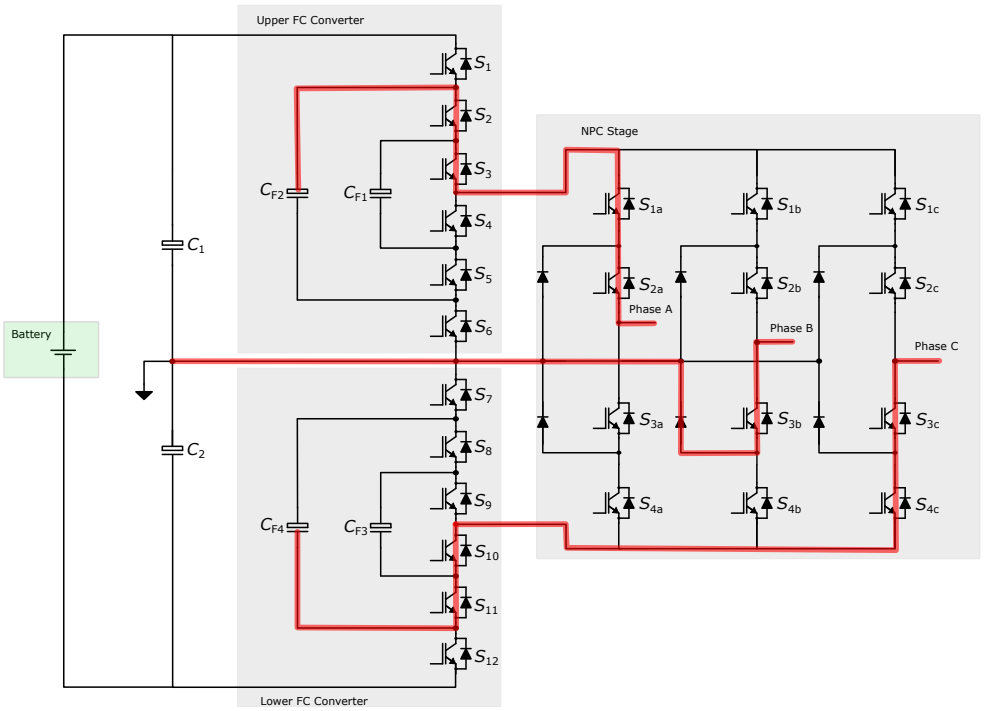

Figure 2.24: Switching operation of $3\phi 3L$ NPC converter during sector 4a.

State 2: In second state of the sector 4 for $3\phi 7LM_XM_L$ converter, phase A receives $\frac{1}{3}V_{dc}$ voltage. For this voltage at phase A, the switches S_2, S_3 from upper FC stage and switches S_{1a}, S_{2a} from NPC stage are turned on. In phase B, there is $0V$ because its connected to the neutral point through a clamping diode and switch S_{3a}. The phase receives $-\frac{1}{3}V_{dc}$ voltage from DC link to lower FC converter stage and finally through NPC stage. The switching operation during this state is: the switches S_{10} and S_{11} from lower FC stage, and switches S_{3c}, S_{4c} from NPC stage as shown in Figure 2.25.

2.3.1.5 Sector 5 of $3\phi 7LM_LM_X$ converter

In Sector 5, the converter produces the following instantaneous switching voltages:

$$\begin{aligned} V_A(sw) &= 0 \rightarrow +\frac{1}{6}V_{dc} \\ V_B(sw) &= +\frac{1}{3}V_{dc} \rightarrow +\frac{1}{6}V_{dc} \\ V_C(sw) &= -\frac{1}{2}V_{dc} \rightarrow -\frac{1}{3}V_{dc} \end{aligned} \tag{2.7}$$

This sector corresponds to a region where both Phases A and B share the positive DC bus, while Phase C operates at a negative potential. The current flow patterns in this sector are described as follows:

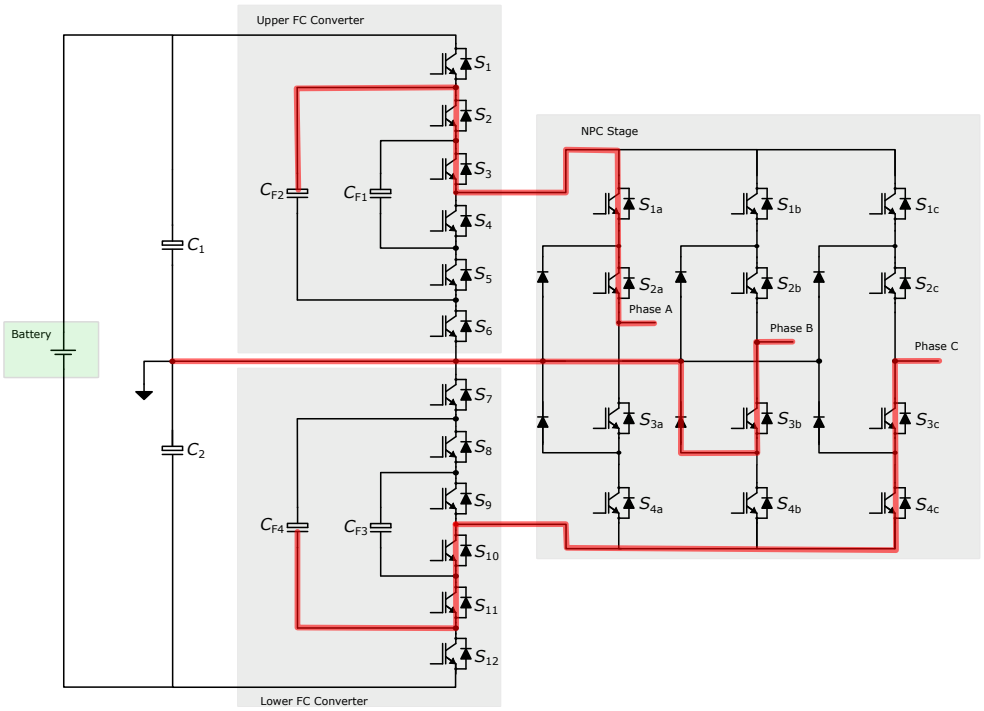

Figure 2.25: Switching operation of $3\phi 3L$ NPC converter during sector 4b.

State 1:

During state 1 of sector 5, Phase A is held at $0V$ by the clamping diode of its NPC leg, while Phase B is active and produces a positive voltage of $+\frac{1}{3}V_{dc}$, its current flows from the positive DC bus through the upper FC converter stage, NPC stage and to the load. Phase A, being clamped, carries its current through the diode toward the neutral point without significant voltage contribution. Phase C, which operates in the negative region at $-\frac{1}{3}V_{dc}$ conducts current from the load back to the converter side, returning it through the lower FC converter stage to the negative DC bus. Hence, during this state, Phase B supplies current from the upper DC bus and upper FC converter stage, Phase C returns current to the lower DC bus through a lower FC stage, and Phase A provides a neutral path through its clamping diode, maintaining the midpoint potential as shown in Figure 2.26.

State 2:

In state 2, As the reference voltage of Phase A is set $+\frac{1}{6}V_{dc}$, its upper NPC switches and upper FC converter begin to conduct. The current of Phase A now flows from the positive DC bus, through its FC converter and NPC leg, and out to the load. At the same time, the reference of Phase B decreases, causing its output to fall toward $+\frac{1}{6}V_{dc}$ from

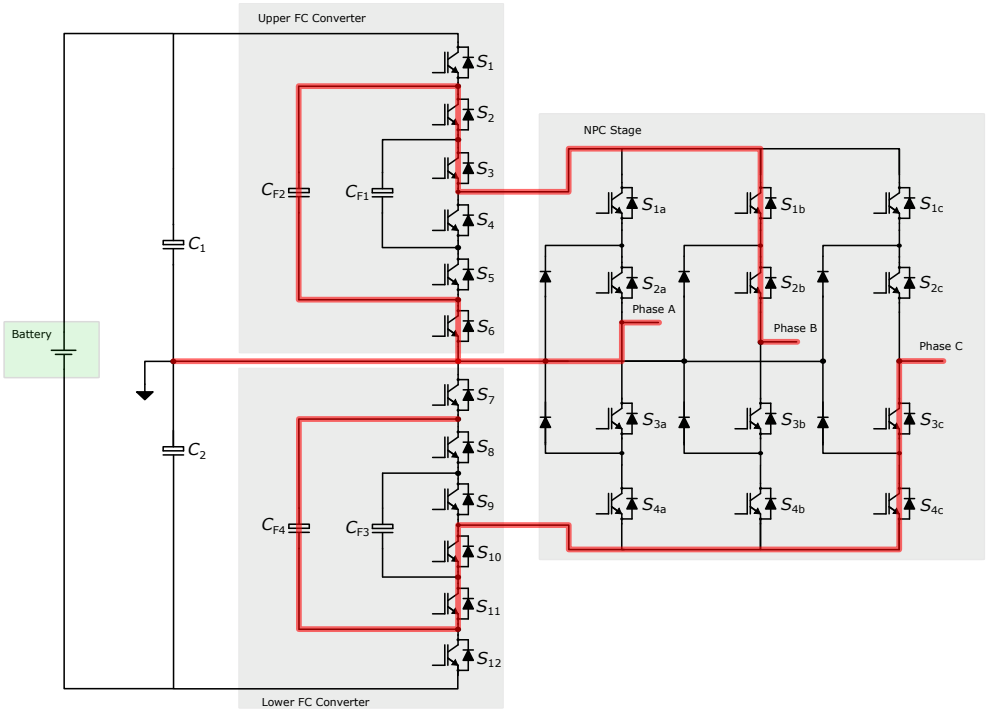

Figure 2.26: Switching operation of $3\phi 3L$ NPC converter during sector 5a.

$+\frac{1}{3}V_{dc}$. Phase C became more negative from $-\frac{1}{3}V_{dc}$ to the $-\frac{1}{2}V_{dc}$. This balanced exchange of current among the three phases stabiles the neutral-point potential and maintains equal voltage sharing across the FCs as illustrated in Figure 2.27.

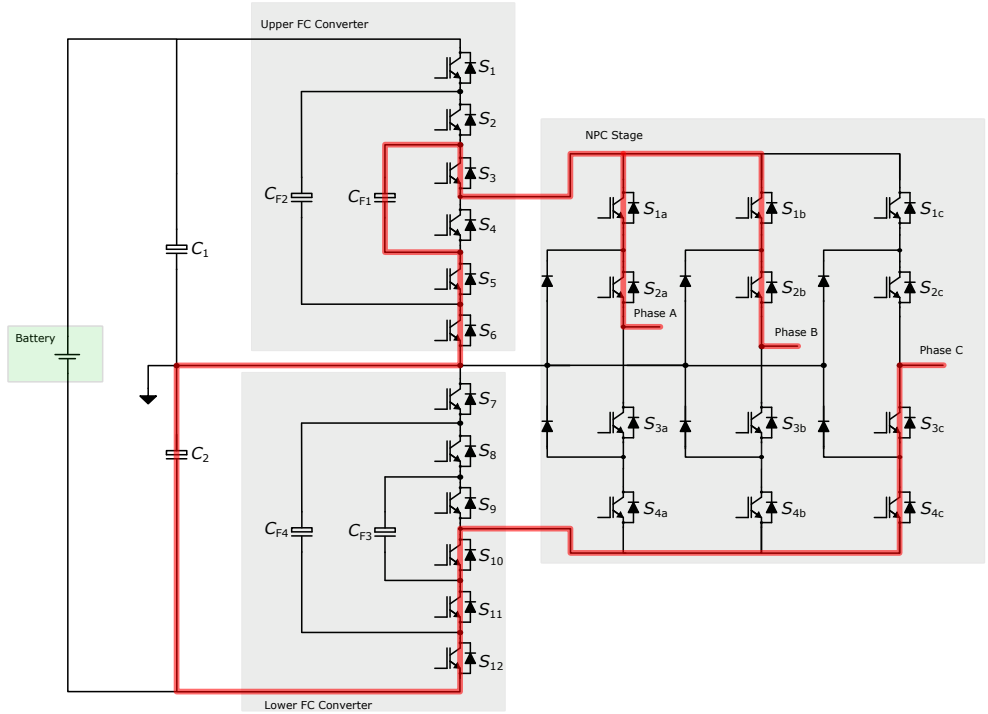

Figure 2.27: Switching operation of $3\phi 3L$ NPC converter during sector 5b.

2.3.1.6 Sector 6 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= 0 \rightarrow -\frac{1}{6}V_{dc} \\ V_B(sw) &= +\frac{1}{2}V_{dc} \rightarrow +\frac{1}{3}V_{dc} \\ V_C(sw) &= -\frac{1}{3}V_{dc} \rightarrow -\frac{1}{6}V_{dc} \end{aligned} \tag{2.8}$$

State 1:

The switching circuit of $3\phi 7LM_XM_L$ converter in second state of the 6th sector is shown in Figure 2.28. The phase A clamped to diode and has zero voltage across the load. The phase B of the converter receives the voltage of $+\frac{1}{2}V_{dc}$ across the load. During this state all upper switches (S_1, S_2, and S_3) of upper FC stage are turned on while S_{1b} and S_{2b} are turned on in the NPC stage of the $3\phi 7LM_XM_L$ converter. In phase C, voltage is $-\frac{1}{3}V_{dc}$, because of the conduction of switches S_{10}, S_{11} in lower FC stage and switches S_{3c}, S_{4c} in the NPC stage.

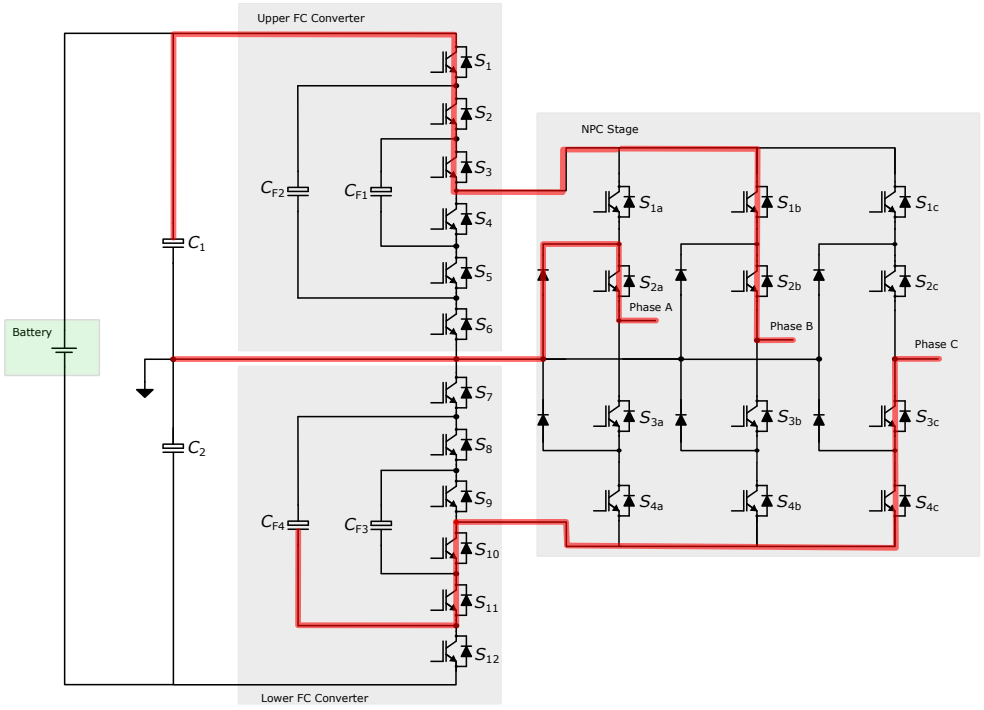

Figure 2.28: Switching operation of $3\phi 3L$ NPC converter during sector 6a.

State 2:

In this state of the sector 6, the phase A make transition from $0V$ to the $-\frac{1}{6}V_{dc}$ by

the conduction of switches S_{10} and S_{3a}, S_{4a} of the lower FC stage and NPC stage of the $3\phi 7LM_LM_X$ converter. The conduction of switches S_2, S_3 and S_{1b}, S_{2b} in upper FC stage and NPC stage make the current flow from C_{F2} to the phase B and appears a voltage of $+\frac{1}{3}V_{dc}$. Similarly for phase C, switches S_{10}, S_{3c} and S_{4c} conducts and voltage across the phase C appears to be $-\frac{1}{6}V_{dc}$.

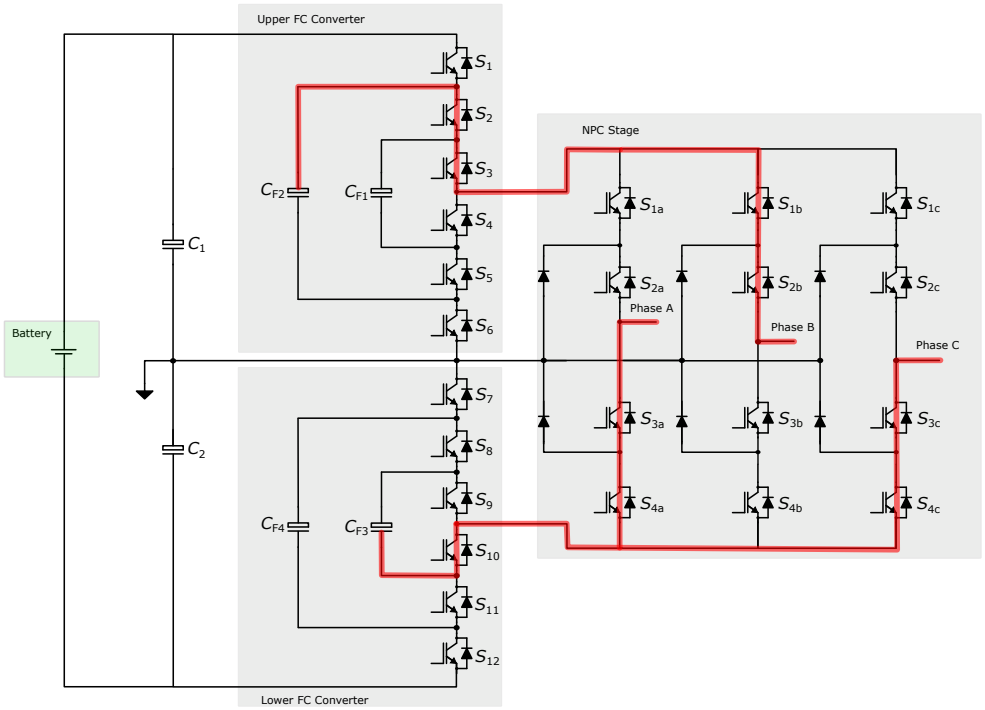

Figure 2.29: Switching operation of $3\phi 3L$ NPC converter during sector 6b.

2.3.1.7 Sector 7 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= -\frac{1}{6}V_{dc} \rightarrow -\frac{1}{3}V_{dc} \\ V_B(sw) &= +\frac{1}{6}V_{dc} \rightarrow +\frac{1}{3}V_{dc} \\ V_C(sw) &= -\frac{1}{6}V_{dc} \rightarrow 0 \end{aligned} \tag{2.9}$$

State 1:

Phase A during the sector 7 in first switching state, has negative voltage of $-\frac{1}{6}V_{dc}$ and turned on switches during this operation are: S_9 of lower FC converter stage and S_{3a}, S_{4a} are turned on. The voltage across the C_{F1} is $+\frac{1}{6}V_{dc}$ which is supplied to the phase B in sector 7. The current follows the path from C_{F1} to the phase B when S_3, S_{1b} and S_{2b} are

turned on. In phase C is the same output voltage as that of the phase A that is $-\frac{1}{6}V_{dc}$ with switches S_{3c}, S_{4c} and S_{10} are in the conduction mode.

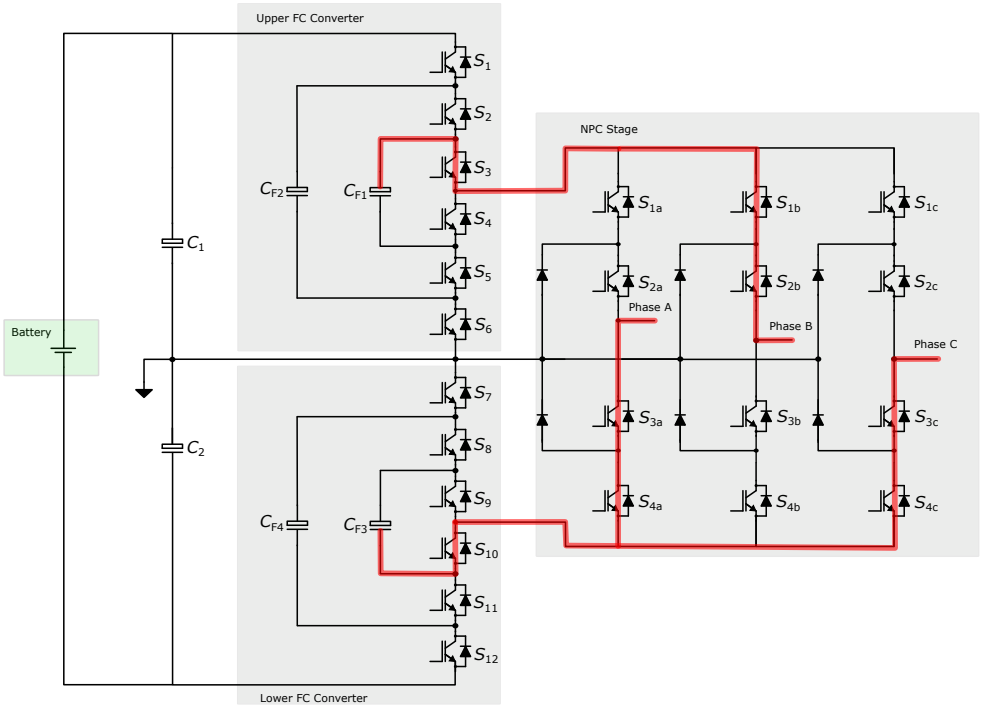

Figure 2.30: Switching operation of $3\phi 7LM_XM_L$ converter during sector 7a.

State 2: In sector 7, during state 2, the voltage at phase A is $-\frac{1}{3}V_{dc}$ because the switches of NPC stage S_{3a}, S_{4a} receives a current from lower Fc converter stage or negative of DC-bus voltage $(-V_{dc}/2)$. The voltage $+\frac{1}{3}V_{dc}$ appears at the phase B, when S_2, S_3 from upper FC converter stage and S_{1b}, S_{2b} from NPC converter stage are turned on. Phase C clamped to the neutral point through a clamping diode and voltage at the phase C is $0V$.

2.3.1.8 Sector 8 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= -\frac{1}{3}V_{dc} \rightarrow -\frac{1}{3}V_{dc} \\ V_B(sw) &= 0 \rightarrow +\frac{1}{6}V_{dc} \\ V_C(sw) &= 0 \rightarrow +\frac{1}{6}V_{dc} \end{aligned} \tag{2.10}$$

State 1:

In sector 8 during the first state, the voltage at phase A is $-\frac{1}{3}V_{dc}$, because switches in that path are turned on like in NPC stage S_{3a}, S_{4a} are conducting, while in lower FC

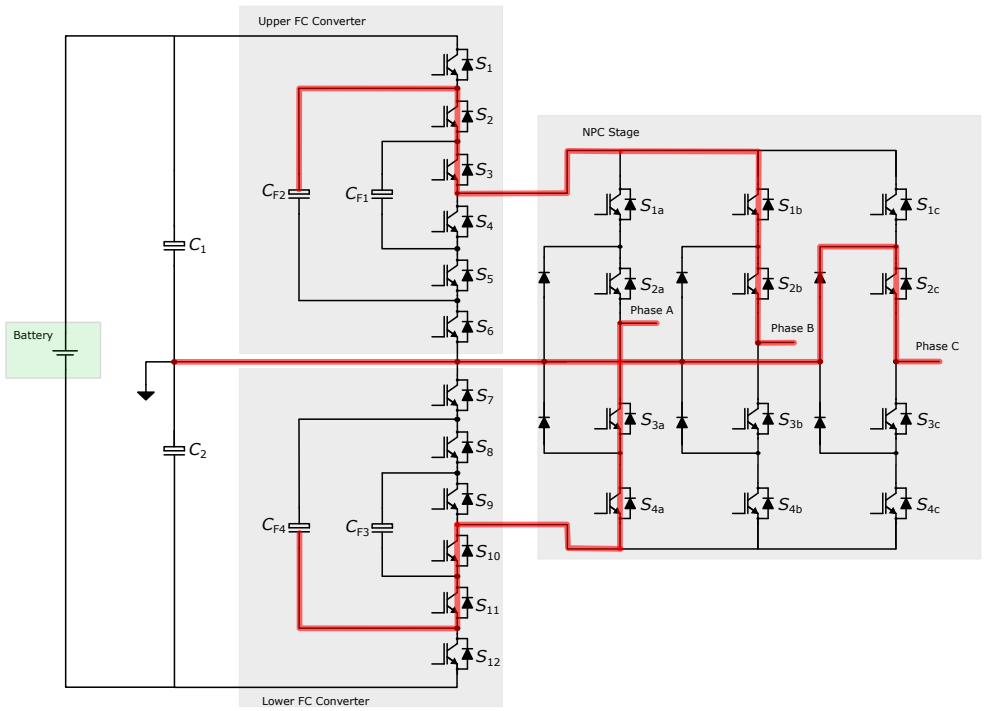

Figure 2.31: Switching operation of $3\phi 3L$ NPC converter during sector 7b.

converter stage switches S_{10}, S_{11} are conducting. The phase B and phase C have the same output voltages of $0V$ that are connected with neutral point of the $3\phi 7LM_LM_X$ converter through a clamping diode.

State 2:

In state 2 of sector 8, the phase A voltage is $-\frac{1}{2}V_{dc}$ which directly connected with DC-link capacitor without connecting with any FCs. The switches operation during this state are: S_{10}, S_{11}, S_{12} of lower FC converter stage and S_{3a}, S_{4a} of the NPC stage of $3\phi 7LM_LM_X$ converter. The phase B and phase C hase the same positive voltage of $+\frac{1}{6}V_{dc}$. The switch S_3 in upper FC converter stage and switches S_{1b}, S_{2b} and switches S_{1c}, S_{2c} of phase B and phase C respectively are turned on to get the voltage of $+\frac{1}{6}V_{dc}$.

2.3.1.9 Sector 9 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= -\frac{1}{6}V_{dc} \rightarrow -\frac{1}{3}V_{dc} \\ V_B(sw) &= -\frac{1}{6}V_{dc} \rightarrow 0 \\ V_C(sw) &= \frac{1}{2}V_{dc} \rightarrow \frac{1}{3}V_{dc} \end{aligned} \tag{2.11}$$

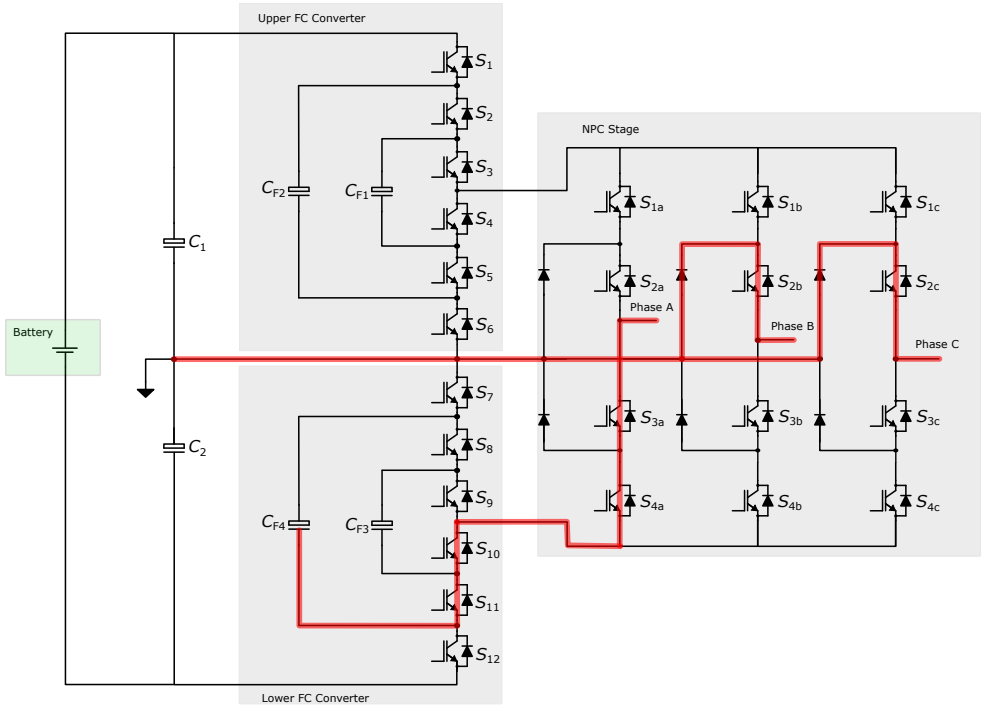

Figure 2.32: Switching operation of $3\phi 3L$ NPC converter during sector 8a.

State 1:

In first state of sector 9, the output voltage at phase A is negative voltage of $-\frac{1}{6}V_{dc}$. The switch S_{10} in lower FC converter stage and switches S_{3a}, S_{4a} in NPC stage are conducting. Phase B has the same voltage as that of phase A but conducting switches in NPC stage are S_{3b} andS_{4b}.

State 2:

The output voltage of phase A, in second state of the sector 9 is $-\frac{1}{3}V_{dc}$. The current flows from the negative DC-link voltage from lower FC converter stage to the NPC stage and finally to the phase A. The switches S_{11}, S_{10}, S_{4a}, and S_{3a} in lower FC converter and NPC stages are conducting. In phase B there is zero voltage because its connected with the neutral point through a clamping diode. Since, phase C has positive voltage of $+\frac{1}{3}V_{dc}$ at output. The conducting switches in NPC stage are: S_{1c} and S_{2c} while in the upper FC converter stage switches S_2 and S_3 are conducting.

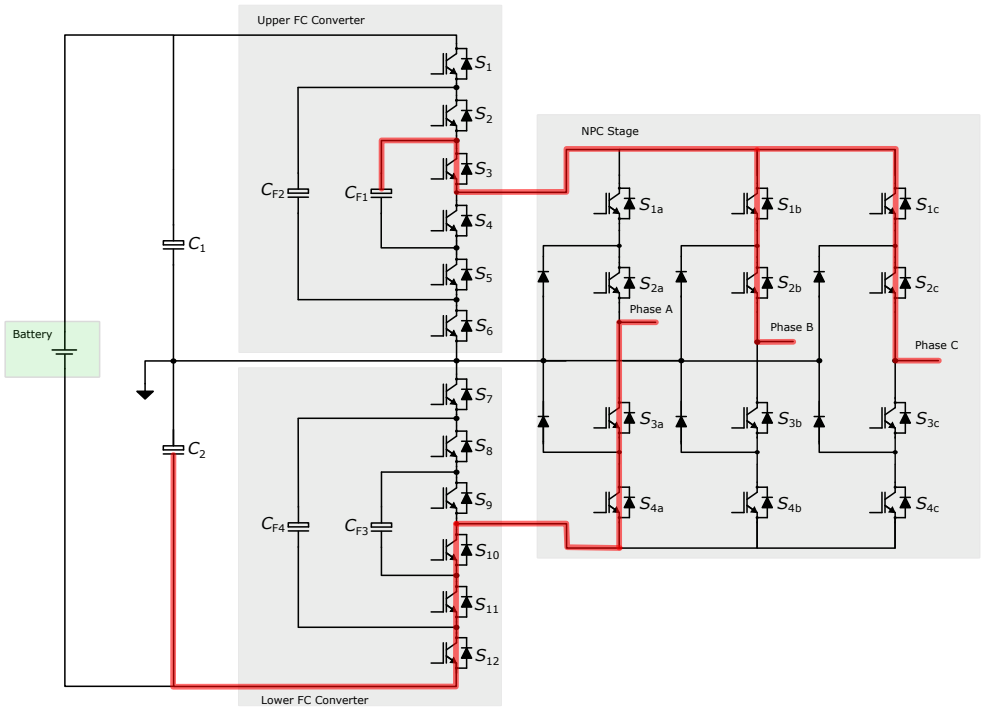

Figure 2.33: Switching operation of $3\phi 3L$ NPC converter during sector 8b.

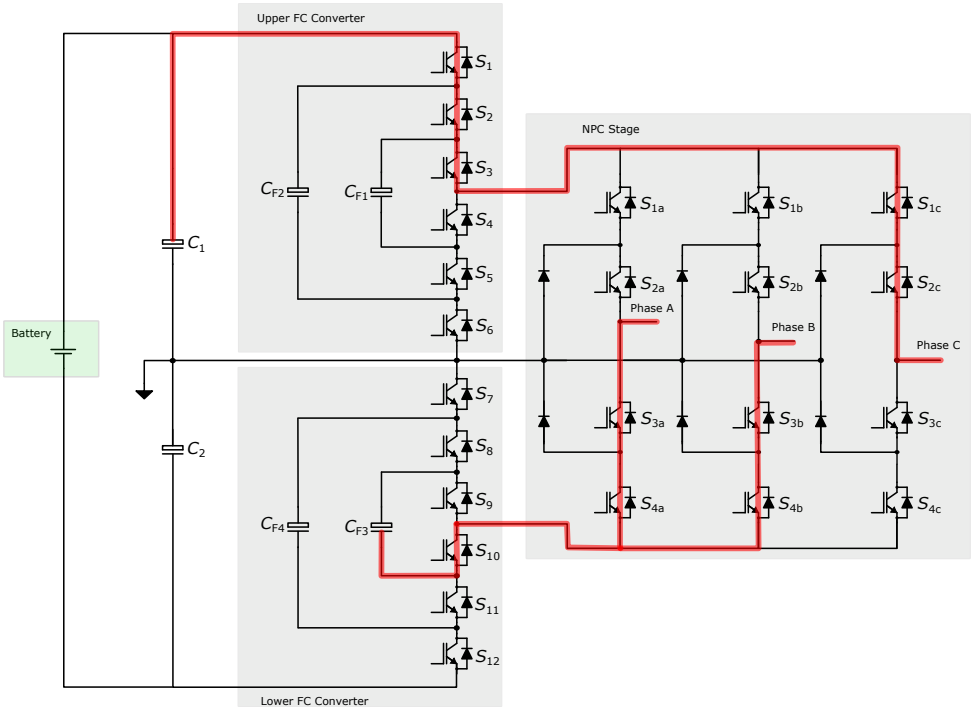

Figure 2.34: Switching operation of $3\phi 3L$ NPC converter during sector 9a.

2.3.1.10 Sector 10 of $3\phi 7LM_LM_X$ converter

The instantaneous switching voltages in this sector are:

$$\begin{aligned} V_A(sw) &= -\frac{1}{6}V_{dc} \rightarrow 0 \\ V_B(sw) &= -\frac{1}{6}V_{dc} \rightarrow -\frac{1}{3}V_{dc} \\ V_C(sw) &= \frac{1}{2}V_{dc} \rightarrow \frac{1}{3}V_{dc} \end{aligned} \tag{2.12}$$

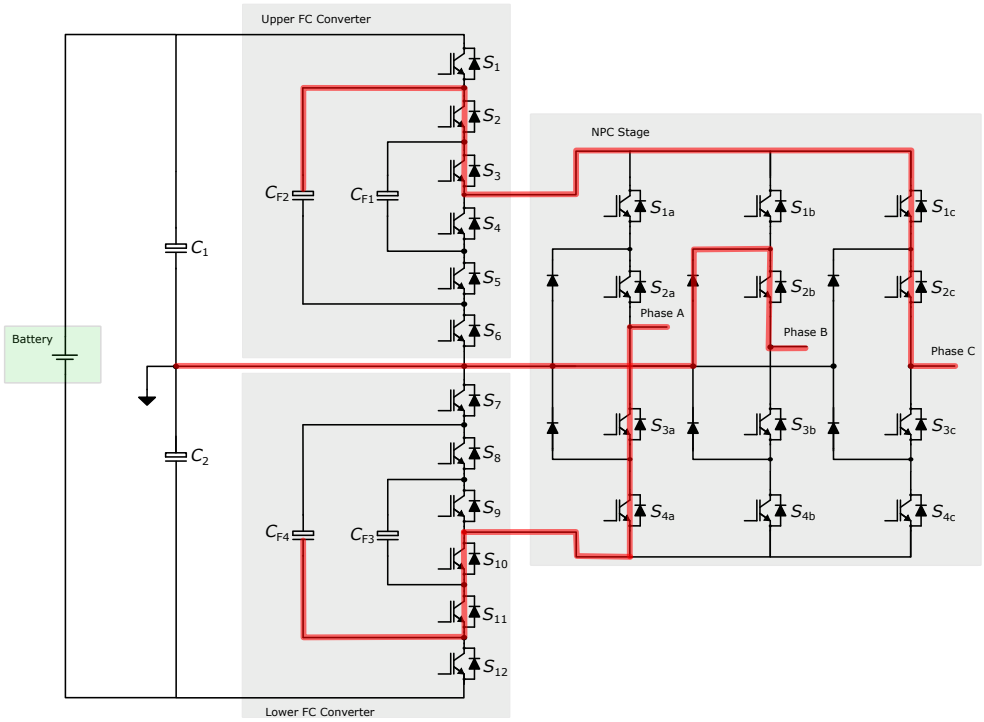

Figure 2.35: Switching operation of $3\phi 3L$ NPC converter during sector 9b.

State 1:

In first state of the sector 10, the phase A has voltage of $-\frac{1}{6}V_{dc}$. The switch S_{10} in the FC converter stage is conducting while in NPC stage are $S3a$ and S_{4a} are conducting. The phase B also have same voltage as of phase A but switches conduction is different in NPC stage that are S_{3b} and S_{4b}. The phase C has output voltage of $+\frac{1}{2}V_{dc}$ with interacting with any FCs.

State 2:

In second state of the sector 10, the phase A voltage is $0V$ because its connected with neutral point through a clamping diode. The phase B has negative voltage of $-\frac{1}{3}V_{dc}$. The switches operation is in this is, switch S_{10}, S_{11} in the lower FC converter stage and switches S_3b, S_{4b} are conducting. In case of phase phase C, the switches S_2, S_3 in upper FC converter stage and S_{1c}, S_{2c} in NPC stage are conducting and produce a positive voltage of $+\frac{1}{3}V_{dc}$.

The voltage make a transition form state 1 to state 2 in each phase, in a sector is shown in Table 2.4.

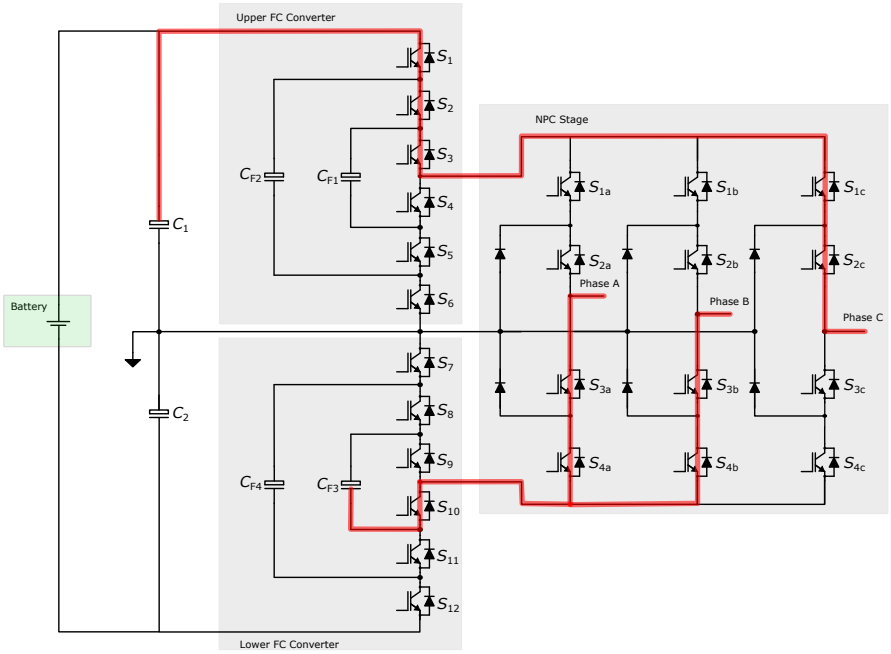

Figure 2.36: Switching operation of $3\phi 3L$ NPC converter during sector 10a.

Table 2.4: Sector states and output voltages in $3\phi 7LM_LM_X$ converter

Sector	State 1: Output Voltage	State 2: Output Voltage
1	$V_a = 0, V_b = -\frac{1}{3}V_{dc}, V_c = +\frac{1}{3}V_{dc}$	$V_a = 0, V_b = -\frac{1}{3}V_{dc}, V_c = +\frac{1}{3}V_{dc}$
2	$V_a = +\frac{1}{6}V_{dc}, V_b = -\frac{1}{6}V_{dc}, V_c = +\frac{1}{6}V_{dc}$	$V_a = +\frac{1}{3}V_{dc}, V_b = -\frac{1}{3}V_{dc}, V_c = 0$
3	$V_a = +\frac{1}{3}V_{dc}, V_b = -\frac{1}{6}V_{dc}, V_c = -\frac{1}{6}V_{dc}$	$V_a = +\frac{1}{2}V_{dc}, V_b = 0, V_c = 0$
4	$V_a = +\frac{1}{3}V_{dc}, V_b = 0, V_c = -\frac{1}{3}V_{dc}$	$V_a = +\frac{1}{3}V_{dc}, V_b = 0, V_c = -\frac{1}{3}V_{dc}$
5	$V_a = 0, V_b = +\frac{1}{3}V_{dc}, V_c = -\frac{1}{6}V_{dc}$	$V_a = +\frac{1}{6}V_{dc}, V_b = +\frac{1}{6}V_{dc}, V_c = -\frac{1}{2}V_{dc}$
6	$V_a = 0, V_b = +\frac{1}{2}V_{dc}, V_c = -\frac{1}{3}V_{dc}$	$V_a = 0, V_b = +\frac{1}{2}V_{dc}, V_c = -\frac{1}{3}V_{dc}$
7	$V_a = -\frac{1}{6}V_{dc}, V_b = +\frac{1}{6}V_{dc}, V_c = -\frac{1}{6}V_{dc}$	$V_a = -\frac{1}{3}V_{dc}, V_b = +\frac{1}{3}V_{dc}, V_c = 0$
8	$V_a = -\frac{1}{3}V_{dc}, V_b = 0, V_c = 0$	$V_a = -\frac{1}{2}V_{dc}, V_b = -\frac{1}{6}V_{dc}, V_c = -\frac{1}{6}V_{dc}$
9	$V_a = -\frac{1}{6}V_{dc}, V_b = -\frac{1}{6}V_{dc}, V_c = +\frac{1}{2}V_{dc}$	$V_a = -\frac{1}{3}V_{dc}, V_b = 0, V_c = +\frac{1}{3}V_{dc}$
10	$V_a = -\frac{1}{6}V_{dc}, V_b = -\frac{1}{6}V_{dc}, V_c = +\frac{1}{2}V_{dc}$	$V_a = 0, V_b = -\frac{1}{3}V_{dc}, V_c = +\frac{1}{3}V_{dc}$

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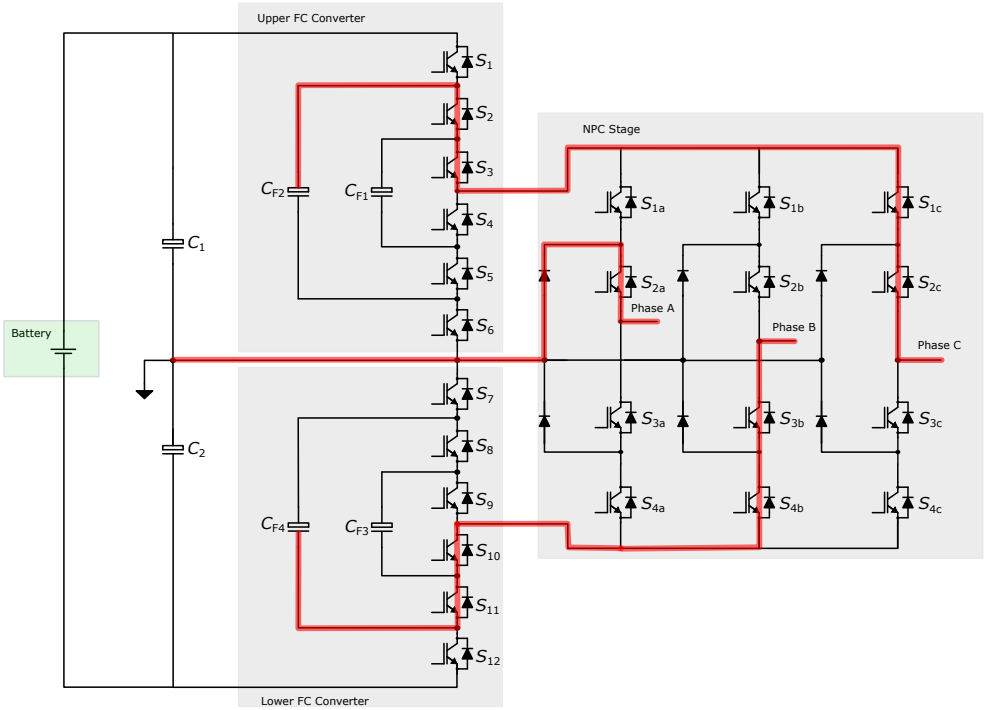

Figure 2.37: Switching operation of $3\phi 3L$ NPC converter during sector 10b.

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Chapter 3:

Balancing of Flying Capacitors for Multiplexed Multilevel Converter

FC multilevel converters are widely employed in medium- and high-power applications due to their ability to produce high-quality output voltages with significantly reduced harmonic distortion and lower dv/dt stress. By generating a large number of voltage levels, these converters minimize THD, reduce filtering requirements, and lower switching stress on semiconductor devices, thereby decreasing both switching losses and electromagnetic interference (EMI). The reduced per-switch blocking voltage also enables the use of faster, lower-loss devices with improved conduction characteristics. These advantages collectively result in enhanced efficiency, improved power quality, and greater reliability, making FC multilevel converters a preferred choice for applications such as renewable energy systems, medium-voltage drives, and grid-connected power conversion.

A defining feature of FC multilevel converters is the incorporation of multiple FCs connected across the switching devices within each phase leg. These capacitors must be precisely regulated at their respective nominal voltage levels (typically fractional multiples of the total DC-link voltage) to ensure correct synthesis of the desired multilevel output waveform and balanced voltage distribution among the power semiconductors. Accurate voltage balance across the FCs is therefore essential for reliable and distortion-free operation of the multilevel converters. However, during dynamic operation, these FCs naturally experience unequal charging and discharging, leading to voltage drift. If the capacitor voltages deviate from their ideal values, the converter may produce distorted output waveforms, suffer increased switching losses, and experience potential overstress or failure. Therefore, ensuring accurate and stable capacitor voltage balancing is essential for reliable converter performance. In literature there are many types of FCs voltage balancing algorithms are discussed but few of main algorithms are discussed here.

3.1 Types of capacitor voltage balancing algorithms

3.1.1 Redundant Switching State Selection Methods

A redundant switching method is fundamental method for balancing voltage across the FCs[1]. In which there are several switching sequence are provided to MLCs to acquire a specific voltage level. The main concept is that there are several switching sequences for the converter to perform switching for a voltage level but each sequence has their own impact on the charging and discharging of the FCs of the MLCs. A controller is used which continuously observing the switching sequence of the MLCs and select a more optimal one, which effectively drives the voltage across the capacitors near the reference voltage. This can be achieved by choosing the switching sequence that helps achieve the required voltage level across the FCs that may do charging or discharging depending on its voltage deviations. The voltage should have minimum deviation after accessing the size and sign of deviation in voltage and compare it with the particular reference voltage for each FC. However, at higher modulation indices ($m = 0.98$) or unity power factor ($pf = 1$), when the available redundancy is less often used, [2] showed that traditional redundant state selection might become ineffective. In order to cope with this issue, sophisticated algorithms like Redundant Level Modulation (RLM) add more output voltage levels throughout a switching cycle, giving the FC voltages more flexibility without changing the basic output waveform [3].

3.1.2 PWM-Based Balancing Algorithms

This method of stabilizing the voltage across the FCs utilizes an inherent property of PWM schemes as a PD-PWM scheme, and PS-PWM scheme in order to achieve a naturally balancing of voltage. The idea behind this is that, average current flowing through the FCs in normal conditions is equal to zero, then modulation scheme will ensure that the FC is charged or discharged equally in a complete switching period [4]. However, the natural balancing method is particularly effective in symmetrical topologies of the multilevel converters and balanced condition of loads. The effectiveness of the natural balancing of the FCs can be destroyed under the influence of unbalanced loads of during the transient period in the MLC. To cope with these issues, the active feedback or offset injection into

the schemes can enhance the balancing of voltage across the FCs. These enhancements allow the modulation index or carrier phase to be dynamically adjusted, providing a robust and adaptive balancing mechanism [5].

3.1.3 Predictive Control Algorithms

Model predictive control algorithms represent a model-based approach to FCs voltage balancing. Using the mathematical model of the MLCs and load, the model predictive control algorithms predicts the future evolution of voltage across the FCs. Within each switching period, the predictive control algorithm check all possible switching sequence of the multilevel converters and select the particular switching sequence of the converter which gives lower value of the cost function or difference of the reference value and actual value of voltages across the FCs. The cost function consists of two controlled variables one is voltage across the FCs and other is the current across the FCs and both controlled variables are weighted through a weighting factor. This method of controlling voltage across the FCs has fast dynamic response and precise voltage regulation, as the controller can anticipate and counteract disturbances before they manifest. The block diagram for model predictive control for balancing the voltage across the FC is shown in Figure 3.1. The measurement blocks take model data like FCs voltages and FC currents,

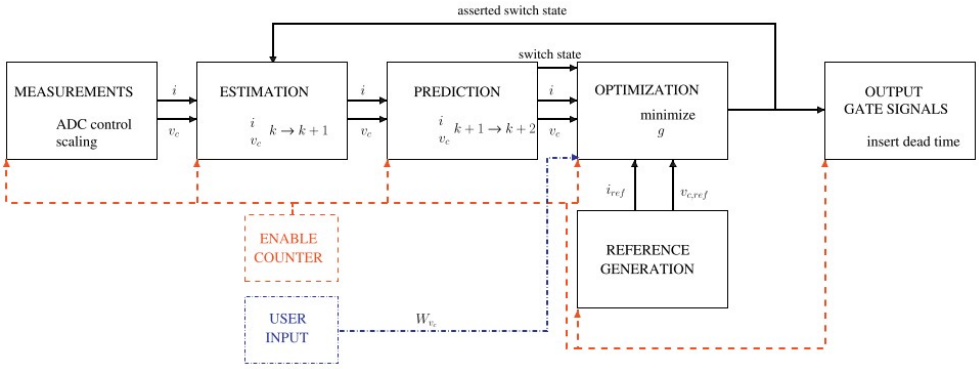

Figure 3.1: MPC control for FC voltage balance for FC converter [6].

then estimates that data for removing any error, the prediction step predict the controlled variable and obtained new predicted value based Euler backward or forward methods. The cost function is minimized, which means set the minimum difference between the actual and reference values of the FC's voltages. In [6] the model is demonstrated for predictive control can simultaneously optimize the voltage across the FCs and quality

of output voltage waveforms, though it needs a exact model of the MLC or load and significant computational time to solve the optimization problem in real-time.

3.1.4 Hysteresis Based Algorithms

The Hysteresis-based controller operate in such a way that, upper and lower voltage thresholds around reference voltage of each flying capacitor as per the levels of FC converter. In case when the voltage across the FC is changed from the reference value of the voltage, then hysteresis controller switches the switching sequences of the multilevel converter to induce a current that brings the voltage across the FCs close to reference value of the FC voltage. The block diagram of hysteresis control is shown in Figure.

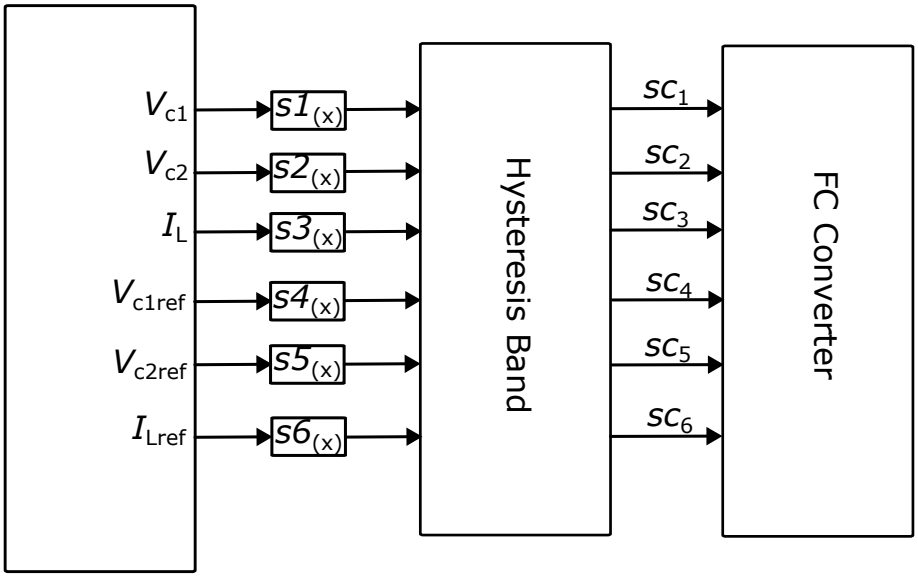

Figure 3.2: Hysteresis control based FC voltage control of FC converter [7].

In Figure 3.4, V_{c1}, V_{c2} are the voltages across the FC1 and FC2. I_L is load current while V_{c1ref} and V_{c2ref} are the reference/required voltages of FCs. The hysteresis control generated the control signals for modulator which generate PWM signals for FC converters. This bang-bang control strategy is theoretically simple and does not require complex modulation or state estimation. The hysteresis based control is illustrated in below Figure.

The diagram of hysteresis based control is presented in Figure 3.3. It consists of four main blocks, (i) redundant state selection (RSS) table, (ii) phase-locked loop (PLL), (iii) output voltage compensator and (iV) a base level calculation. The PLL determines the

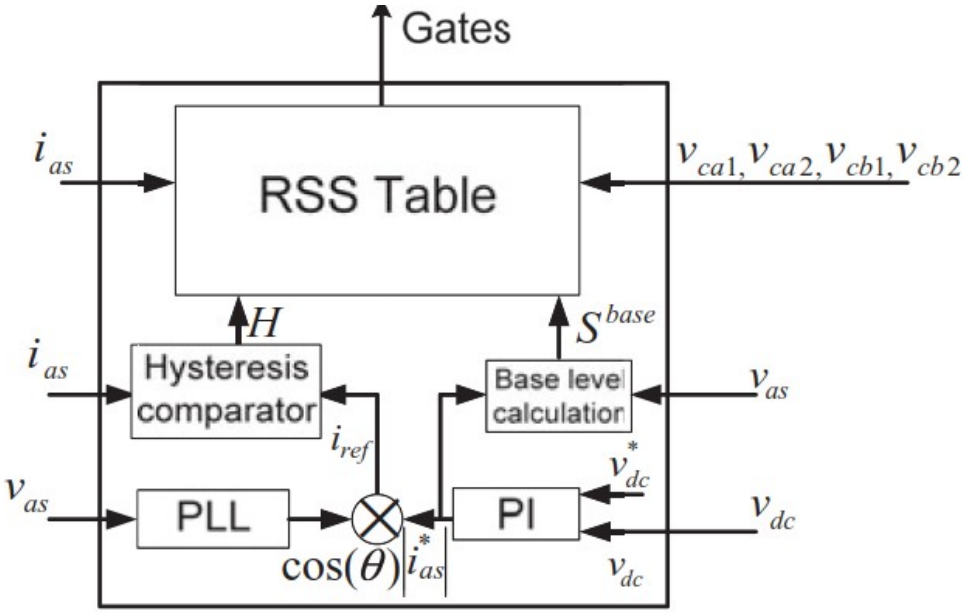

Figure 3.3: Hysteresis based FC voltage control of $1\phi 4L$ FC converter [8].

phase angle of the input voltage, output of voltage compensator is the magnitude of reference current. V_{ca1}, V_{ca2}, V_{cb1}, and V_{cb2} are the voltages across the FCs of the converter. V_{as}, and I_{as} are the phase voltage and phase current of the converter. However, as shown by [8] the switching frequency becomes variable and depends on the rate at which capacitor voltages cross their thresholds, which can lead to increased switching losses and EMI if not properly managed. Recent work by [9] has further refined hysteresis control to improve its performance in wide output voltage applications.

3.1.5 Feedback Loop-Based Algorithms

The feedback loop based controllers like proportional integral (PI) controller employ the continuous feedback loop to regulate the voltage across the FCs of the converter. The PI controller in feedback with the multilevel converter takes the measured output voltages of FCs and compare it with the required output voltage. The PI controller generates the control signal based on input error signals. The control signal can adjust the switching action of the converter. In classical control theory, the control law is designed to minimize the error signal so that measured voltage should as close as possible to the reference voltage in order to ensure the robust and stable operation of the converter during the load transient and parameters mismatch. A feedback loop-based PI controller is proposed in [10] to regulate the voltage across FCs of-level FC converter.

The block diagram of the controller is shown in Figure 3.4.

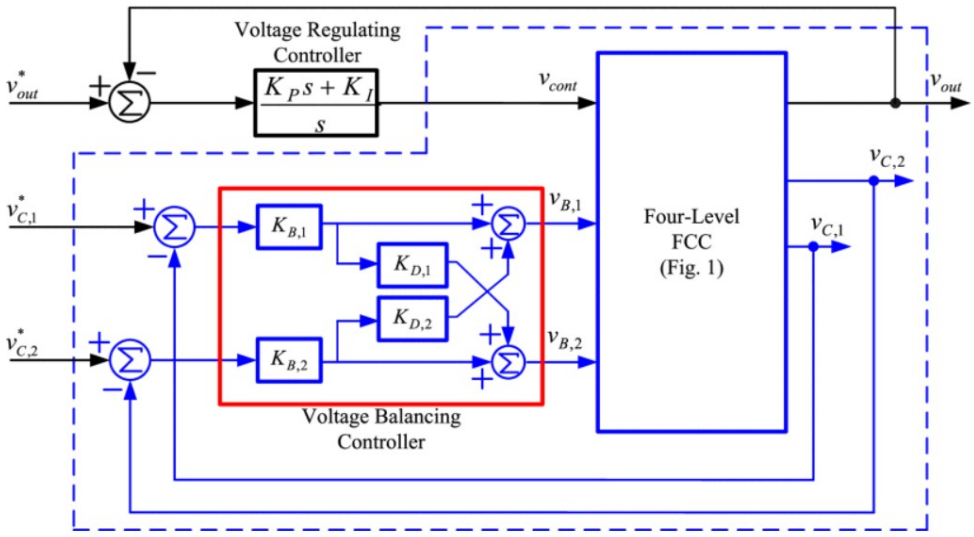

Figure 3.4: PI based FC voltage control of $1\phi 4L$ FC converter [9].

There are three controllers used in this approach, one PI controller to regulate the output voltage of the converter, the remaining two P-controller used to control the voltage across the FCs. Its challenging to control FC converter because of the coupling effect of the three control loops. Some simple design steps proposed to design the controller, first step is to decoupled voltage balancing control are designed then design the voltage regulating controller for output voltages.

3.1.6 Sliding Mode Control

The sliding mode controller (SMC), has been widely implemented in the field of power electronics converters. It offers the key benefits of: robust to system uncertainties and disturbances, fast dynamic response of voltage balancing across the FCs, and easy to implement. In SMC, the controller defines a sliding surface based on the FCs voltage errors and applies discontinuous control to force the trajectory of system to remain on this surface, ensuring convergence of the FCs voltages to the reference FCs voltages even under any disturbance or model error. However, SMC has some drawbacks including chartering effect, and need of high gains. The high gain is effective in fast convergence and handling of uncertainties in the system but leads to significant issues in practical applications [11].

Method	Idea	Complexity	Pros	Cons
Redundant states	Chooses among possible switch states each cycle to minimize capacitor voltage error using a cost function.	Medium	Fast, robust balancing; effective at all loads.	Requires voltage measurement and control logic.
PWM natural balancing	Uses phase/level-shifted PWM so the average charge on each capacitor is zero, relying on symmetry.	Low	Very simple and requires no extra sensors.	Slow to correct imbalanced voltage and weak during asymmetrical loads.
Predictive control	Predicts the FC's each voltage levels for all switching actions and chooses the best predicted values.	High	fast dynamic response and precise; supports multi-objective control.	Requires a model of multilevel converter and load; it also takes significant computation time.
Hysteresis control	Switches only when a capacitor voltage leaves a defined window and restores it inside the band.	Low	Simple and robust control; it is also responsive to errors.	Variable switching frequency; increased ripple.
PI / feedback	Uses capacitor voltage error to adjust the PWM.	Medium	Possess a good accuracy and minimizes the steady-state error.	Requires tuning and has slow dynamic response.
Sliding mode control	Uses the nonlinear laws for robust, rapid convergence of error under any perturbations.	High	Highly robust and fast response.	Complex to design and implement.

Table 3.1: Comparison of flying capacitor voltage balancing methods

3.2 Cost function-based voltage balancing algorithm

In this thesis, cost function based balancing of FC is used to balance the FC converter stage of $3\phi 7LM_XM_L$ converter. The $3\phi 7LM_XM_L$ converter has two stages of $1\phi 4L$ FC

converter. The upper FC converter stage and lower FC converter stage. Each FC of upper and lower FC converter will be balanced by cost-function based voltage balancing algorithm. Before implementing a control algorithm for $3\phi 7LM_XM_L$ converter, first to understand the operation of $1\phi 4L$ FC converter.

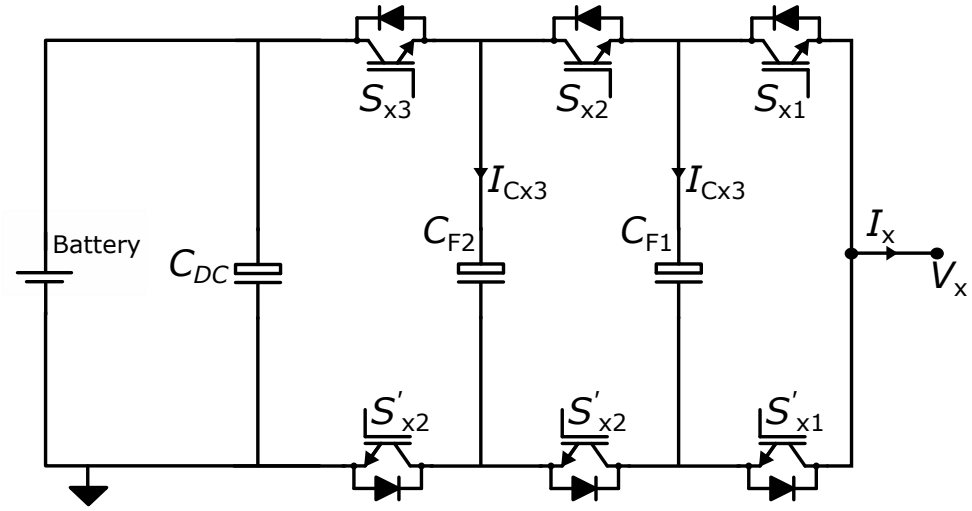

Figure 3.5: Topology of $1\phi 4L$ FC converter.

The schematic of one phase leg of $4L$FC converter is shown in Figure 3.5. The subscript X indicates the phase of the $3\phi 4L$ FC converter that is $X = a, b, c$. During the operation of the FC converter, the mean value of voltage across each FC of both upper and lower FC converter stage are: $V_{dc}/6$, and $V_{dc}/3$. where V_{dc} is the DC-bus voltage. The voltage across each switch in both stages of FC converter is $V_{dc}/6$. By applying Kirchhoff's voltage law and current law, the line to ground voltage and current [12] through the FCs can be written as:

$$\begin{aligned} v_{x0} =& s_4 V_{\text{dc}} + (s_3 - s_4)\, v_{C3} + (s_2 - s_3)\, v_{C2} + (s_1 - s_2)\, v_{C1} \\ i_{C1} =& (s_2 - s_1)\, i_1 \\ i_{C2} =& (s_3 - s_2)\, i_2 \\ i_{C3} =& (s_4 - s_3)\, i_3. \end{aligned} \tag{3.1}$$

Where S_z is the switch control function, where z is the particular switch of FC converter in a leg $z = \{1, 2\}$. The value of switch control function can be either 0 or 1 which means either switch is on or off. The 6 switches of $4L$ FC converter operates in complementary way according the operation. In the case of a $3L$ FC converter, voltage across the FCs

of the converter are relatively straightforward and manageable to regulate as per the desired voltage levels during each switching period. This is because the two available redundant switching states can be easily alternated effectively to maintain the voltage levels of the FCs separately. However, as the topology level up to high output voltage levels for FC converter with more levels (n > 3), the complexity of the control algorithm increases voltage balancing increases significantly. In these cases, a similar approach to voltage balancing can be applied, but it becomes much more intricate due to the need to regulate additional FCs voltage levels. Furthermore, the increased number of available switching states introduces more variables and scenarios that must be carefully managed to ensure proper operation and voltage stability of the FCs. The higher number of levels necessitates advanced control strategies to handle the additional degrees of freedom and maintain consistent voltage levels across all FCs, which is crucial for reliable performance of the FC converter. Each redundant condition in the charging and discharging of FCs voltages produces dynamically changing impacts, which is the primary cause of voltage imbalance across FCs. This imbalance can adversely affect the overall performance, stability, and efficiency of the $1\phi 4L$ FC converter, making it a critical issue to address in the design and operation of such topologies of power electronic converters. For the proper balancing of the FCs, the redundant switching states should be carefully selected to ensure proper balancing of the voltage across the FCs. This selection process often involves the implementation of advanced control algorithms that uses a cost function to prioritize the balancing the of FC voltage. The cost function evaluates the impact of each possible switching state and determines the optimal sequence to maintain consistent voltage levels across the FCs. By minimizing the deviation from the desired voltage levels, the control strategy ensures that the converter operates reliably and efficiently. Moreover, the use of such optimization techniques can help mitigate the impact of external disturbances, load variations, and other dynamic factors that could otherwise exacerbate the voltage across the FCs. This approach is especially vital in multilevel converters with a higher number of voltage levels, where the complexity of managing the redundant switching states increases significantly [13]. An equation for minimization of the cost function to balance the FCs is

$$J_{xz} = \frac{1}{2}\sum_{j=1}^{n-2} C_{xj}\left(V_{Cxj} - V_{Cxj}^{*}\right)^{2} \tag{3.2}$$

Where x identifies the FC converter (i.e., x = u for upper FC converter of the $3\phi 7LM_LM_X$ converter and x = l for lower FC converter of the $3\phi 7LM_LM_X$ converter) and z represents the switching state, with z = 1, ..., 8. The index (j) is used to identify each FC. In this paper j = 1, 2. The V_{cxj}^{*} is the reference voltage, and V_{cxj} is a specific FC of the upper and lower FC converters stages of $3\phi 7LM_LM_X$ converter. When the voltages across all the FCs are equal to their reference/desired values, the cost function shown in Equation (1) will be equal to zero. To achieve a proper desired voltage across each FC, it must be reduced during each switching time. The differential Equations (3.3) and (3.4) derived equation (3.2) show the minimized differential equations:

$$\frac{d}{dt}J_{xz} = \frac{d}{dt}\frac{1}{2}\sum_{j=1}^{n-2} C_{xj}\left(V_{Cxj} - V_{Cxj}^{*}\right)^{2} \tag{3.3}$$

$$\frac{d}{dt}J_{xz} = \sum_{j=1}^{n-2}\left(\Delta v_{Cxj} i_{Cxj}\right) \leq 0 \tag{3.4}$$

where Δv_{Cxj} is the deviation of any specific FC voltage from the referenced voltage value of any FC. Since $\Delta v_{Cxj} = V_{Cxj} - V_{Cxj}^{*}$, the current in each FC can be represented as i_{Cxj}, which depends on the selected redundant switching states of the converter and the output FC current of the upper FC converter and lower FC converter, as shown in Table 2.

Table 2 illustrates the redundant switching states for voltage levels $\pm 1/2\mathrm{V}_{dc}$, $\pm 1/3\mathrm{V}_{dc}$, and $\pm 1/6\mathrm{V}_{dc}$ that produce distinct current routes across any FCs of upper and lower FC converters stages and, therefore, have a unique impact of charging and discharging on the FCs of upper and lower FC converters. A phase leg of four-level upper and lower FC converters that incorporate FCs are schematically shown in Figure 2. The mean voltage values of FCs C_{x1} and C_{x2} for upper FC converter should be kept at V_{dc}/6 and V_{dc}/3 respectively, during regular operation. The upper FC converter has four output voltage levels, but the zero voltage level will be omitted by always closing the switch S_3, and the output voltage will be produced: V_{dc}/6, V_{dc}/3, and V_{dc}/2. The same is true for the lower FC at voltage levels of -V_{dc}/6, -V_{dc}/3, and -V_{dc}/2. The switching state that minimizes the

Table 3.2: Four-level upper and lower FCC: voltage levels, switching states, FC currents, and effects on FC voltages.

Voltage Leve		Switch States			FC Current		FC Voltage	
	z	S_1	S_2	S_3	I_{CF1}	I_{CF2}	V_{CF1}	V_{CF2}
$+\frac{V_{dc}}{2}$	8	1	1	1	0	0	X	X
$+\frac{V_{dc}}{3}$	7	1	1	0	0	i_x	X	↑
	6	1	0	1	i_x	$-i_x$	↑	↓
	5	0	1	1	$-i_x$	0	↓	X
$+\frac{V_{dc}}{6}$	4	1	0	0	i_x	0	↓	X
	3	0	1	0	$-i_x$	i_x	↑	↑
	2	0	0	1	0	$-i_x$	X	↓
0	1	0	0	0	0	0	X	X
Voltage Level	z	S_7	S_8	S_9	I_{CF3}	I_{CF4}	V_{CF3}	V_{CF4}
$-\frac{V_{dc}}{2}$	8	1	1	1	0	0	X	X
$-\frac{V_{dc}}{3}$	7	1	1	0	0	i_x	X	↑
	6	1	0	1	i_x	$-i_x$	↑	↓
	5	0	1	1	$-i_x$	0	↓	X
$-\frac{V_{dc}}{6}$	4	1	0	0	i_x	0	↓	X
	3	0	1	0	$-i_x$	i_x	↑	↑
	2	0	0	1	0	$-i_x$	X	↓
0	1	0	0	0	0	0	X	X

Note: The charging and discharging effects in FC are given: assuming that i_x is positive with the following notations:
↑ Increasing capacitor voltage.
↓ Decreasing capacitor voltage.
X No change in capacitor voltage.

cost function is chosen for every voltage level and each switching period. For example, J_{u6} is the estimated cost function of the 6^{th} switching state for upper FC converter, i.e., S_1=1, S_2=0, and S_3=1 (or 1 0 1). The overall structure of the FCs balancing using the cost function minimization technique is shown in Figure 3.6. For a specific reference voltage level, more redundant states may be possible. For each redundant state, the cost function is calculated. Then, the redundant state corresponding to the minimum cost function is applied.

The Figure 3.6 consists of five blocks which constitute a complete FC voltage balancing algorithm.

3.2.1 Reference voltage generation

In Figure 3.6, the left top block is the three-levels reference voltage. A reference sinusoidal signal is compared with the 6 triangular carriers to generate the reference

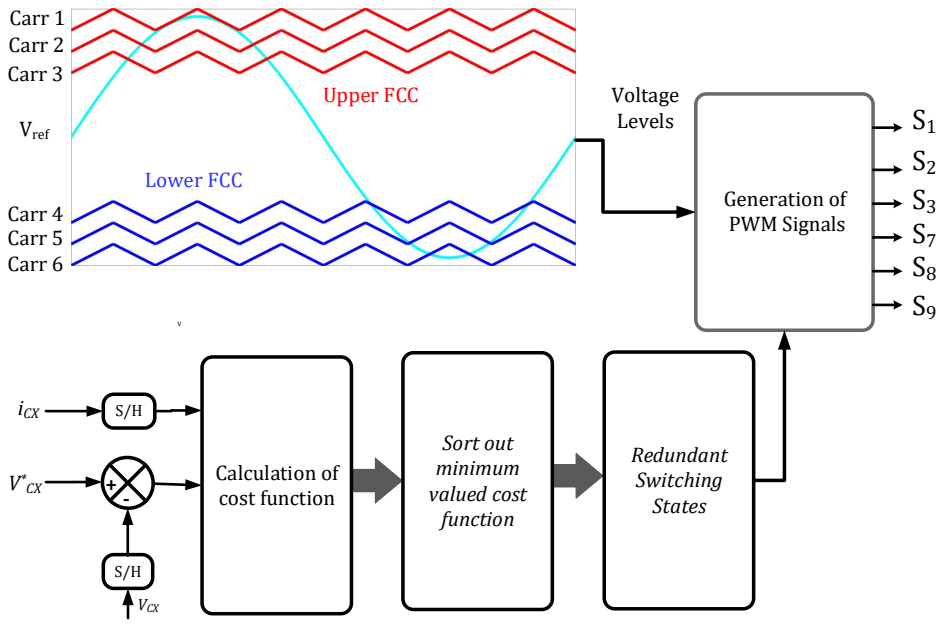

Figure 3.6: Voltage balancing algorithm for $3\phi 7LM_LM_X$ converter.

levels of voltage for both upper and lower FC converter stages of $3\phi 7LM_LM_X$ converter. Based on these reference voltage levels, particular switching sequences are applied to both upper and lower FC converter stages to perform voltage balancing across the FCs of the FC converter stages. The waveform in red color is the reference triangular waveform used to generate reference voltage levels for upper FC converter stage which generate positive half cycle of the $3\phi 7LM_LM_X$ converter. The triangular waveform in blue color is the reference triangular waveform for lower FC converter stage and used to generate a negative half cycle of the $3\phi 7LM_LM_X$ converter. The final generated reference voltage for the FC converter stages of the $3\phi 7LM_LM_X$ converter are shown in Figure 3.7.

3.2.2 Calculation of cost function

In the part, the error signal generated from reference voltage of FCs and actual voltage of FCs which feed to the cost function block to minimize the error between actual value of voltage between the FC and reference voltage. In case of upper FC converter and lower FC converter the voltage across the FCs like C_{F1}, C_{F2}, C_{F3} and C_{F4} are compared with reference voltage which generates error signal. The squared error based cost function calculates the minimum value of cost function for each of the FC.

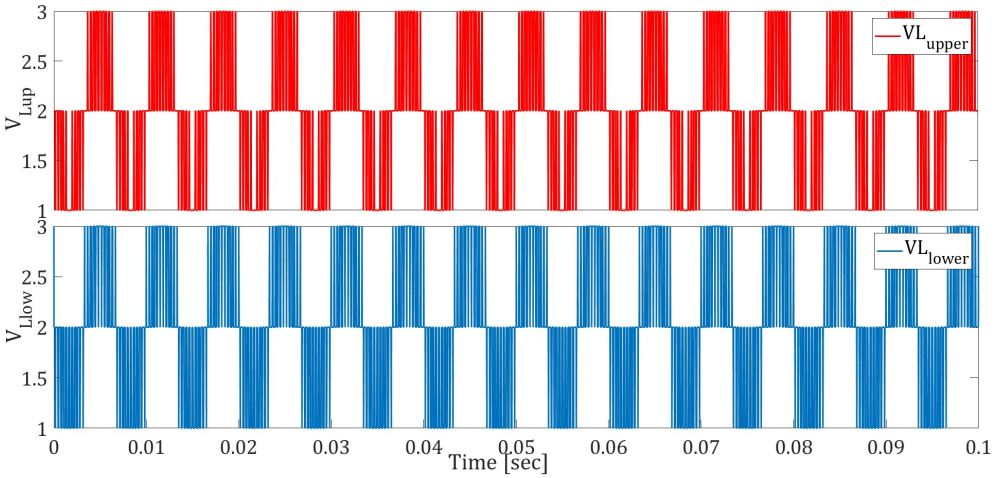

Figure 3.7: Reference voltages levels for upper and lower FC converter stages.

3.2.3 Bubble and sort algorithm

The capacitor voltage balancing sorting algorithm first monitor the values of voltages across the FCs of upper and lower FC converters. The Figure 3.8 shows the sorting mechanism for lower valued cost function. As can be seen from the Figure 3.8, that there are

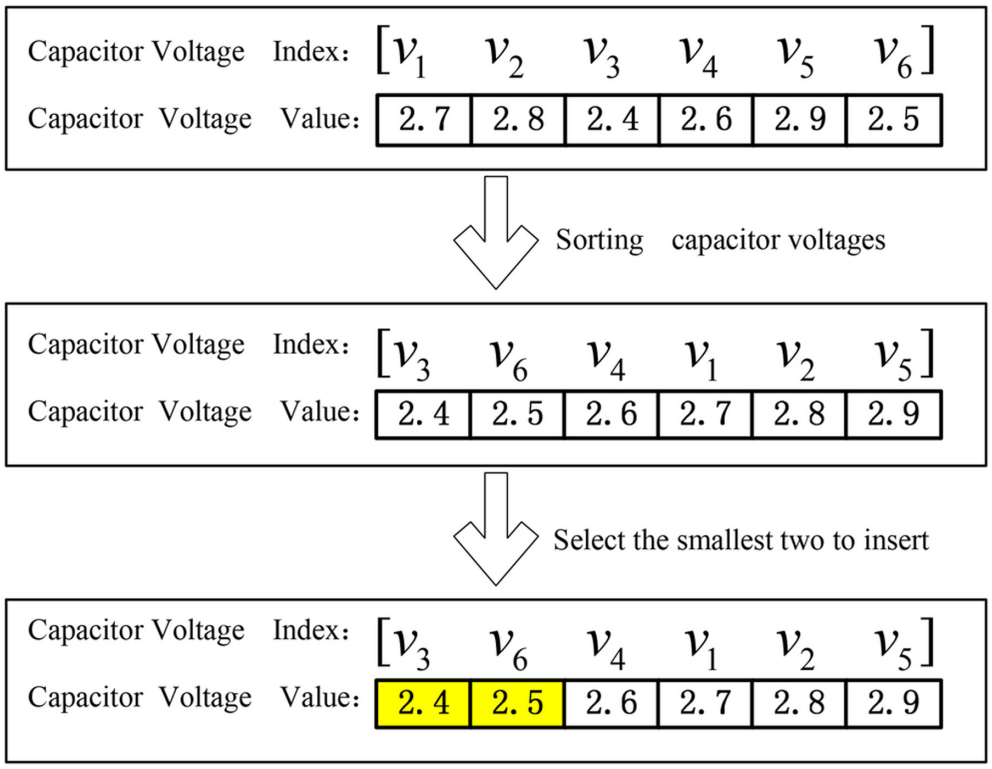

Figure 3.8: Sorting algorithm of FC voltages of upper and lower FC converter stages.

six values of voltages with different values and sorting algorithm sort the the values in a way that it set the minimum value to maximum value. In this way it choose minimum

value of cost function for each of the voltage across the FCs.

3.2.4 Selection of redundant switching state

In this part of the voltage balancing algorithm for FCs, a particular switching state with lower value of the cost function is chosen. For example in a voltage level there are three redundant switching states with different values the state with lower valued cost function is chosen and applied to the converter.

3.2.5 Carrier-Based PWM for multiplexed multilevel Converter

The common PWM modulation techniques used in multilevel converters are the carrier based PWM. Where carrier signal can be a sawtooth wave or triangular wave depends on the implementation required. The carrier signal then compared with sinusoidal modulation signal to generate a PWM signals for the multilevel converters. In case of triangular carrier signal, the PWM modulation occurs when a modulation signal is greater than the triangular carrier signal then output is on state and when the modulation signal lower than the carrier signal then output will in off state. This results in a series of pulses whose widths vary in proportion to the amplitude of the modulation signal, hence the name PWM.

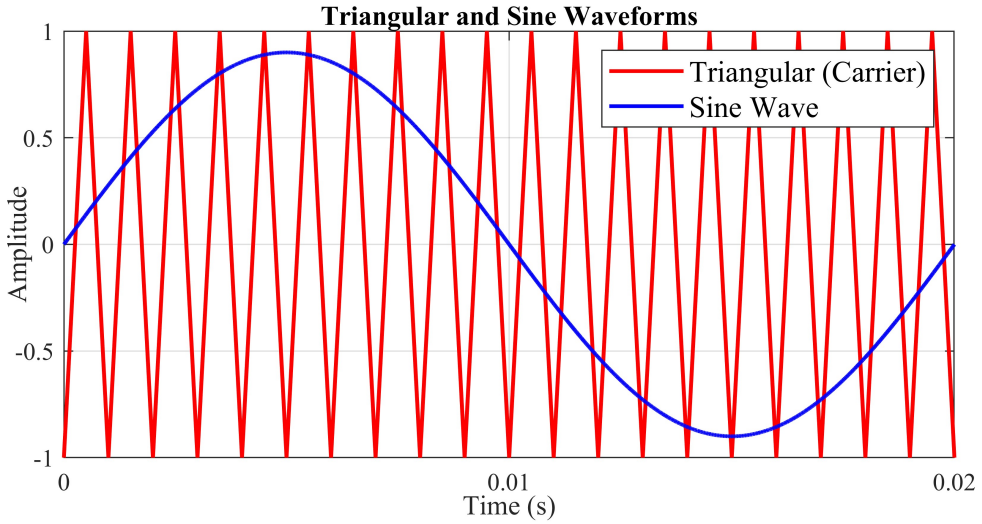

Figure 3.9: Sawtooth carrier based sinusoidal pulse width modulation

The sawtooth based carrier based PWM works in the same way but linearly ramping of sawtooth carrier can influence the converter switching frequency and harmonic contents.

With the help of carrier-based PWM the control of the output voltage, reduce the THD, and improve overall efficiency can be improved in multilevel converters. This technique is widely preferred because of its simplicity, ease of implementation, and effectiveness in producing high-quality voltage waveforms.

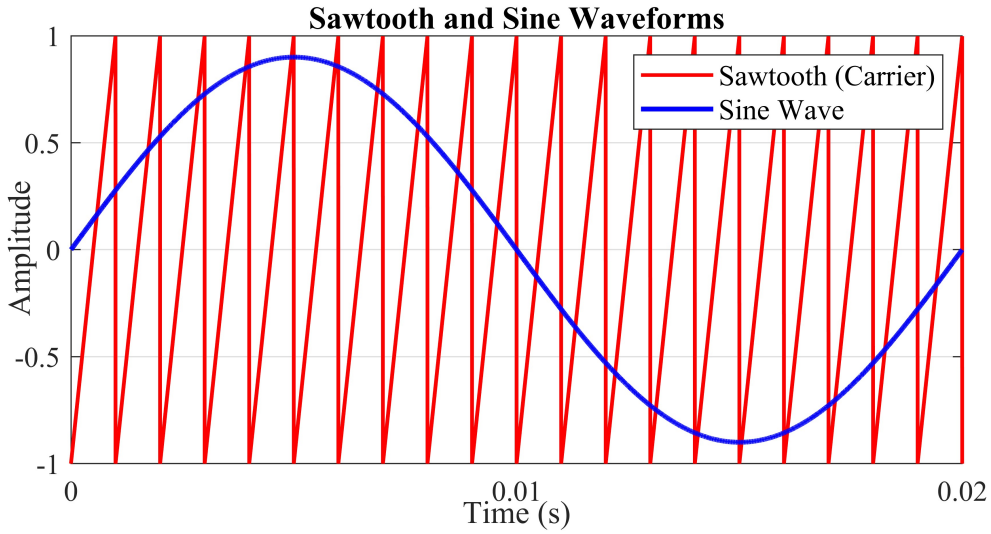

Figure 3.10: Triangular carrier based sinusoidal pulse width modulation

In paper, the classical PWM technique has been extended for diode clamped multilevel inverters. however, the same PWM technique can extended to the FC multilevel converters. In the case of multilevel converters there is only one sinusoidal signal while there there many carrier signals as per the required voltage levels of the converter. For the N-level converter there should be N-1 carrier signals are required. The required carrier signals should have the same frequency, and same peak to peak amplitude. In case of multi-carrier method is the same PWM generation, like in classical method where carrier signal compared with sinusoidal signal. There are N-1 carrier signals and their PWM signal after comparing with sinusoidal signal in each carrier band is the connection to the nearest higher level if the reference signal is higher than the carrier one or the connection to the nearest lower level if the modulation signal is lower than the carrier one.

The phase disposition based modulation for $3\phi 7LM_LM_X$ converter is illustrated in Figure 3.6. The PD-SPWM has been used to control switches of $3\phi 7LM_LM_X$ converter. In the Figure, Car1, Car2, and Car3 are the carriers from 0.5 to 1, used for generating PWM signals for upper FC converter stage of the $3\phi 7LM_LM_X$ converter. Car6, Car7, and Car8 are the carrier signals from -0.5 to -1, used for generating PWM signals for the lower FC

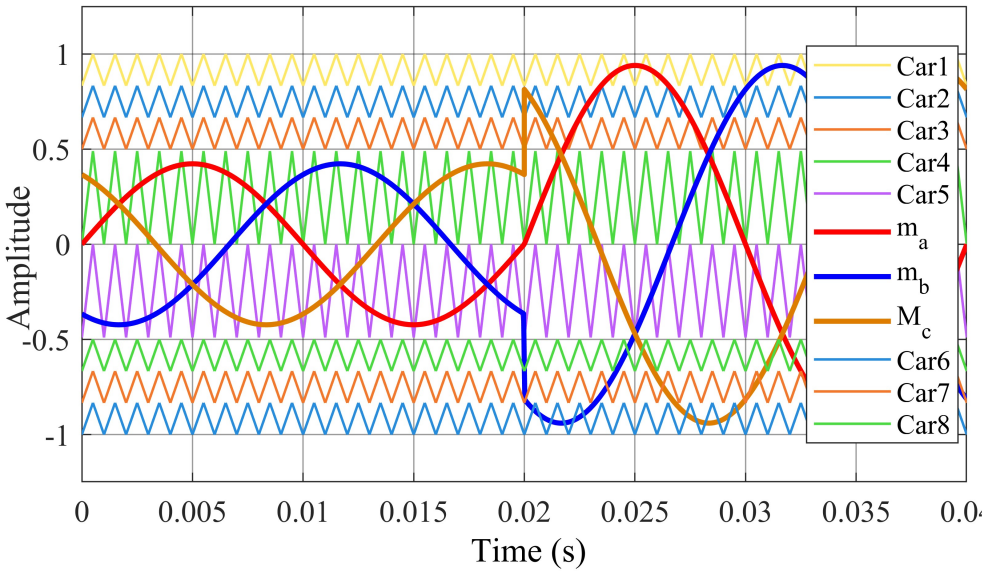

Figure 3.11: Carrier based modulation of $3\phi 7LM_LM_X$ converter.

converter stage of the $3\phi 7LM_LM_X$ converter. Car4 and Car5 signals from -0.5 to 0.5 used for generating PWM signals for NPC stage of the $3\phi 7LM_LM_X$ converter. The $3\phi 7LM_LM_X$ converter operate depending upon the magnitude of the modulation signals. If its lower than 0.5 then only NPC stage of the $3\phi 7LM_LM_X$ converter will operate while the upper and lower FC converter stage will not operate and just send the input same voltage across the input terminals of the NPC stage of the $3\phi 7LM_LM_X$ converter. When the modulation signals are greater the 0.5 then upper, lower stage of FC converter stage along with the NPC stage will be in operation. In detail, when $m < 0.5$ then upper and lower FC converter stages provides $\pm 1/3V_{DC}$. In the upper FC converter stage, the switches S_3, S_5, and S_6 are turned on while in the lower FC converter stage, S_7, S_8, and S_{10} are closed. In the NPC stage of the $3\phi 7LM_LM_X$ converter, the modulating signal (V_{ref}) and two carrier signals (Car4 and Car5) between amplitude of −0.5 and +0.5 are compared to produce the PWM signals for the power semiconductors as shown in Figure 3.11. When modulations signals are greater than 0.5 ($m > 0.5$) it is possible to notice that modulation signals make a transition between upper FC converter, lower FC converter, and NPC converter stage of the $3\phi 7LM_LM_X$ converter. In each stage when the modulation signals are compared with the carrier signals from Carr1 to Car8. The positive top peak of modulation signals compared with Car1, Car2, and Car3, modulation signals from +0.5 to -0.5 compared with Car4, and Car5 for NPC converter operation. Negative peak of the modulation signals is compared with Car6, Car7 and Car8 and generate PWM signals for lower FC converter

stage of the $3\phi 7LM_LM_X$ converter.

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Chapter 4:

Power Losses and Efficiency Calculations

The modeling of power losses in multilevel converters are beneficial in optimal design of multilevel converter and maximize their efficiency around any operating point. Usually, the modeling of power losses for multilevel converters is more complicated that have many, inductors, capacitors, and semiconductors [1, 2]. Under the normal operating conditions, the mostly occurring power losses are: FCs losses, inductors losses, semiconductors switching losses and semiconductor conduction losses. The following section includes the modeling and calculations of these losses.

4.1 Semiconductor power losses

The semiconductors in the multilevel converters perform switching action which helps to converter the voltage from one form to another form. The power losses calculation in semiconductors are very crucial because they higher in quantity which can lead to higher power losses. The power loss dissipation in semiconductors can be categorized into two categories and explained in below subsections.

4.1.1 Conduction losses in semiconductors

The conduction losses in semiconductors occurs because of the semiconductors have some resistance to the flow of current which causes some amount of voltage drop across the semiconductors during the conduction state of the semiconductors. The technology used for calculating the conduction losses in this thesis is the IGBT. The energy lost during a conduction loss in an IGBT can computed as [3]:

$$E_{\text{con, IGBT}} = \int_0^t R_{dson} \cdot i(t)^2 dt \tag{4.1}$$

The total conduction power losses of the IGBT ($P_{\text{con, IGBT}}$) can calculated as:

$$P_{\text{con, IGBT}} = E_{\text{con, IGBT}}/t; \tag{4.2}$$

Where E_{con} is the energy dissipated during the conduction state of IGBT, R_{dson} is the resistance offered by an IGBT during the conduction of current in its on state and $i(t)$ instantaneous current flowing through an IGBT at the instant of time t. The conduction power losses in IGBT are represneted as $P_{con,IGBT}$ The conduction losses in a body diode [3] of the IGBT can computed as in below equation.

$$E_{\text{con, diode}} = U_{\text{diode}} \cdot I_{\text{diode}} \cdot \left(\frac{t_{\text{rise}}}{2} + \frac{t_{\text{fall}}}{2} + t_{\text{don}} + t_{\text{dead}} \right) \tag{4.3}$$

$$P_{\text{con, diode}} = E_{\text{con, diode}}/(t_{rise} + t_{fall} + t_{don} + t_{dead}) \tag{4.4}$$

Where, E_{diode} in energy drop across the body diode, P_{diode} is the total power loss in diode, U_{diode} and I_{diode} are the forward voltage drop and current through the body diode. The t_{rise}, t_{fall}, t_{don}, and t_{dead} are the rise, time, fall time, on-off delay time, and dead time (that is between turn on of one switch and turn-off of other switch) of the body diode.

In the inductive circuits, when an IGBT turn on or turn off the circuit or may interact with circuital parasitic inductance. In these circuits the lower time is required to change the state of switching which might produce high voltage spikes that can damage an IGBT. To cope with this issue an IGBT comes with a bode diode that help the current to flow when IGBT commutates to a blocking state.

4.1.2 Switching power losses

Switching losses in the semiconductors occurs when it change its state from blocking state to conduction state and vice versa. Switching losses of any IGBT are the function of supplied voltage, current and required switching time in a period. Every switching time when an IGBT change its state, the energy dissipated in the system [4]. That energy lost is give by the energy lost during turn-off and turn on of the IGBT. When an IGBT turn on, its free-wheeling diode has some losses that is reverse recovery loss ($E_{off,Diode}$) within that diode and an additional loss ($E_{off,Diode-IGBT}$) depends on additional reverse recovery

current flows inside the IGBT. The overall switching losses of an IGBT can be calculated as [5]:

$$E_{sw} = E_{off,IGBT} + E_{on,IGBT} + E_{off,Diode} + E_{off,Diode-IGBT}$$

$$\begin{aligned}
&E_{off,IGBT} = E_{on,Diode} = \frac{1}{4} \cdot V_{in} \cdot I \frac{t_{rise} + t_{fall}}{2} \cdot V_{in};\\
&E_{off,Diode} = \frac{1}{4}.Q_{rr}.Vin;\\
&E_{off,IGBT} = .Q_{rr}.Vin;\\
&P_{off,IGBT} = E_{off,IGBT}/(t_{rise} + t_{fall});\\
&P_{on,IGBT} = E_{on,IGBT}/(t_{rise} + t_{fall});\\
&P_{sw,IGBT} = P_{off,IGBT} + P_{on,IGBT};
\end{aligned} \tag{4.5}$$

Where, E_{sw} are the switching losses of the converter, V_{in} is the input supplied voltage, Q_{rr} is the diode reverse recovery charge, t_{rise}, t_{fall} are the rise time and fall of the IGBT, $P_{off,IGBT}$ and $P_{on,IGBT}$ are power losses during off and on transition, and $P_{sw,IGBT}$ are total switching losses of the IGBT.

4.2 Losses in flying capacitors

In FC converters, the FCs are subjected to charging and discharging currents during switching operations, resulting in power losses primarily due to their equivalent series resistance (ESR) [5]. These losses are generally smaller than semiconductor conduction and switching losses but can be significant in high-power applications or when using capacitors with non-negligible ESR. The power loss in an individual FC is calculated as [6].

$$P_{C_f} = I^2_{C_f,\text{rms}} \cdot \text{ESR}_f \tag{4.6}$$

whereP_{Cf} is the power loss in a FC, $I_{C_f,\text{rms}}$ is the root-mean-square (RMS) current through the FC, and ESR_f is its equivalent series resistance (typically provided in the capacitor datasheet and frequency-dependent). The conduction losses in all normal FCs

C_{F1} and C_{F2} can be calculated by:

$$P_{c_f,\,\text{total}} = \sum_k I^2_{C_fk,\text{rms}} \cdot \text{ESR}_{fk} \tag{4.7}$$

Where, $P_{c_f,\,\text{total}}$ is the total power loss in the FCs k indicates the number of FCs, I_fk is the current flowing through each FC and ESR_{fk} is the ESR in each FC of the converter.

4.3 Total Losses

By adding the each losses of the individual component, the total losses of the $3\phi 7LM_LM_X$ converter can be calculated by:

$$P_{lossesT} = P_{con,IGBT} + P_{sw,IGBT} + P_{c,total} + P_{con,diode} \tag{4.8}$$

Where, P_{con} is conduction power loss of an IGBT, P_{sw} is the switching power loss across an IGBT, $P_{c,total}$ is the total power loss in FCs of the converters.

4.4 Calculations of power losses and efficiency

The simulations are performed using MATLAB®Simscape (R2024a or later), which incorporates an advanced semiconductor device library that allows direct importation of detailed datasheet parameters for Hitachi high-voltage IGBT modules directly from the manufacturer's official website. This integrated workflow eliminates the need for manual curve fitting and significantly enhances the modeling accuracy and real behavior of the semiconductors. In MATLAB®Simulink R2024, the power loss summary of the semiconductors used in the multilevel converters can be used generated using specialized functions like "ee_getPowerLossSummary" or "ee_getPowerLossTimeSeries" on simulation log data (e.g., simlog_YourModel) to get average losses or time-varying losses for components like diodes, IGBTs, etc., providing insights into conduction and switching losses for thermal analysis or efficiency studies. An example summary of the losses of all components used in multilevel converters are calculated and shown in Figure 4.1.

The efficiency of converter can also be calculated easily using "ee_getefficiency (loa-

LoggingNode	Power	SwitchingLosses
{'IGBTThermal.Load' }	11385	0
{'IGBTThermal.S1' }	5.9888	691.14
{'IGBTThermal.S3' }	5.6716	4.5955
{'IGBTThermal.S4' }	5.6708	345.04
{'IGBTThermal.S2' }	5.5666	2.2875
{'IGBTThermal.Diode1' }	0.0039122	0
{'IGBTThermal.Diode2' }	0.0028541	0
{'IGBTThermal.Resistor3' }	5.6924e-06	0
{'IGBTThermal.Resistor2' }	5.6924e-06	0
{'IGBTThermal.PWM.Half_Bridge_Driver' }	0	0
{'IGBTThermal.Subsystem1.Half_Bridge_Driver1'}	0	0

Figure 4.1: Power losses calculation for multilevel converter.

didentifier,node)". This command is verified and compared with manual conventional way of calculating the efficiency of converter.

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Chapter 5:

Results and Discussion

In this thesis an in-depth comparative analysis is conducted to evaluate the performance of the $3\phi 7LM_LM_X$ converter with the conventional $3\phi 3LNPC$ converter topologies. The investigation focuses on several critical electrical and thermal parameters, including the voltage balancing dynamics across the FCs, characteristic output voltage and current waveforms, voltage stress distribution across the IGBTs, total power losses (comprising conduction losses and switching losses), and overall efficiency of the converter. These performance metrics are rigorously examined under a wide range of operating conditions, specifically at high, medium, and low modulation indices, to provide a comprehensive understanding of the converters' behavior across the entire modulation range. For the $3\phi 7LM_LM_X$ converter topology, appropriate IGBT devices are selected for the upper FC converter stage, lower FC converter stage and the NPC stage. Specifically, the Hitachi 5SNG0900R120590 IGBT, rated to block $V_{dc}/6$, is employed in the both upper and lower FC converter stages, whereas the Hitachi 5SNA1000G650300 IGBT, designed for a blocking voltage of $V_{dc}/2$, is utilized in the NPC stage. These device selections align with the voltage stress requirements inherent to each sub-module within the hybrid seven-level structure. All simulations are performed using the Simscape Electrical toolbox within the latest release of MATLAB®. This advanced simulation environment incorporates detailed physical modeling of semiconductor devices, including accurate thermal networks that account for junction temperature variations under realistic operating conditions. Furthermore, the built-in loss calculation and efficiency estimation features of Simscape enable precise quantification of conduction losses, switching losses, and reverse-recovery effects, thereby facilitating a robust and reliable comparative assessment of the two converter topologies.

The parameters for $3\Phi 3L$ NPC converter and $3\Phi 7LM_LM_X$ converter are shown in Table 5.1. The switching losses, conduction losses, efficiency, and THD are evaluated

according to the parameters shown in Table 5.1 for $3\Phi 3L$ NPC and $3\Phi 7LM_LM_X$ converters.

The detailed electrical and operational parameters for both $3\phi 3L$ NPC converter and the $3\phi 7LM_LM_X$ converter are comprehensively presented in Table 5.1. These parameters include, DC-link voltage (V_{dc}), FCs capacitance values, output filter inductance (L), load specifications (R), switching frequency (F_{sw}), and modulation strategy employed in the simulation study.

Table 5.1: Parameters for a $3\phi 7LM_LM_X$ converter.

Parameter	Value
DC-Bus voltage (V_{dc})	5000 V
Switching frequency (F_{sw})	3000 Hz
Fundamental frequency (F_m)	50 Hz
Load inductance per phase (L)	20 mH
Load resistance per phase (R)	5Ω

Figure 5.1 shows the calculated THD in the load current against the load current for $3\Phi 7LM_LM_X$ converter and $3\Phi 3L$ NPC converter. The $3\Phi 7LM_LM_X$ converter has lower THD at lower, medium, and higher load currents. For the $3\Phi 7LM_LM_X$ converter, the THD values are calculated as 0.6% at a higher load current of 173A, 0.6% at 145A, 0.7% at 112A, 0.8% at 73A, 0.7% at a load current of 58A and 1.7% at a lower load current of 29A. In contrast, for the $3\Phi 3L$ NPC converter, the THD values are 1.4% at 173A, 1.8% at 145A, 2.3% at 112A, 2.8% at 73A, 3% at 58A, and 3.5% at a lower load current of 29A.

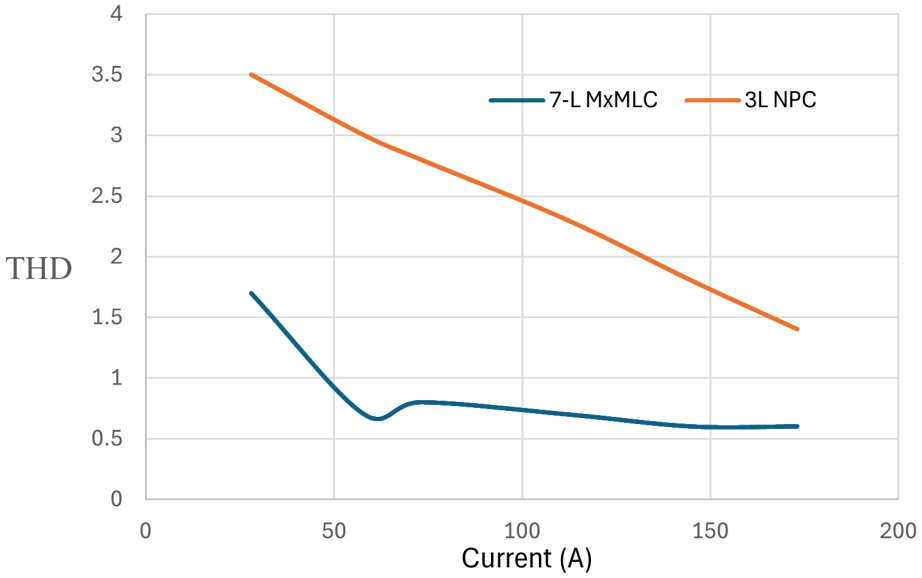

Figure 5.1: THD in the load current of $3\Phi 3L$ NPC converter and $3\Phi 7LM_LM_xC$ converter.

The voltage stress across the IGBTs and voltage during switching in the upper FC converter stage of the multiplexed converter is just $V_{dc}/6$. The voltage stress across each IGBT in the NPC stage and FC converter stage of the $3\phi 7LM_LM_X$ converter is $V_{dc}/2$. The voltage during switching in the FC converter stage is $V_{dc}/6$, while in the NPC stage, it varies depending on the switches: $S_{1a} = V_{dc}/3$, $S_{1b} = V_{dc}/6$, and similarly for their complementary switches in each phase, as detailed in Table 5.2. The voltage stress across

Table 5.2: Voltage stress across the switches of $3\Phi 7LM_LM_X$ converter.

FCC Stage of 3ϕ7LM$_L$M$_X$ converter		
Switch Number	Voltage Stress	Voltage during switching
S_1-S_{12}	$\frac{V_{dc}}{6}$	$\frac{V_{dc}}{6}$
NPC Stage of 3ϕ7LM$_L$M$_X$ converter		
S_{1a}, S_{4a}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{3}$
S_{2a}, S_{3a}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{6}$
S_{1b}, S_{4b}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{3}$
S_{2b}, S_{3b}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{6}$
S_{1c}, S_{4c}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{3}$
S_{2c}, S_{3c}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{6}$

the IGBTs and voltage during switching for each IGBT of the conventional $3\Phi 3L$ NPC converter are shown in Table 5.3. Both voltages are same and it has higher voltage during switching and voltage stress of $V_{dc}/2$ compared with the $3\Phi 7LM_LM_X$ converter which causes more switching losses in $3\Phi 3L$ NPC converter than the $3\Phi 7LM_LM_X$ converter.

Table 5.3: Voltage stress across the switches of $3\phi 3L$ NPC converter.

$3\phi 3L$ NPC converter		
Switch Number	Voltage Stress	Voltage during switching
S_{1a} - S_{4a}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
S_{1b} - S_{4b}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
S_{1c} - S_{4c}	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$

Figures 5.2 and 5.3 represent the waveform of the voltage across the IGBTs for the NPC stage and both FC converter stages of $3\phi 7LM_LM_X$ converter respectively, where voltage during switching and voltage stress can be seen from the waveforms for switches. For $3\phi 3L$ NPC stage the waveforms of only upper switches of one leg are shown. For FC

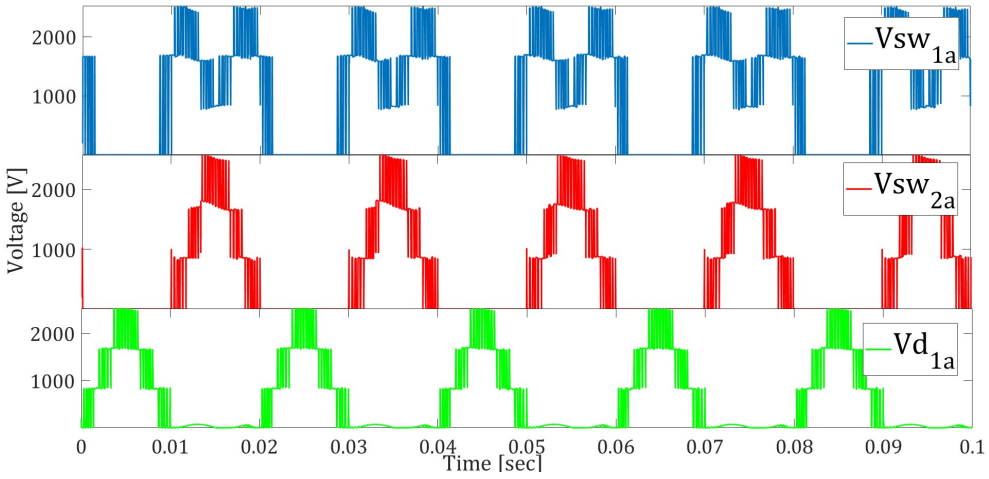

Figure 5.2: Voltage across the IGBTs of S_{1a}, S_{2a}, and D_{1a} in the NPC stage of $3\Phi 7LM_LM_X$ converter.

converter stage the waveforms of upper switches in the upper FC converter stage of $3\phi 7LM_LM_X$ converter are shown.

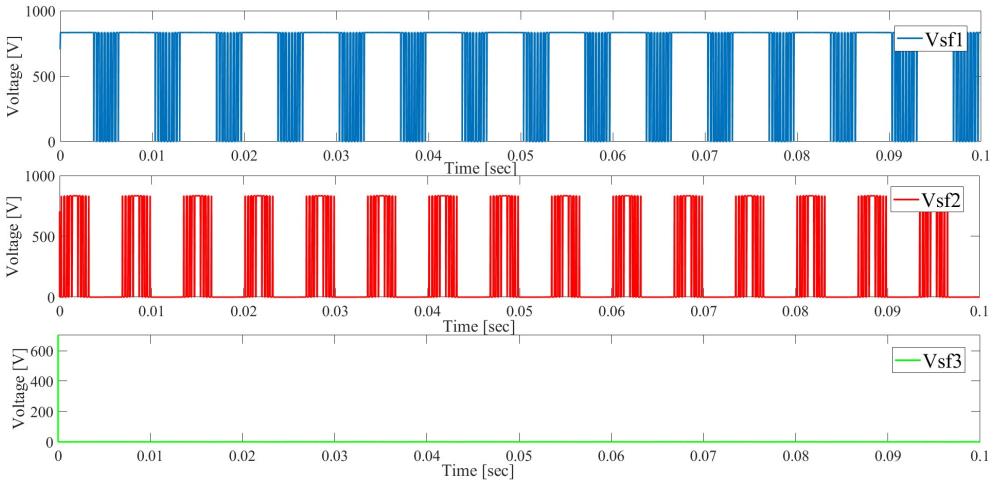

Figure 5.3: Voltage stress across IGBTs of S_1, S_2 and S_3 in upper FC converter stage of $3\phi 7LM_LM_X$ converter.

The four-level upper and lower FC converters of $3\Phi 7LM_LM_X$ converter will act like 3-level converters by always closing the switch S_3 from the upper FC converter stage and S_{10} from the lower FC converter stage. This is because the zero voltage level will be generated by the NPC stage of $3\Phi 7LM_LM_X$ converter. The output voltage from upper FC converter stage and lower FC converter stage are shown in Figure 5.4. The red waveform indicates the output voltage of the upper FC converter stage, and blue waveform is the output voltage of the lower FC converter stage. At higher load current the converter operates at higher modulation index and has maximum voltage of $\pm V_{dc}/2$ across the FC

converter stages. During medium load current of 145A the voltage across the upper and

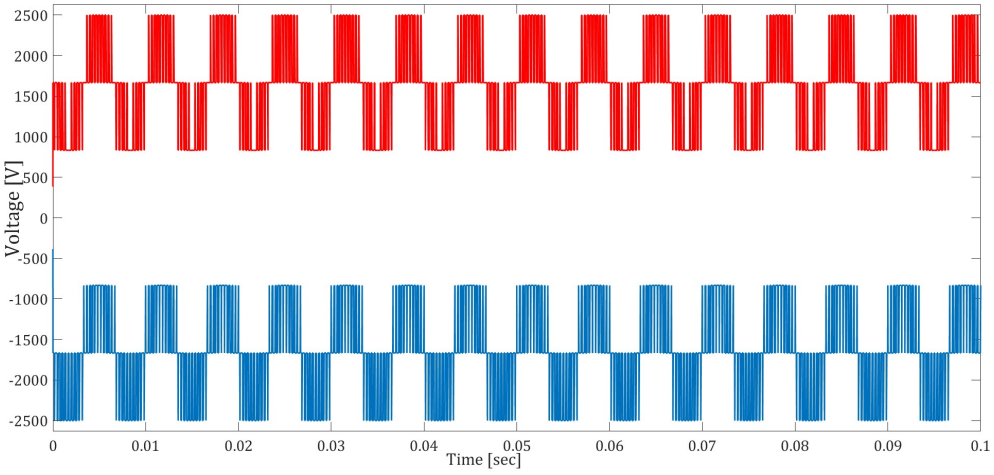

Figure 5.4: Output voltage across the FC converter stages of $3\phi 7LM_LM_XC$ converter during a high load current of 173A.

lower FC converters stages of $3\Phi 7LM_LM_X$ converter are shown in figure 5.5. The switch S_1 is always opened because voltage $V_{dc}/2$ is clipped out and voltage $V_{dc}/3$ is the peak voltage. The switch S_2 will perform switching as the output voltage, while the switch S_3 will always remain closed. For lower FC converter stage, the switch S_7 will always remain open, switch S_8 will perform switching as output voltage of lower FC converter stage while S_9 will always remain closed. The red and blue waveforms indicate the output voltage across the upper FC converter stage and lower FC converter stage. In this medium current stage the modulation index decrease accordingly and maximum voltage across the FC converter stage is $\pm V_{dc}/3$.

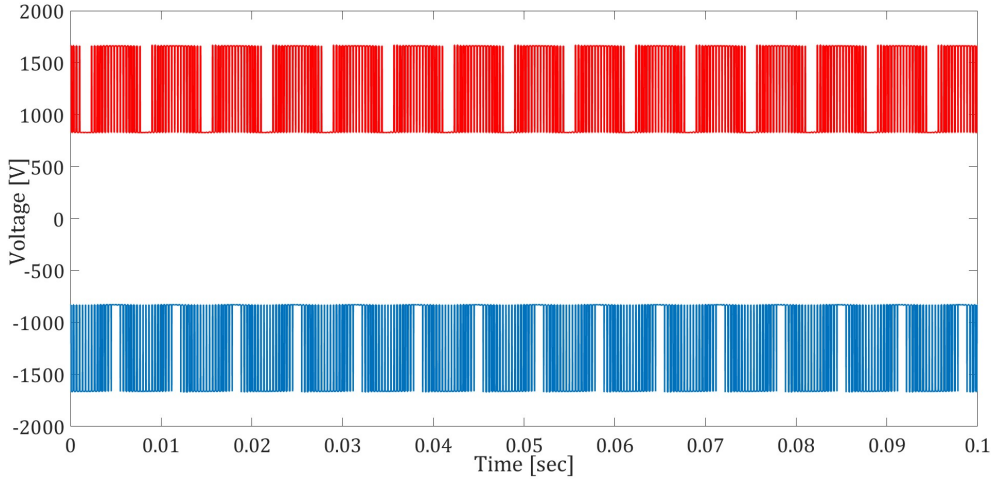

Figure 5.5: Output voltage across the FC converter stages of $3\phi 7LM_LM_X$ converter during a medium load current of 145A.

During the lower load current of 58A or 28A in $3\Phi 7LM_LM_XC$ so, as explained earlier, it is verified from the Figure 5.6 that switches S_3, S_5, and S_6, will remain closed while in lower FC converter part S_7, S_8, and S_{10}, will be closed which will allow only $V_{dc}/6$ voltage from FC converter stage to NPC stage of the $3\Phi 7LM_LM_X$ converter.

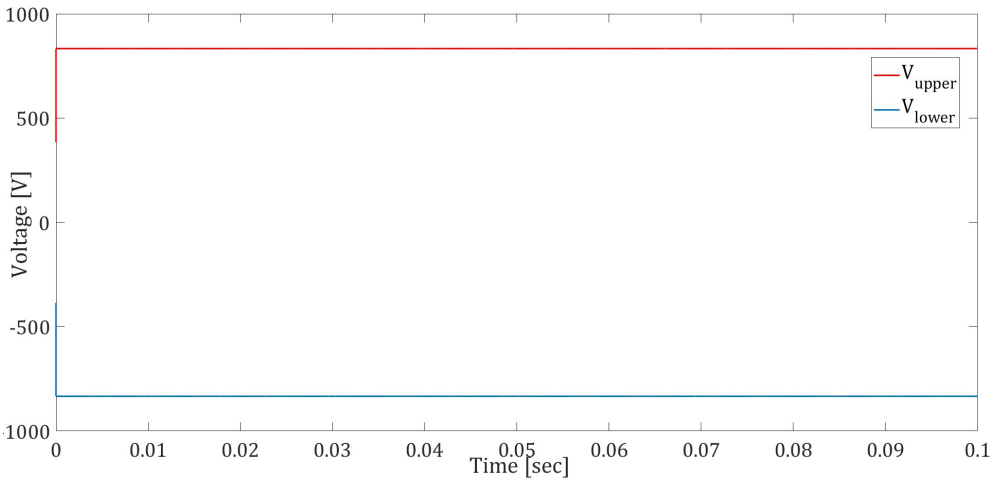

Figure 5.6: Output voltage across the FCC stage of $3\phi 7LM_LM_XC$ converter during a low load current of 58A.

The losses of the $3\Phi 7LM_LM_X$ converter and $3\Phi 3L$ NPC converter are evaluated based on the converter's parameters shown in the Table 5.1 and results are reported in Figure 5.7 to Figure 5.9. The voltages during switching in the upper FC converter, lower FC converter and NPC stages of the $3\Phi 7LM_LM_X$ converter are lower than the conventional $3\phi 3L$ NPC converter. So, the switching losses are much lower in $3\Phi 7LM_LM_X$ converter. The switching power losses, power conduction losses, and total power losses of the $3\Phi 7LM_LM_X$ converter and $3\phi 3L$ NPC converter at higher, medium, and lower modulation indexes are shown in Figure 5.7, Figure 5.8 and Figure 5.9 respectively. In Figure

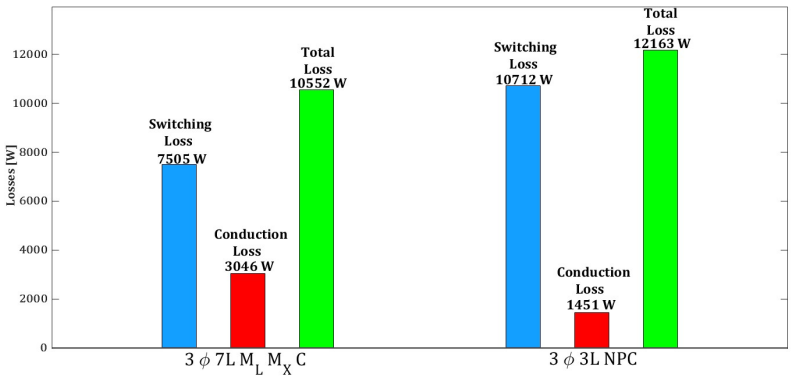

Figure 5.7: Losses of IGBTs in $3\phi 7LM_LM_X$ and $3\phi 3L$ NPC converters during a load current of 173A.

5.8 the $3\phi 7LM_LM_X$ and $3\phi 3L$ NPC Converters operate at the same load current and load parameters. Compared with the $3\phi 3L$ NPC Converter, the $3\phi 7LM_LM_X$ converter exhibits more conduction losses because of the large number of switches, while it has lower switching losses. But the total losses of the $3\phi 7LM_LM_XC$ are lower comparatively. The

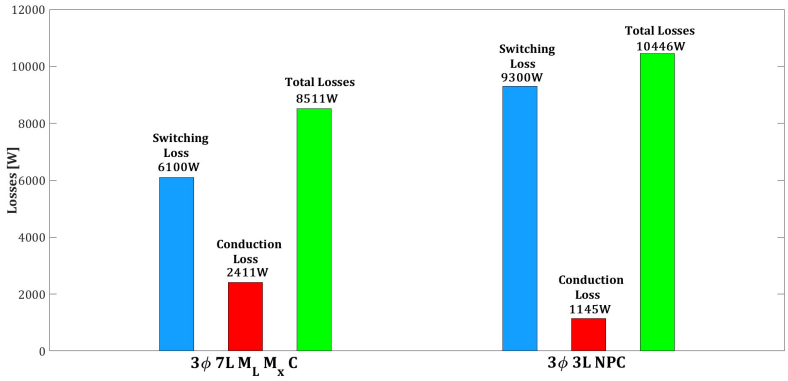

Figure 5.8: Losses of IGBTs in $3\phi 7LM_LM_XC$ and $3\phi 3L$ NPC converters during load current of 145A.

same case for medium and smaller load currents. The total losses of the $3\phi 7LM_LM_X$ converter are less than the $3\phi 3L$ NPC converter under similar load conditions and switching frequency. Tables 5.2 and 5.3 present the voltage across the switches and the voltage

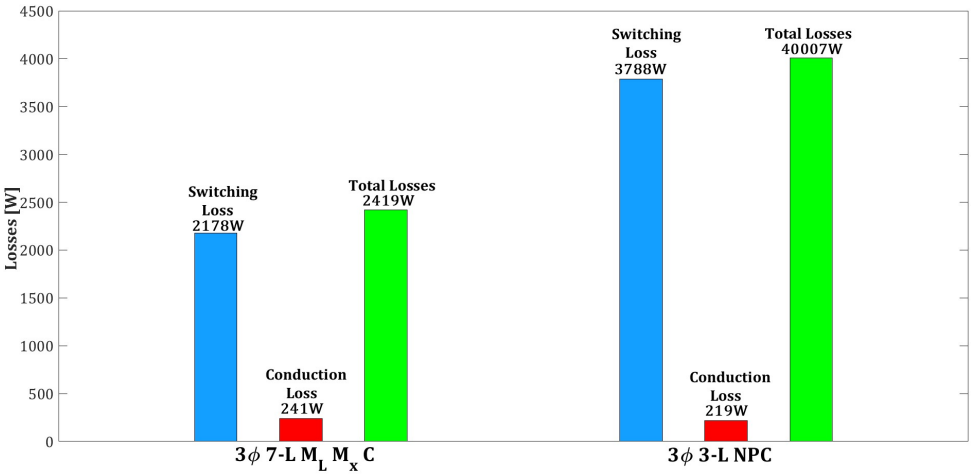

Figure 5.9: Losses of IGBTs in $3\phi 7LM_LM_XC$ and $3\phi 3L$ NPC converters during load current of 58A.

during switching for the $3\Phi 3L$ NPC converter and the $3\Phi 7LM_LM_xC$. While the voltage stress across the switches is identical in both converters, the voltage during switching is higher in the conventional $3\Phi 3L$ NPC converter. It is evident from Figures 5.7, 5.8, and 5.9 that the switching losses are higher in the $3\Phi 3L$ NPC converter. However, its conduction

losses are lower due to the reduced number of switches compared to the $3\Phi7LM_LM_xC$. As a result, $3\Phi7LM_LM_xC$ has slightly higher efficiency.

Table 5.4: Comparison of $3\phi3L$ NPC converter and $3\Phi7LM_LM_X$ converter.

Parameter	$3\Phi3L$ NPC	$3\Phi7LM_LM_X$ converter	
		FC stage of $3\Phi7LM_LM_XC$	NPC stage of $3\Phi7LM_LM_XC$
Number of switches	12 + 6 clamping diodes	12	12 + 6 clamping diodes
Voltage during switching	$S_1 = V_{dc}/2$	$S_1 = V_{dc}/6$ $S_2 = V_{dc}/6$ $S_3 = V_{dc}/6$	$S_1 = V_{dc}/3$ $S_2 = V_{dc}/6$ $D_1 = V_{dc}/6$
Voltage stress	$V_{dc}/2$	$V_{dc}/6$	$V_{dc}/2$
Voltage levels	3	7	
Efficiency	97.9%	98.1%	

The Table 5.4 summarize the detailed comparison of two converters as:

- The $3\phi3L$ NPC converter requires 12 switches plus 6 clamping diodes, while the $3\Phi7LM_LM_X$ converter uses 12 switches in its FC stage and 12 switches plus 6 clamping diodes in its NPC stage.
- In the $3\phi3L$ NPC topology, switches experience a voltage stress of $V_{dc}/2$ during switching operations.
- The FC stage of the $3\phi3L$ NPC converter distributes voltage more evenly, with switches S_1, S_2, and S_3 each handling $V_{dc}/6$, resulting in lower voltage stress of $V_{dc}/6$.
- The NPC stage of the $3\phi3L$ NPC converter has S_1 experiencing $V_{dc}/3$, S_2 experiencing $V_{dc}/6$, and diode D_1 handling $V_{dc}/6$, with an overall voltage stress of $V_{dc}/2$.
- The $3\phi3L$ NPC converter generates 3 distinct voltage levels for output waveform synthesis.
- The $3\phi3L$ NPC converter produces 7 voltage levels, providing better harmonic performance and smoother output waveforms compared to the 3-level topology.
- The $3\phi3L$ NPC achieves an efficiency of 97.9%, while the $3\Phi7LM_LM_X$ converter demonstrates improved efficiency at 98.1%.

- The multilevel approach in the $3\Phi 7LM_LM_X$ converter reduces switching losses and voltage stress on individual components, contributing to the higher efficiency despite increased complexity.

Chapter 6:

Conclusion

This thesis has presented a comprehensive comparative study of the conventional $3\phi 3L$ NPC converter and the $3\phi 7LM_LM_X$ Converter. The analysis focused on critical performance indicators, including THD of the output voltage and current, conduction losses, switching losses, voltage stress across semiconductors during commutation, semiconductors count, and overall power efficiency under different modulation indices and load conditions. Simulation results, obtained using the electro-thermal modeling capabilities of MATLAB® Simscape library, conclusively demonstrate the superior performance of the $3\phi 7LM_LM_X$ converter topology in several key aspects. Notably, the transitions voltage across individual semiconductors in the $3\phi 7LM_LM_X$ converter is significantly lower than in the $3\phi 3L$ NPC converter and that is limited to $V_{dc}/6$ in the FC converter stage and $V_{dc}/6$ in the NPC stage—compared to the full $V_{dc}/2$ blocking voltage in the conventional $3\phi 3L$ NPC converter. In FC converter stage the semiconductors have maximum voltage stress of $V_{dc}/6$ which much lower than the conventional NPC converter while NPC stage of multiplexed converter has voltage stress during switching is just $V_{dc}/6$. This reduced voltage stress during transition state contributes in $3\phi 7LM_LM_X$ converter to lower switching losses, decreased dv/dt stress, improved electromagnetic compatibility and does not cost much as compared with conventional $3\phi 3L$ NPC converter. Despite requiring a higher switch counts (30 active switches in $3\phi 7LM_LM_X$ converter and 18 in the $3\phi 3L$ NPC), the $3\phi 7LM_LM_X$ converter exhibits superior output power quality. The THD remains consistently low and nearly independent of load current variations, whereas the $3\phi 3L$ NPC shows a pronounced increase in harmonic distortion at lighter loads. This robustness in waveform quality across the operating range makes the $3\phi 7LM_LM_X$ converter topology particularly advantageous for applications with variable or dynamic loading, such as RESs integration and variable-speed drives. In terms of efficiency, the $3\phi 7LM_LM_X$ converter achieves marginally higher values than the $3\phi 3L$ NPC across the

different modulation range, primarily due to reduced switching losses enabled by lower switch voltage stress and optimized switching transitions although it has more switch counts.

In summary, the $3\phi 7LM_LM_X$ converter represents a compelling advancement over the conventional $3\phi 3L$ NPC topology, delivering enhanced output power quality, lower THD, lower switch stress, and improved efficiency, albeit at the cost of increased design complexity. These attributes position it as a highly suitable candidate for next-generation medium- and high-power conversion systems, including grid-tied photovoltaic inverters, wind power converters, medium-voltage motor drives, and flexible AC transmission systems (FACTS) devices.